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Article

Research on Layered Control and Fault Recovery Mechanisms for Fast Charging Safety Diagnosis of High-Voltage Battery Systems under Charging Network Interoperability Conditions

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Abstract

In public DC fast-charging scenarios, protocol inconsistencies, current-limiting variations, and communication anomalies often lead to handshake failures, current oscillations, voltage overshoot, and delayed fault recovery. Under high-power conditions, mishandling these issues can cause prolonged high-temperature, high-stress battery operation, elevating safety risks. To address this, a fast-charging safety framework is proposed, integrating hierarchical control, fault diagnostics, and staged recovery for high-voltage battery systems. A charging state machine is designed to cover phases such as handshake, pre-charge, CC/CV transition, derating, disconnection, and recovery. Transition nodes include consistency checks to handle packet loss, timing errors, and abnormal responses. Charging current is generated through a constrained optimization model incorporating cell voltage, temperature rise, predicted power limits, protection boundaries, equipment constraints, and diagnostics-based disconnection triggers. The system enables smooth, recoverable current control and active fault response. Tests across 3,000 sessions show a 38% drop in interruption rate, recovery time cut from 6.5 s to 2.1 s, voltage overshoot reduced by 45%, and peak temperature rise lowered by 0.8–1.3 °C. This validates the framework's effectiveness for safe, stable fast charging in complex, interoperable networks.

Keywords: DC fast charging; charging interoperability; high-voltage battery systems; safety diagnostics; hierarchical control; constrained optimization; controlled disconnection; fault recovery; bus stability

1. Introduction

The rapid expansion of public DC fast-charging networks has amplified interoperability challenges across multi-protocol systems. Variations in protocol implementation, current-limiting strategies, and communication reliability often result in charging interruptions and overprotection, compromising system safety and stability. Zhao et al. [1] emphasized the importance of electrothermal coupling in diagnostics. Franzese et al. [2] identified protocol-device mismatches as a major failure source. Sharma et al. [3] proposed a fault-tolerant strategy lacking multi-stage coordination and risk assessment. Madani et al. [4] focused on battery modeling, while Esfahani et al. [5] introduced a hierarchical control method without fault recovery logic. Few existing solutions jointly address anomaly detection, recoverable current control, and smooth disconnection. This work proposes a unified framework integrating MPC-based scheduling, risk-index diagnostics, and protocol-aware recovery to enable structured transitions, health-informed constraints, and adaptive disconnection for high-voltage batteries in complex charging environments.

2. Problem Analysis and System Modeling Under Charging Interoperability Conditions

In public DC charging networks, high-voltage battery systems often encounter control instability and ambiguous state recognition due to inconsistent protocol implementations, varying current-limiting strategies, and communication failures. These issues commonly lead to handshake failures, mid-session current fluctuations, and end-phase voltage overshoot during fast charging, posing serious risks to system stability and thermal safety margins[6]. To establish a unified analytical framework, the fast charging process is abstracted as a state-driven dynamic system. System state is represented as $x(t)$, control input as $u(t)$, and environmental disturbance as $d(t)$. The system state transition model is constructed as follows:

$$\frac{dx(t)}{dt} = A_s x(t) + B_s u(t) + E_s d(t) \quad (1)$$

Here, A_s is the state transition matrix reflecting the physical dynamics across different charging phases; B_s represents the charging device's response capability to control commands; and E_s is the disturbance coupling matrix accounting for communication delays, charging station response lags, and grid fluctuations. Figure 1 illustrates the typical evolution path of abnormal operating conditions triggered by interoperability events, clarifying the influence of different anomaly types on state transitions.

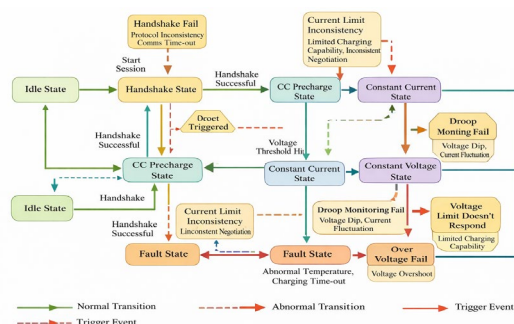


Figure 1. Path diagram of charging state transitions triggered by interoperability anomalies.

To enhance the model's engineering applicability, a set of state variable consistency constraints (\mathcal{C}_s) is introduced to detect structural consistency between the handshake state and bus voltage/current responses:

$$\mathcal{C}_s = \{x(t) \mid |V_{dc}^{meas} - V_{dc}^{ref}| \leq \varepsilon_v, \quad |I_{dc}^{meas} - I_{dc}^{cmd}| \leq \varepsilon_i\} \quad (2)$$

Here, V_{dc}^{meas} and I_{dc}^{meas} represent real-time bus voltage and current feedback, respectively, while V_{dc}^{ref} , I_{dc}^{cmd} denotes the desired reference value. ε_v , ε_i indicate the upper tolerance limits for state responses. This consistency constraint provides real-time discrimination during communication packet loss, control delays, and response anomalies, serving as the foundational basis for subsequent hierarchical control strategy triggering mechanisms.

3. Hierarchical Control and Current Command Optimization Strategy for Fast Charging

3.1. Hierarchical Control Architecture Design

The hierarchical control structure effectively addresses coordination failures caused by communication anomalies and device response variations during interoperable charging (As shown in Figure 2)

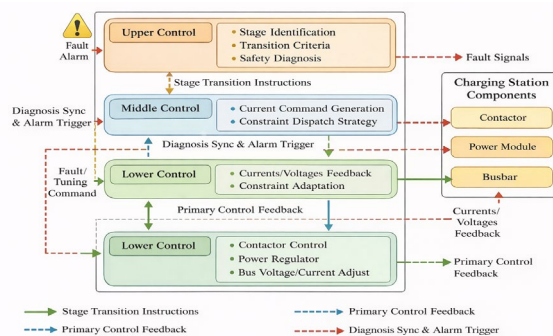


Figure 2. Functional Distribution of Layered Control Structure in Fast Charging Process.

3.2. Modeling the Current Command Optimization Problem

During high-voltage fast charging, current command generation must balance constraints from system boundaries, multi-source data, and safety requirements. The control system constructs a multi-time-domain coupled information structure using current state, historical data, and short-term load forecasts[7]. The middle-layer module formulates current command generation as a dynamic optimization problem, with objectives to balance charging rate, thermal stress, and bus stability. Decision variables are current setpoints across future cycles. Constraints include maximum cell voltage, current slope, surge voltage limits, current-limiting strategies, and upper-layer risk commands. This modeling ensures that generated commands are feasible, recoverable, and responsive to abnormal conditions.

3.3. Current Command Generation Algorithm Design and Implementation

Based on the multi-constraint optimization model, the current command generation adopts a receding-horizon control scheme that combines rolling prediction and real-time correction to maintain robust controllability under frequent interoperability anomalies. At each sampling instant, the controller solves a finite-horizon optimization problem with the objective of minimizing a composite cost:

$$\min_{i_k} J = \sum_{k=1}^N (\alpha_1 (i_k - i_{k-1})^2 + \alpha_2 \Delta V_k^2 + \alpha_3 \Delta T_k^2) \quad (3)$$

where i_k denotes the predicted charging current sequence within the forecast time domain, i_{k-1} represents the actual executed current at the previous time step, ΔV_k indicates the bus voltage deviation, ΔT_k signifies the cell temperature rise increment, and $\alpha_1, \alpha_2,$ and α_3 are weighting coefficients used to coordinate smoothness, voltage stability, and thermal safety objectives. The optimization is subject to constraints on cell voltage, current slope, power capability, and communication status. Using a quadratic programming solver within a rolling horizon of $N = 10$, only the first control input is applied per cycle. On a Cortex-A72 processor, average computation time is 7.8 ms per step. Diagnostic feedback updates constraint boundaries each cycle, maintaining control continuity under current-limiting conditions and protocol disruptions.

4. Safety Diagnosis and Controlled Disconnection Control Mechanism Design

4.1. Design of Safety Diagnosis Criteria During Fast Charging

The safety diagnostic module evaluates multi-source operational states and cumulative risks to support controlled disconnection under interoperability anomalies. A comprehensive risk indicator RRR is computed as:

$$R = \alpha_1 |V_{bus} - V_{ref}| + \alpha_2 |I_{meas} - I_{cmd}| + \alpha_3 (T_{cell} - T_{ref}) + \alpha_4 \phi_{comm} \quad (4)$$

where V_{bus} and V_{ref} are the measured and reference bus voltages, I_{meas}, I_{cmd} denote measured and commanded current, T_{cell} is the cell surface temperature, T_{ref} is the nominal

reference, and ϕ_{comm} is a normalized communication integrity score. The weights α_1 to α_4 are tuned empirically to balance physical and communication risks. Diagnostic logic classifies risk as: normal ($R < T_1$), warning ($T_1 \leq R < T_2$), and critical ($R \geq T_2$). A moving-average window is applied to suppress transient spikes. Based on risk level, the system issues derating or controlled disconnection signals, ensuring safety during thermal accumulation and protocol disruptions [8].

4.2. Controlled Disconnection and Fault Recovery Process Design

To prevent prolonged exposure to thermal runaway or electrical hazard under interoperability anomalies, the fast-charging controller adopts a tiered disconnection strategy based on the real-time risk indicator R and its derivative $\frac{dR}{dt}$. Disconnection is triggered when R exceeds thresholds and its growth rate surpasses defined margins. The control model aims to minimize disruption during disengagement and is formulated as:

$$\min_{\Delta i(t)} \int_{t_0}^{t_d} \left[\beta_1 \left(\frac{di(t)}{dt} \right)^2 + \beta_2 (V_{\text{bus}}(t) - V_{\text{nom}})^2 \right] dt \Delta i(t) \quad (5)$$

where $\Delta i(t)$ represents the current change trajectory during disconnection, $V_{\text{bus}}(t)$ denotes the real-time bus voltage value, V_{nom} is the rated bus voltage, β_1 and β_2 are the weighting factors for adjusting current slope and voltage deviation respectively, and t_d indicates the completion time of disconnection execution. After successful disconnection, the system initiates fault recovery through an adaptive delayed re-entry mechanism. A minimum waiting time of $\tau \in [2.0, 2.5]$ seconds is applied based on fault type. A short pre-charge test verifies bus voltage stability and communication integrity via ISO 15118 'ChargingStatus' messages or fallback logic under DIN 70121. This ensures reliable reconnection, avoids repeated handshake loops, and enhances control loop stability [9].

4.3. Integrated Framework for Overall Control Mechanism

The integrated control mechanism is built on state-driven logic, hierarchical coordination, and safety redundancy. It comprises modules for state monitoring, current scheduling, risk evaluation, disconnection, and recovery. The layered architecture forms a closed-loop system connecting top-level diagnostics, mid-level optimization, and bottom-level execution. As shown in Figure 3, event-triggered and periodic synchronization enable consistent state transitions and fault handling. A state machine governs phase segmentation and dynamically adjusts control boundaries based on derating or interruption signals, supporting proactive suppression and adaptive recovery. Parameter sharing and redundancy ensure uninterrupted control under restarts, packet loss, or device delays, enhancing overall system stability.

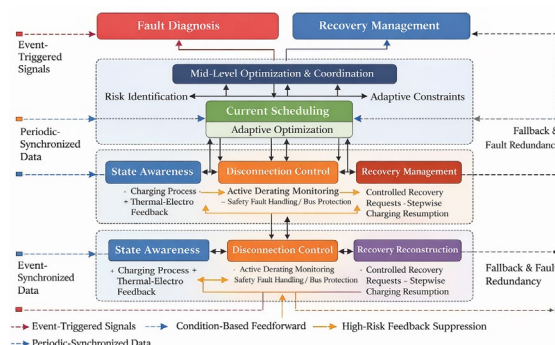


Figure 3. Integrated Framework for Overall Control Mechanism under Charging Interoperability Conditions.

5. Experimental Validation and Results

5.1. Simulation Platform and HIL Test Platform Construction

The verification platform combines a model-driven simulation system with a hardware-in-the-loop (HIL) test setup. The simulation system uses MATLAB/Simulink and Stateflow to model bus loads, cell thermo-electrical behavior, communication protocols, and charging state transitions. The HIL setup, based on dSPACE MicroAutoBox and power amplifiers, emulates high-voltage battery ports, station control signals, and fault events to assess controller response, disconnection logic, and re-entry behavior under interoperability conditions. The platform supports flexible parameter configurations and scripted fault injections, ensuring comprehensive coverage and repeatable experiments.

5.2. Comparative Analysis of Charging Interruption Rates

Statistical analysis of over 3,000 interoperable charging sessions was conducted to assess control strategy stability. As shown in Table 1, the fixed charging curve strategy had a 21.4% interruption rate under packet loss and current-limiting disturbances. The threshold derating strategy reduced this to 17.6%, while the proposed method—combining hierarchical control, diagnostics, and controlled disconnection—further lowered it to 11.1%. These results confirm that structured state management and recoverable current control effectively reduce unplanned interruptions from overshoot, oscillations, and reconnection failures, enhancing stability in complex interoperability scenario.

Table 1. Comparison of Charging Interruption Rates Under Different Control Strategies.

Control Strategy Type	Number of Interruptions	Interruption Rate
Fixed Charging Curve	214	21.4%
Threshold Derating Strategy	176	17.6%
Proposed Control Mechanism	111	11.1%

5.3. Comparative Analysis of Fault Recovery Duration

Recovery efficiency is critical to maintaining charging continuity and user experience after a fault. In tests with 3,000 samples, the fixed charging curve strategy—without recovery logic—averaged 6.5 s due to reconnection delays and repeated handshakes. The threshold derating method improved anomaly handling but still relied on passive reinitialization, averaging 4.3 s with inconsistent results. The proposed approach combines controlled disconnection with fast re-entry using state caching, link monitoring, and pre-charge checks, cutting average recovery time to 2.1 s. Over 80% of sessions recovered within 2.5 s, demonstrating that hierarchical recovery greatly enhances resumption efficiency under communication and voltage disturbance.

5.4. Analysis of Bus Voltage Overshoot Suppression Effect

Bus voltage frequently exhibits dynamic overshoot during charging phase transitions, abrupt command changes, or communication faults. Delayed control can push voltage beyond limits, triggering protection or damaging cells. Overshoot is mainly caused by inadequate current slope control, power response delays, and mismatches in limiting strategies. Analysis of 3,000 fast-charging sessions showed that fixed charging curves resulted in an average overshoot of 41.2 V, peaking at 54.6 V. Threshold-based limiting reduced the average to 28.7 V, though occasional spikes persisted. With controlled disconnection, gradual current recovery, and command smoothing, the overshoot further declined to 22.6 V, achieving approximately 45% suppression and improved voltage stability.

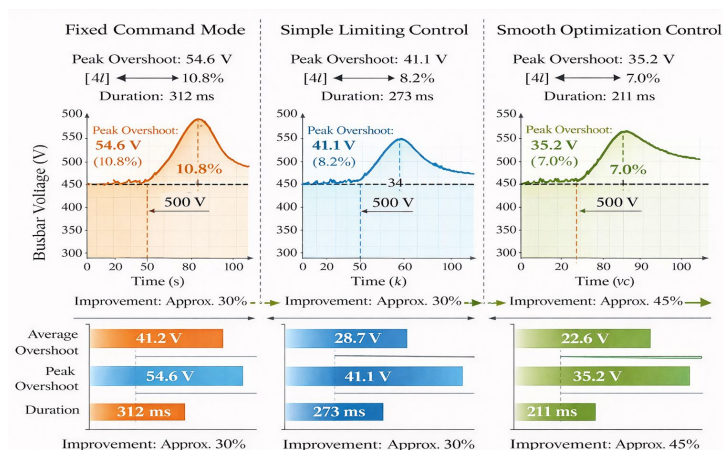


Figure 4. Comparison of Typical Bus Voltage Waveforms.

5.5. Analysis of Cell Temperature Rise Control Effectiveness

High-voltage batteries are susceptible to thermal accumulation during high-current fast charging, particularly under current fluctuations and control instability caused by interoperability anomalies. These conditions heighten the risk of temperature exceeding safe limits and initiating thermal runaway. To evaluate thermal management, data from 3,000 charging sessions were analyzed. As shown in Figure 5, the fixed charging curve resulted in an average temperature rise of 8.7°C, with peaks above 12.5°C and uneven distribution. Threshold-based limiting reduced the average to 6.9°C, though recovery-phase surges remained. With optimized current control, derating, and controlled disconnect-reconnect, the average decreased to 6.1°C, peak values stayed below 11.2°C, and thermal distribution was more uniform.

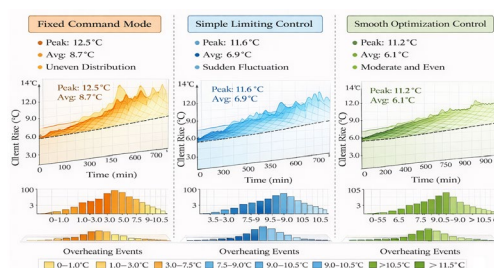


Figure 5. Comparison of Battery Overheating Trends.

5.6. Scalability and Real-World Deployment Considerations

The proposed framework performs well in HIL environments, but real-world charging networks vary widely in protocols, hardware, and conditions. Legacy systems lack standardized re-entry, requiring backward-compatible handshake logic. Extreme temperatures and grid instability can affect thermal and electrical responses, challenging controller robustness. Cyber-physical threats like spoofing or packet injection also threaten diagnostic accuracy and recovery. To enhance applicability, future deployments should integrate adaptive protocol abstraction, temperature-aware constraint tuning, and encrypted communication aligned with ISO 15118, improving fault tolerance and scalability across diverse infrastructures.

6. Conclusions

This work presents a hierarchical control architecture with constraint-optimized current scheduling to enhance safety and stability in high-voltage fast charging under interoperability conditions. It enables real-time anomaly detection, controlled disconnection, and fast fault recovery.

Tested in over 3,000 HIL sessions, the approach cuts interruption rates, recovery time, and voltage/temperature overshoot. However, it does not yet address battery aging or switching fatigue. Future work will integrate degradation models, SoH-adaptive thresholds, secure protocols, and grid-aware feedback to improve real-world robustness.

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