Dynamically Reconfigurable XNOR/IMP Logic Based on Dual-Mechanism Operation in an Electrically Tunable Two-Dimensional Heterojunction

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Article

Dynamically Reconfigurable XNOR/IMP Logic Based on Dual-Mechanism Operation in an Electrically Tunable Two-Dimensional Heterojunction

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Abstract

Reconfigurable logic is crucial for future adaptive computing but are challenging to realize with conventional complementary metal-oxide-semiconductor technology due to the limited field-effect characteristics of the fundamental silicon devices. Two-dimensional materials offer a promising platform, yet enhancing their functional versatility requires novel operational mechanisms. Here, we demonstrate a single WSe_2/h-BN/graphene heterojunction capable of dynamically switching between distinct logic functions—XNOR and IMP—simply by modulating the drain-source voltage. At a low bias of 0.3 V, the carrier distribution is governed by capacitive coupling, realizing an XNOR gate. Increasing the bias to 3 V activates Fowler–Nordheim tunneling between the graphene floating gate and the drain, enabling IMP logic operation. The interplay and voltage-induced transition between these two physical mechanisms underpins the device's multifunctional capability. This work introduces a novel operational strategy for two-dimensional material-based reconfigurable logic, providing a pathway toward compact, adaptive hardware for post-CMOS computing.

Keywords: reconfigurable logic; electrically tunable; Fowler-Nordheim tunnel

1. Introduction

The miniaturization of conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) is approaching its physical limits.[1] To further improve information processing performances, electronic devices based on new physical principles or emerging technologies are required.[2–4] In this context, reconfigurable logic has emerged as a transformative paradigm, offering the ability to dynamically alter circuit functionality within the same hardware footprint.[5–10]Such capability is crucial for adapting to diverse computational tasks, enhancing hardware utilization, and enabling more flexible and compact computing systems, which are central to the development of adaptive electronics, edge computing, and neuromorphic engineering.[11,12]

The advent of two-dimensional (2D) materials has opened new avenues for such innovations.[10] Materials like graphene, transition metal dichalcogenides, and hexagonal boron nitride exhibit exceptional electronic, optical, and mechanical properties, along with atomically thin bodies that enable potent electrostatic control.[13–17] Over the past decade, researches into 2D material-based transistors and logic devices have intensified, demonstrating promising pathway toward more sophisticated, functionally integrated systems.[9,11,18–24]Notably, these include the development of neuromorphic computing components that mimic synaptic and neuronal functions for energy-efficient, brain-inspired hardware;[8,25,26] devices capable of synergistic optoelectronic co-modulation, where optical and electrical inputs interact to define novel operational states;[18,27–32] and architectures that integrate logic and non-volatile memory functions (logic-in-memory)—to

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overcome the von Neumann bottleneck. [33–35]Collectively, these advances underscore a shift from simple electronic switches toward reconfigurable, multi-domain systems with broader application potential. Despite these advances, the versatility of 2D logic devices can be further enhanced by introducing novel operational mechanisms, thereby enabling distinct reconfigurable logic from a single device.

Here, we demonstrate a WSe_2/h-BN/graphene heterostructure that exhibits dynamically reconfigurable multifunctional logic operations (XNOR and IMP), controlled by the polarity combinations of gates and drain voltages. The ambipolar WSe_2 channel is simultaneously modulated by the floating gate and the back gate, where the floating-gate voltage regulates the channel regions on both sides of the electrode, while the back-gate voltage governs the central area of the channel. Under a low source-drain bias (0.3 V), the electrostatic coupling from both the floating gate and the back gate primarily dictates the carrier distribution within the channel, enabling the realization of XNOR logic function. When the source-drain bias is increased (3 V), the operational mechanism moves beyond the established paradigm of capacitive coupling and Fowler–Nordheim tunneling between the floating gate and the drain emerges as an essential and complementary switching mechanism, which allows the device to perform IMP logic. The co-existence and interplay of these two mechanisms underpin the device's multifunctional capability. By introducing a new mechanistic dimension into 2D device operation, this work provides a viable pathway toward more versatile and compact post-CMOS computing hardware.

2. Materials and Methods

A schematic diagram of the heterojunction fabricated on a commercial silicon-on-insulator (SOI) wafer is depicted in Figure 1a, where tungsten diselenide (WSe_2), hexagonal boron nitride (h-BN), and graphene (Gr) flakes serve as the channel layer, tunneling dielectric, and floating gate, respectively. Two graphene floating gates (FG) are placed beneath the source and drain electrodes, respectively, and connected together to serve as input 1 (IN1), with the heavily doped silicon back gate (BG) acting as the input 2 (IN2). Figure 1b shows the optical microscope image of the photodetector, where WSe_2, h-BN, and Gr flakes are indicated by blue, green, and purple dashed lines, respectively. As shown in the figure, the channel length between the source and drain is approximately 6.5 μm. The Raman spectroscopy of the Gr flakes, h-BN flakes, h-BN/Gr heterostructure, and WSe_2/h-BN/Gr heterostructure are depicted in Figure 1c. The WSe_2 flakes exhibit one characteristic peak at 254 cm^{-1}, corresponding to the out-of-plane (A_{1g}) vibrational modes. The characteristic peak of h-BN is located at 1366 cm^{-1}, corresponding to the in-plane (E_{2g}) vibrational mode. Furthermore, the peaks at 1578 cm^{-1} (*G*) and 2705 cm^{-1} (2*D*) are two typical characteristic peaks of multi-layer graphene. The cross-sectional TEM image and energy-dispersive spectrometry (EDS) of WSe_2/h-BN/Gr heterostructure beneath the source electrode is obtained and the results are shown in Figure 1d. The boundary of h-BN/Gr and WSe_2/h-BN interfaces can be clearly resolved, and the thicknesses of WSe_2, h-BN, and Gr flakes is identified to be 1.1, 11.5 and 1.5 nm, respectively, in good accordance with the atomic force microscopy (AFM) results in Figure 1e.

The heterostructure was constructed with standard dry transfer method. The commercial SiO_2/Si substrate (285 nm oxide thickness) first underwent a standard cleaning procedure. It was immersed sequentially in acetone, isopropanol (IPA), and deionized (DI) water, followed by drying with a nitrogen stream to obtain an atomically clean surface. Subsequently, flakes of multilayer graphene, h-BN, and WSe_2 were transferred onto the pre-cleaned SiO_2 surface via mechanical exfoliation. The PC adhesion layer can pick up 2D materials at ~90 ℃ and release at ~180 ℃ and the WSe_2, h-BN flakes were sequentially picked up by this polymer and finally released onto the graphene flake on the SiO_2/Si substrate.[36] The remaining polycarbonate (PC) was dissolved in a chloroform ($CHCl_3$) bath for two minutes. Subsequently, the device was annealed at 300 °C under vacuum for three hours to improve interfacial contact and release residual stress within the heterostructure. Finally, electrodes were defined via standard electron-beam lithography (EBL) and deposited by electron-beam evaporation of Cr/Au (5/50 nm).

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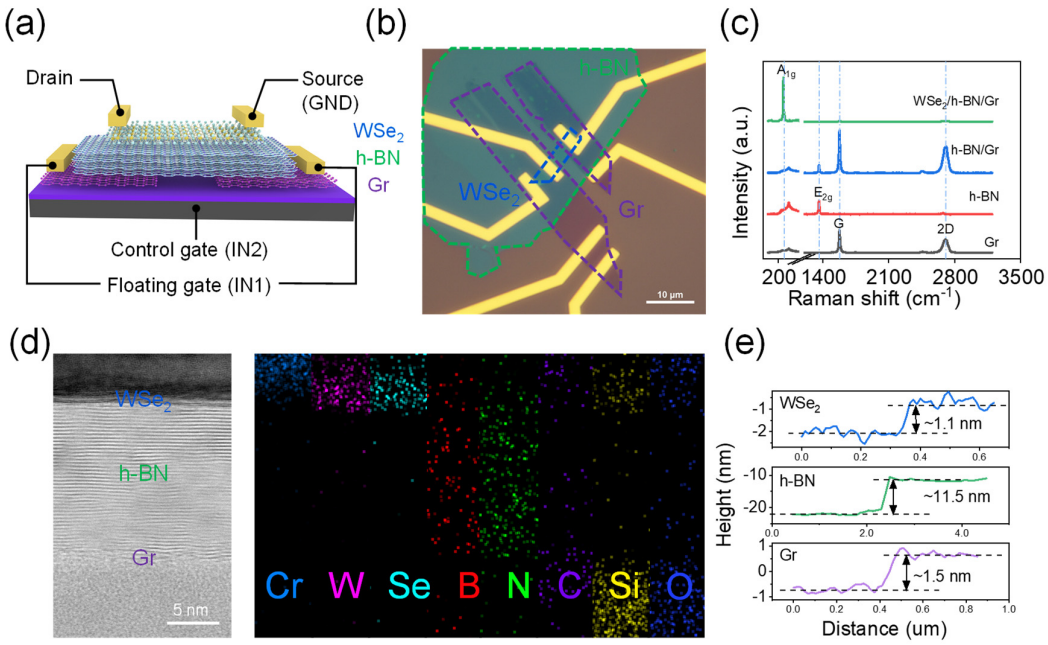

Figure 1. Schematic illustration of the WSe_2/h-BN/Gr heterojunction. (**a**) Schematic diagram of the WSe_2/h-BN/Gr heterojunction and the corresponding circuit configuration; (**b**) Optical microscope image of the fabricated WSe_2/h-BN/Gr heterojunction; (**c**) Raman spectroscopy of the Gr flakes, h-BN flakes, h-BN/Gr heterostructure, and WSe_2/h-BN/Gr heterostructure; (**d**) Cross-sectional TEM image and corresponding energy-dispersive spectrometry (EDS) of WSe_2/h-BN/Gr heterostructure beneath the source electrode; (**e**) The atomic force microscopy (AFM) results of WSe_2, h-BN, and Gr flakes.

3. Results and Discussions

The electrical properties of WSe_2 layer were firstly characterized by I-V and transfer curve measurements. Figure 2a presents the I-V characteristics of WSe_2/h-BN/Gr heterostructure under various floating-gate voltages. (Schematic of the measurement circuit for Figure 2a-c is illustrated in Figure S1.) The curves maintain a linear relationship even with increasing gate bias, indicating excellent ohmic contact between the two-dimensional (2D) materials and the electrodes. Figure 2b shows the transfer curve of WSe_2 at a source-drain voltage of 0.3 V under floating-gate modulation. The curve exhibits ambipolar behavior with a high on/off ratio of up to 10^6, demonstrating effective control of WSe_2 by the floating gate. Figure 2c shows the transfer curve of WSe_2 under back-gate modulation and the curve exhibits a clear hysteresis window resulting from the charge trapping and release in the floating gate.[37,38] Overall, the WSe_2 demonstrates effective and independent modulation by both the floating gate and the back gate. Besides, the WSe_2 channel exhibits clear ambipolar conduction and the maximum on-state current occurs at a floating-gate voltage of 8 V (back-gate voltage of 30 V) for electron-dominated conduction and -8 V (back-gate voltage of -60 V) for hole-dominated conduction.

As shown in Figure 1a, the device's channel is electrostatically controlled by both the floating gate and the back gate, with the FG dominating near the electric contacts and the BG in the mid-channel. High conduction is achieved only when both gates accumulate carriers of the same type (both electrons or holes). When both gates bias the channel toward electron/hole accumulation, a uniform conductive path forms, turning the device on. Conversely, a mismatch in carrier type—where one gate induces electron conduction and the other induces hole conduction—creates a potential barrier or carrier depletion in the channel, thus leading to a significantly reduced drain current. Figure 2d,g present the I-V characteristics measured at a floating-gate voltage of 8 V/-8 V, with the back-gate voltage set to 30 V and -60 V. Similarly, Figure 2e,h demonstrate the I-V

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characteristics under a constant BG voltage of 30 V (-60 V), with the FG voltage set to 8 V and -8 V. A key observation from the figures is that the channel current is significantly larger when the floating-gate and back-gate voltages have the same polarity, compared to when they have opposite polarities. The source-drain current with V_{FG} = 8 V (-8 V) and V_{BG} = 30 V (-60 V) is substantially higher than that with V_{FG} = 8 V (-8 V) and V_{BG} = -60 V (30 V), highlighting the critical role of gate voltage alignment.

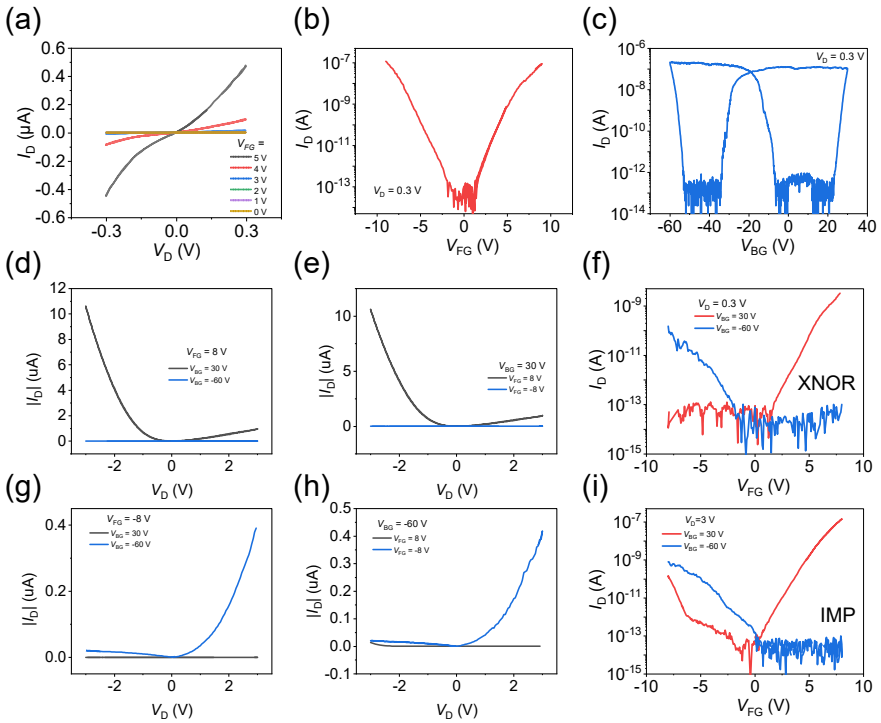

Figure 2. Transport properties of the device. (**a**) Output curves under various floating-gate voltage; (**b**) Transfer curves under the modulation of floating gate at 0.3 V bias; (**c**) Transfer curves under the modulation of back gate at 0.3 V bias; (**d**), (**g**) IV curves with floating gate at 8/-8 V and back gates at 30 V and -60 V; (**e**), (**h**) IV Curves with back gate at 30/-60 V and floating gates at 8 V and -8 V; (**f**) Transfer curves under the modulation of floating gate at 0.3 V bias and back gates at 30 V and -60 V; (**i**) Transfer curves under the modulation of floating gate at 3 V bias and back gates at 30 V and -60 V.

Furthermore, the drain current increases with the applied source-drain voltage, as expected. Figure 2f,i present the corresponding transfer curves measured at source-drain voltages of 0.3 V and 3 V, respectively. At V_D = 0.3 V, the transfer curve exhibits n-type semiconductor behavior when V_{BG} = 30 V, while exhibits p-type behavior when V_{BG} = -60 V. This indicates that back-gate voltage determines the type of majority carrier induced in the channel layer. By applying floating-gate voltage and back-gate voltage as inputs, the device can be configured to function as a XNOR logic gate. In contrast, at V_D = 3 V, a distinct ambipolar behavior is observed in the transfer characteristics when V_{BG} = 30 V, while the transfer curve maintains p-type behavior when V_{BG} = -60 V. The underlying mechanism for this ambipolar behavior is the strengthening electric field between the floating gate and the drain with increasing drain bias. This enhanced field gives electrons a higher probability of tunneling from the floating gate to the drain, thereby inducing n-type characteristics in the channel region near the drain, similar to the central region.[39] By utilizing the electron tunneling effect, the device can be configured to function as IMP logic gate, with floating-gate voltage and back-gate voltage as inputs.

To elucidate the reconfigurable logic functionality of the device, we investigate its operating mechanism by examining the charge carrier distribution and energy band structure. The charge

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carrier distribution through the WSe_2 channel is jointly modulated by the silicon back gate (V_{BG}), the graphene floating gate (V_{FG}), and the drain-source bias (V_D). We take the device under a small V_D (0.3 V) as a detailed example to illustrate how floating-gate voltage (IN1) and back-gate voltage (IN2) affect the charge carrier distribution. As shown in Figure 3a, When the V_{FG} and V_{BG} are set to -8 V and -60 V ((IN1,IN2) = (-8 V,-60 V)), a negative voltage applied to the floating gate induces hole accumulation in the channel regions near the source and drain electrodes due to electrostatic induction. Similarly, a negative voltage applied to the back gate leads to hole accumulation in the central region of the channel. (Due to electrostatic screening from the floating gate, the back-gate capacitive coupling effect is largely restricted to the central part of the channel.) Consequently, the entire channel exhibits p-type conduction behavior. Conversely, when the V_{FG} and V_{BG} are set to -8 V and 30 V ((IN1,IN2) = (-8 V,30 V)), the negative floating-gate voltage still causes hole accumulation near the electrodes, while the positive back-gate voltage induces electron accumulation in the middle section of the channel. This results in a p-n-p configuration across the channel. The formation of the central electron-potential well significantly suppresses the source-drain current. The charge distributions for the remaining cases, derived from the same analysis, are also presented in the figure. The results demonstrate that the channel conduction is uniformly n-type (when (IN1,IN2) = (8 V,30 V)) or p-type (when (IN1,IN2) = (-8 V,-60 V)) when the floating-gate and back-gate voltages share the same-polarity, whereas opposite polarities induce either an electron ((IN1,IN2) = (-8 V,30 V)) or hole ((IN1,IN2) = (8 V,-60 V))potential well, leading to a significantly suppressed source-drain current. This observation is fully consistent with the transport properties presented earlier.

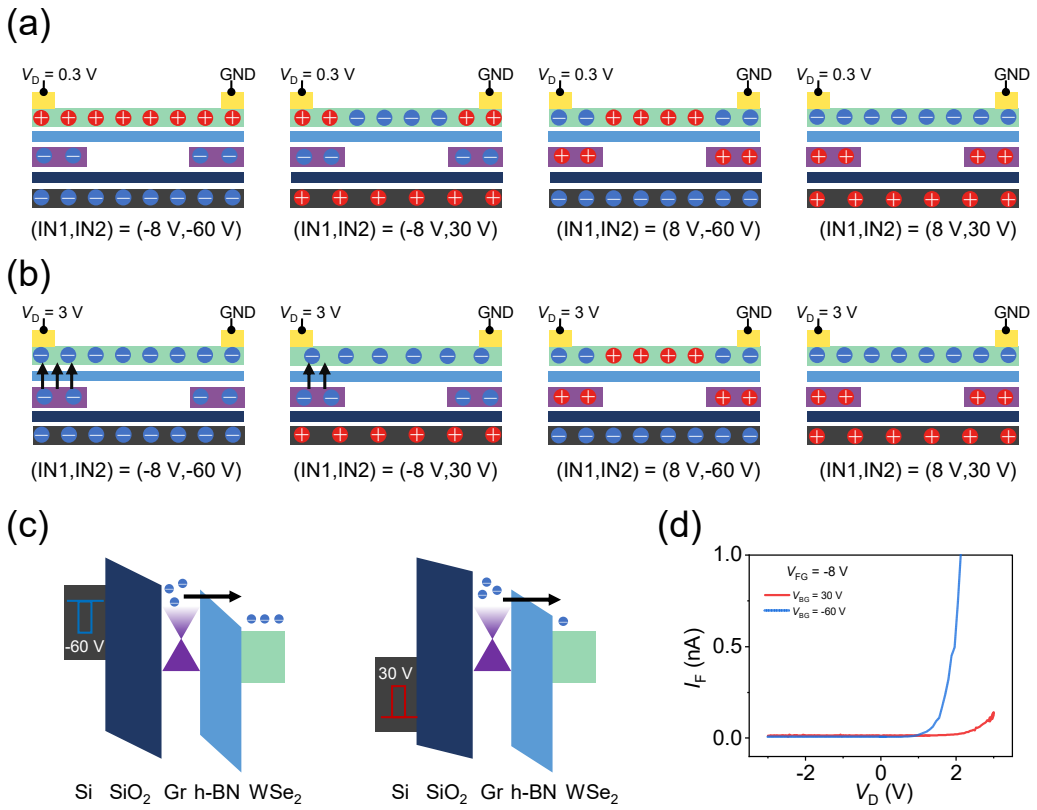

Figure 3. Working principle of the reconfigurable logic device. (**a**), (**b**) Schematic illustration of charge carrier distribution at 0.3 V and 3 V bias, respectively. The red circles represent holes, and blue circles represent electrons. From top to bottom, the device is structured as WSe_2, h-BN, Gr, SiO_2, and Si. The solid arrow indicates the direction of electron injection; (**c**) Energy band diagram for electron tunnelling at -60 V and 30 V back-gate voltage; The floating-gate voltage is -8 V and the V_D is 3 V; (**d**) Tunneling current as a function of V_D with the floating-gate voltage set to -8 V and back-gate voltage set to -60 V/30 V.

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When the drain-source voltage is set to 3 V (Figure 3b), the device behavior differs under a floating-gate voltage of -8 V. At V_D = 3 V and V_{FG} = -8 V, the electric field across h-BN becomes sufficiently strong to induce tunneling. Consequently, the floating gate modulates the channel carrier distribution predominantly through direct charge injection instead of capacitive coupling. Figure 3c presents the energy band diagrams of the device under a source-drain voltage of 3 V and a floating-gate voltage of -8 V, with the back-gate voltage set to -60 V and 30 V, respectively. A back-gate voltage of -60 V generates a stronger electric field in h-BN tunneling layer, leading to more pronounced band bending. This stronger band bending facilitates greater electron tunneling into the channel. In contrast, at V_{BG} = 30 V, the electric field induced by the back gate in h-BN opposes that of the floating gate, thereby partially canceling the overall field and resulting in weaker band bending and thus less electron tunneling. The corresponding tunneling currents are quantified in Figure 3d measured at V_{FG} = -8 V for V_{BG} = 30 V/-60 V. It is evident that the tunneling current at V_{BG} = -60 V is significantly larger than that for V_{BG} = 30 V. This experimental result directly corroborates the theoretical analysis presented above.

To gain deeper insight into the mechanism of electron tunneling, Figure 4a presents the tunneling current versus voltage characteristics for WSe_2/h-BN/Gr heterostructure, with the corresponding test setup shown in Figure S2. As observed, the tunneling current remains low at small floating-gate voltages. When the voltage exceeds a certain threshold, the current exhibits a sharp exponential increase. This behavior is attributed to a transition in the tunneling mechanism: direct tunneling (DT) dominates at lower voltages, while Fowler-Nordheim tunneling (FNT) becomes operative above the threshold voltage. The relationship between current density (J) and electric field (E) for direct tunneling and FN tunneling are given below:

$$J_{\mathrm{DT}} = A \exp\left[\beta E_{\mathrm{DT}}^{\frac{1}{2}}\right] \quad (1)$$

$$J_{\mathrm{FNT}} = A E_{\mathrm{FNT}}^{2} \exp\left[\frac{-B}{E_{FNT}}\right] \quad (2)$$

where A and B are constants.[40,41] It can be derived from the equations that for direct tunneling: $\ln(I_{\mathrm{DT}}) \propto \sqrt{V_{\mathrm{DT}}}$ and for Fowler-Nordheim tunneling: $\ln(\frac{I_{\mathrm{FNT}}}{V_{\mathrm{FNT}}^2}) \propto \frac{-1}{V_{\mathrm{FNT}}}$. Figure 4b,c presents the plots of $\ln(\frac{I_{\mathrm{F}}}{V_{\mathrm{FG}}^2})$ versus $\frac{-1}{V_{\mathrm{FG}}}$ for backward and forward sweeps of the floating-gate voltage. Figure S3 presents the plots of $\ln(I_{\mathrm{F}})$ versus $\sqrt{|V_{\mathrm{FG}}|}$ for backward and forward sweeps of the floating-gate voltage. From these curves, the threshold voltages for FNT are extracted to be approximately 9 V (forward sweep) and -8 V (reverse sweep), respectively. This asymmetry stems from the difference in the energy barriers that carriers must overcome: during the forward sweep, the primary barrier is at the Gr/h-BN interface, whereas during the reverse sweep, it is at the WSe_2/h-BN interface. The distinct heights of these two interfaces account for the observed difference in threshold voltages. Since a lower threshold voltage is required for tunneling in the negative FG direction, our work employs a drain voltage of 3 V combined with an FG voltage of -8 V to implement the IMP logic function, rather than using a drain voltage of -3 V with an FG voltage of 8 V.

Figure 4d shows the source-drain current as a function of the FG voltage under different source-drain biases, with the back gate grounded. It clearly demonstrates that a higher V_D lowers the FG voltage needed to trigger FNT. Notably, the current remains minimal before FNT occurs, because the capacitive coupling effect dominates at the carrier redistribution process. By exploiting the transition of the dominant operating mechanism between capacitive coupling and electron tunneling, the reconfigurable logic functions of XNOR and IMP are achieved and the corresponding truth table is presented in Figure 4e. Here, −8 V and 8 V are used to represent the logic 0 and 1 for IN1 and −60 V and 30 V are used to represent the logic 0 and 1 for IN2. The logic output is defined by the channel current and a logic output of "1" is defined as a current greater than 10^{-11} A, while a logic "0" corresponds to a current less than 10^{-11} A. Figure 4f displays the output currents measured under different combinations of input logic for XNOR and IMP logic. As can be seen from the figure, the device operates as a XNOR logic gate at V_D = 0.3 V, and as a IMP logic gate at V_D = 3 V. Therefore, the logic function can be switched simply by adjusting the source-drain voltage.

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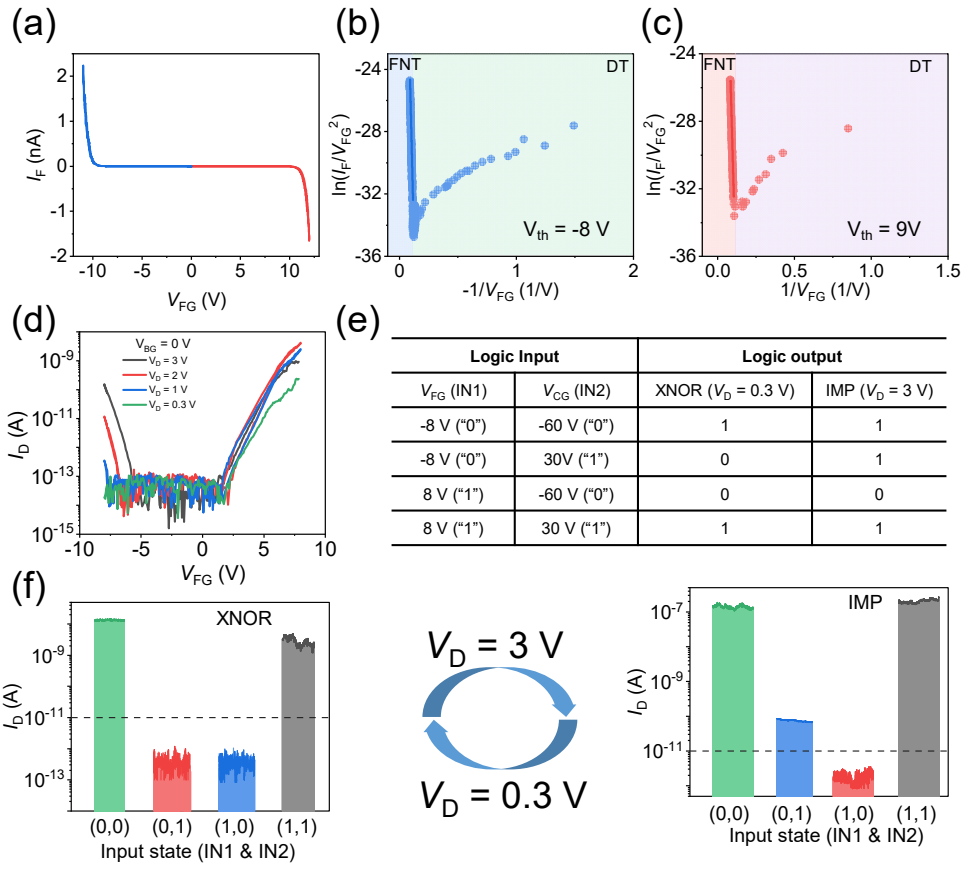

Logic Input		Logic output	
V_{FG} (IN1)	V_{CG} (IN2)	XNOR (V_D = 0.3 V)	IMP (V_D = 3 V)
-8 V (“0”)	-60 V (“0”)	1	1
-8 V (“0”)	30V (“1”)	0	1
8 V (“1”)	-60 V (“0”)	0	0
8 V (“1”)	30 V (“1”)	1	1

Figure 4. Reconfigurable logic gate operation between XNOR and IMP. (**a**) Current-voltage (I-V) tunneling characteristics for WSe_2/h-BN/Gr heterostructure; (**b**), (**c**) The $\ln(I_F/V^2_{FG})$ versus $1/V_{FG}$ curves under negative and positive floating-gate voltages; (**d**) Transfer curves under the modulation of floating gate at various V_D; (**e**) Truth table for the reconfigurable logic gates XNOR and IMP; (**f**) Transition between XNOR and IMP logic gates.

4. Conclusions

In summary, we have demonstrated a dynamically reconfigurable logic device based on WSe_2/h-BN/Gr heterostructure. The carrier distribution in the bipolar WSe_2 channel is simultaneously controlled by the floating-gate voltage, back-gate voltage and the source-drain voltage, where the floating-gate voltage regulates the channel regions on both sides of the electrode, while the back-gate voltage governs the central area of the channel. Under a small source-drain voltage, the channel carrier distribution is primarily governed by electrostatic modulation induced by the floating gate and the back gate, thereby achieving XNOR logic. As the source-drain voltage increases, Fowler-Nordheim tunneling between the floating gate and the drain electrode, coupled with significant capacitive coupling, becomes the dominant operational mechanism, enabling the device to execute IMP logic. The developed two-dimensional reconfigurable heterojunction offers a promising pathway toward compact, multi-functional logic elements with simplified operational control, providing a tangible advantage for future adaptive electronic systems.

Supplementary Materials: The following supporting information can be downloaded at: Preprints.org.

Author Contributions: Conceptualization, Y.H.; methodology, Y.H.; investigation, Y.H.; resources, Z.Z.; data curation, Y.H.; writing—original draft preparation, Y.H.; writing—review and editing, Y.H. and Z.Z; visualization, Y.H.; supervision, Z.Z.; project administration, Z.Z.; funding acquisition, Z.Z. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest.

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