Review

Is GaN the Enabler of High Power Density Converters? An Overview of the Technology, Devices, Circuits, and Applications

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Article

Is GaN the Enabler of High Power Density Converters? An Overview of the Technology, Devices, Circuits, and Applications

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Abstract: The growing demand for electric vehicles, renewable energy, and portable electronics has increased the prevalence of power conversion systems, as exemplified by the architecture of electric automobiles. While silicon devices and circuits are widespread due to their cost-effectiveness, and structures such as the superjunction MOSFET have helped maintain its competitiveness in power applications, the technology remains fundamentally limited by its physical properties. Research and development in semiconductor technologies aim to reduce system size and improve power efficiency in these applications. The Gallium Nitride wide-bandgap semiconductor, with its critical electric field of 3.75 $\frac{MV}{cm}$, which is 12.5 times higher than that of silicon, has emerged as a strong candidate to meet these demands. This paper reviews key milestones of GaN technology; covering devices, compact modeling, packaging, circuit design, and converter implementation; highlighting its suitability for power electronics. For example, a monolithically integrated GaN Buck converter employing soft-switching achieves a peak efficiency of 95.4% when stepping down from 250V to 150V. In the case of a synchronous boost converter using discrete GaN transistors, delivered power can be increased by 37.5% while maintaining an efficiency of 99%. Additionally, GaN has enabled new converter topologies, achieving a power density of 123.3kW/L and an efficiency of 90.9%.

Keywords: comparison; converter; dc-dc; gallium; GaN; HEMT; hybrid; model; monolithic; nitride; overview; packaging; power; stage; transistor; wide-bandgap

1. Introduction

Power electronics (PE) has become one of the leading fields in engineering, driven by the ongoing digitization and electrification of modern infrastructure. Power conversion systems (PCS) are found in a wide range of applications, including server farms [1], electric vehicles [2], portable devices, household appliances, and renewable energy systems [3]. The growth of this field is fueled by the demand for higher energy efficiency, reduced system size, and the emergence of new technologies and topologies, such as [4] and [5].

To illustrate the widespread use of power conversion systems, Figure 1 presents the architecture of a fully electric vehicle. In this type of vehicle, two batteries are used: a high-voltage (HV) battery that powers the traction motors, and a low-voltage (LV) battery from which various lower-voltage power buses are derived. The system includes an onboard battery charger (OBC) that enables external charging of the HV battery by converting the grid's AC voltage into the required HV DC voltage. The LV battery is charged from the HV battery via a DC-DC converter.

As shown in Figure 1, multiple vehicle subsystems are powered from the LV voltage rail. These include body electronics (BE), infotainment systems (INFO), and Advanced Driver Assistance Systems (ADAS). Each of these subsystems may use the LV supply bus to generate their specific required voltages. The electric traction motor is driven by an inverter that converts HV DC power into a three-phase AC voltage. This power architecture clearly demonstrates that numerous power conversions

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are necessary within such a complex system, with the majority being implemented using various topologies of switching converters (SC).

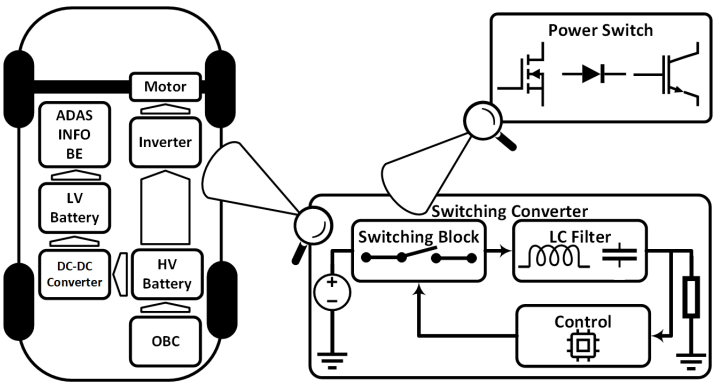

Figure 1. Power architecture, from system to semiconducting device

The lower right side of Figure 1 shows a block diagram of a switching converter (SC). Its main functional components are the control circuit, the switching block (SB), and the output LC filter composed of reactive elements [6]. Among these, the switching block has the most significant impact on the system's overall efficiency. At its core is the power switch (PS), whose primary role is to transfer power from the source to the load. It operates in cycles, alternating between on and off states, driven by square-wave pulse signals generated by the control circuit.

An ideal PS turns on and off instantaneously, exhibits zero resistance when conducting, and blocks any voltage when turned off. In practice, however, PS devices are implemented using semiconductors that introduce several non-idealities, such as conduction resistance (R_{on}), finite switching time, limited drain-to-source breakdown voltage (BV), and, in the case of diodes, a non-zero forward voltage drop [6]. These deviations from ideal behavior result in power losses within the PCS, reducing overall efficiency. Additionally, limitations such as low BV and slow switching speed can restrict the range of applications for a given semiconductor device.

While silicon (Si) is the most commonly used material for power devices, other semiconductors have also been explored. Gallium Arsenide (GaAs) is widely used in the radio frequency (RF) field [7], but it is not suitable for power applications due to its relatively low thermal conductivity of $0.5\frac{W}{cm \cdot K}$ compared to Si's $1.5\frac{W}{cm \cdot K}$. At present, the primary commercial competitors for the PS role are Silicon Carbide (SiC) and Gallium Nitride (GaN), which are wide bandgap (WBG) semiconductors. These materials exhibit approximately $8.3\times$ and $12.5\times$ higher critical electric fields, respectively, enabling devices that can withstand higher BVs in the same or even smaller areas than Si based devices. Furthermore, the reduced area leads to lower parasitic capacitances, which in turn enable higher switching frequencies. At the system level, this allows for the use of smaller inductors and capacitors [8].

This work extends [9] and has the purpose to highlight the widespread use of PCSs and how their performance and implementation are influenced by the semiconductor technologies and device structures employed. Although several semiconducting materials are presented and compared; including Si, GaAs, SiC, and ultra-wide bandgap (UWBG) materials such as Aluminum Nitride (AlN) and β-Gallium Oxide (β-Ga_2O_3); the primary focus is on GaN technology. This material is explored in detail by synthesizing the performance data of various reported power transistors, emphasizing key advantages such as higher BVs in smaller device areas, switching frequencies exceeding 500 kHz, and improved current conduction enabled by $\approx 1.5\times$ higher electron mobility compared to Si.

Based on our evaluation of multiple GaN and Si power stage integrated circuits (ICs), the monolithic integration of PSs and drivers opens the path to high-efficiency, low-footprint PCSs. The use of GaN transistors over their Si counterparts can increase the delivered power by 37.5% while raising the efficiency from 97% to 99% in the case of a synchronous boost converter [10]. Furthermore, this

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technology can enable new converter topologies, such as a Hybrid point-of-load (POL) converter that achieves a power density of 123.3 kW/L with an efficiency of 90.9% [11].

The remainder of this paper is organized as follows. Section 2 presents several semiconductor technologies in the context of power applications, emphasizing the physical characteristics that make them suitable for this field. Section 3 focuses on GaN technology, detailing the types of devices fabricated in this process, the simulation model developed for the lateral device, and packaging solutions for emerging technologies. In Section 4, GaN monolithic circuit design is explored, addressing both digital and analog design challenges and summarizing the performance of various circuits. Section 5 highlights the efficiency improvements achieved through GaN devices and introduces converter topologies enabled by this technology. Finally, Section 6 concludes the paper.

2. Semiconductor Technologies for Power Conversion Applications

The application's power rating and switching frequency dictate the choice of semiconductor device [12], as illustrated in Figure 2. For high power applications, Si thyristors are commonly used. In the medium to high power range, insulated-gate bipolar transistors (IGBTs) were traditionally the preferred choice. However, with the advent of SiC MOSFETs, the two technologies are now in competition. SiC MOSFETs offer several advantages, including an intrinsic body diode, whereas IGBTs require an external freewheeling diode on the printed circuit board (PCB) or integrated at package level. Additionally, SiC devices support higher switching frequencies than IGBTs [13].

For low to medium PCSs, Si MOSFETs compete with both SiC MOSFETs and GaN High Electron Mobility Transistors (HEMTs). These wide-bandgap devices offer superior performance in terms of voltage-blocking capabilities and switching speed, typically in smaller packages. SiC MOSFETs are favored for their higher BV and thermal conductivity, while GaN HEMTs are preferred for their fast switching capabilities [14].

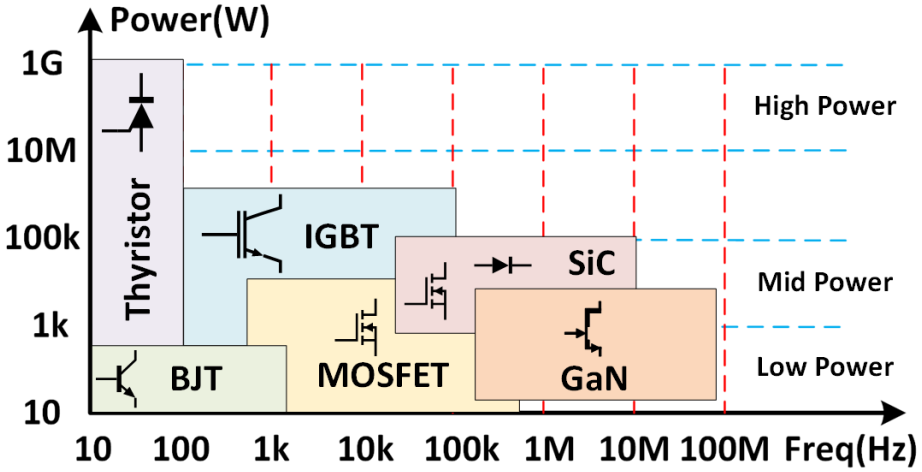

Figure 2. Device distribution across different power levels

The feasibility of using emerging WBG semiconductors as PSs stems from their superior physical properties. These materials offer higher critical electric fields, wider bandgaps, greater thermal conductivity, and improved electron mobility. A summary of the physical characteristics of various semiconductor materials is presented in Table 1 [7,15–18] with key parameters including band gap (E_g), dielectric constant (ϵ_r), carrier mobility (μ_n), critical electric field (E_c), electron saturation velocity (v_s), and thermal conductivity (k).

GaAs offers a higher μ_n of $8.500\frac{cm^2}{V \cdot s}$ compared to Si's $1.350\frac{cm^2}{V \cdot s}$, making it a preferred material for high-frequency applications such as optical switches and RF devices [7]. However, its low k of $0.5\frac{W}{cm \cdot K}$ limits its suitability for power applications. SiC, by contrast, is well-suited for high-power and high-voltage applications due to its $\approx 10\times$ higher thermal conductivity compared to GaAs and about $8\times$ higher E_c than Si. It also serves as a suitable substrate for GaN devices [7]. GaN surpasses

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all the aforementioned materials in terms of E_g and E_c, while also exhibiting higher electron mobility than both Si and SiC. As a result, GaN based devices are widely adopted alongside SiC devices in commercial PCS due to their technological maturity and performance [19].

For future power devices, UWBG materials such as AlN, $\beta - Ga_2O_3$, and diamond are currently under research [15–18,20]. As shown in Table 1, $\beta - Ga_2O_3$ offers promising characteristics compared to GaN, including an $\approx 2.1\times$ higher E_c and $\approx 1.4\times$ higher E_g, which could enable devices with even higher BVs in the future. AlN stands out with the highest E_c of 15.9 $\frac{MV}{cm}$ among the listed materials, along with a high k of 3.21 $\frac{W}{cm \cdot K}$, surpassed only by SiC and diamond. Among all presented semiconductors, diamond exhibits the best properties, with a $\approx 3.5\times$ higher μ_n, $\approx 2.7\times$ higher E_c, and about $\approx 18.7\times$ higher k compared to GaN. The remainder of this article will focus on developments based on GaN semiconductor technology.

Table 1. Semiconductors properties

Material	E_g (eV)	ϵ_r	μ_n $\left(\frac{cm^2}{V \cdot s}\right)$	E_c $\left(\frac{MV}{cm}\right)$	v_s $\left(\frac{cm}{s}\right)$	k $\left(\frac{W}{cm \cdot K}\right)$
Si	1.12	11.7	1350	0.3	$1 \cdot 10^7$	1.5
GaAs	1.42	12.9	8500	0.4	$2 \cdot 10^7$	0.5
4H-SiC	3.23	9.66	900	2.5	$1.9 \cdot 10^7$	4.9
GaN	3.39	8.9	1265*	3.75	$2.5 \cdot 10^7$	1.3
$\beta - Ga_2O_3$	4.9	10	300	8	$1.5 \cdot 10^7$	0.23**
Diamond	5.47	5.7	4500	10	$2 \cdot 10^7$	24
AlN	6.1	8.5	500	15.9	$2 \cdot 10^7$	3.21

Notes: *1265 $\frac{cm^2}{V \cdot s}$ in bulk, 2000 $\frac{cm^2}{V \cdot s}$ in 2DEG
**0.23 for [010] and 0.13 for [100]

3. GaN Technology

This chapter provides insight into the development of the standard GaN transistor structure and compares various lateral and vertical device implementations. It also covers specific aspects such as the industry-standard simulation model for this transistor and the packaging methods commonly used for these power devices.

3.1. GaN Devices

The first GaN transistors utilized a lateral Metal-Insulator-Semiconductor High Electron Mobility Transistor (MIS-HEMT) structure, as shown in Figure 3 a). In this implementation, a dielectric layer is inserted between the gate and the two-dimensional electron gas (2DEG) formed at the GaN - AlGaN heterojunction, resulting in a depletion-mode (d-mode) device. In such devices, the channel conducts by default, and electron flow can only be interrupted by applying a negative gate voltage, which repels charge carriers from the channel. Although these transistors offered performance advantages over their Si counterparts, their normally-on behavior was considered unsuitable for PE applications due to safety and control concerns. An early commercial solution to this limitation was the GaN-Si cascode structure, which combined a low-voltage Si MOSFET with a high-voltage GaN d-mode HEMT to create a normally-off, enhancement-mode (e-mode) configuration [10]. This approach also allowed for the integration of features such as gate driving and protection circuitry within the Si circuit [21].

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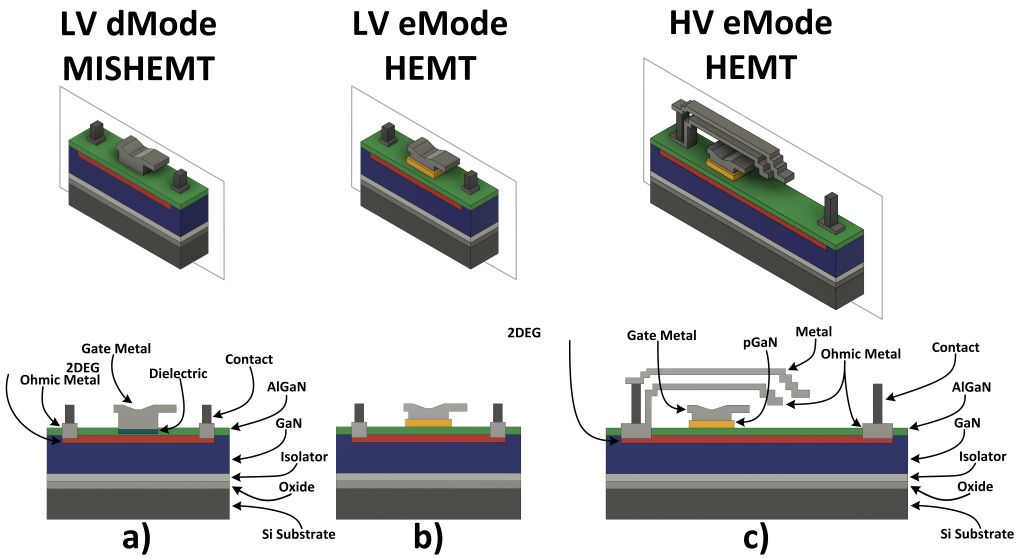

Figure 3. GaN devices: a)MIS-HEMT b)LV pGaN gate HEMT c)HV pGaN gate HEMT

To eliminate the need for additional components, various device-level modifications have been explored to create e-mode HEMTs. The most widely adopted solution is shown in Figure 3 b), where a p-doped GaN layer is introduced beneath the gate. This forms a reverse-biased Schottky junction, which creates a depletion region that suppresses the 2DEG channel under zero gate bias, thereby achieving normally-off behavior. To reach BVs in the range of 200V to 650V, a HV variant of the device is employed, as depicted in Figure 3 c). In this version, the drain region is extended, and field plates are added to redistribute the electric field away from the gate. Another approach to developing devices that leverage the advantages of GaN semiconducting material while exhibiting higher BVs, currents, and reliability than HEMTs is the use of vertical structures such as [22] and [23].

A milestone in GaN device development is the realization of the dual-gate bidirectional switch (BDS) [24]. This device operates in four modes: it blocks current when both gates are unbiased, functions as a switch when both gates are biased, and acts as a rectifier when only one gate is biased (true for either gate). BDSs are especially useful in SCs such as matrix converters, an AC-AC converter topology that eliminates the need for a DC-link capacitor. Traditionally, the switches in these topologies are implemented using two anti-series connected devices, such as MOSFETs or IGBTs. The GaN BDS offers advantages such as reduced cost, area, and R_{on}, by utilizing a shared drift region. This innovation has already reached commercial availability [25].

An initial obstacle that hindered the widespread adoption of GaN devices was the difficulty of growing large GaN crystals suitable for wafer production [7]. The high cost associated with native GaN substrates led to the use of alternative materials such as Si, sapphire, and SiC. Among these, Si is the most cost-effective option, SiC offers improved thermal conductivity at a higher cost, and sapphire is typically used in RF and optoelectronic applications of GaN devices. Recently, a technological breakthrough enabled the production of 300mm wafers, a development that is expected to reduce GaN device prices in the long term [26].

Table 2 synthesizes multiple reported lateral and vertical devices. This GaN fin FET [23] offers $\approx 24\times$ more current conduction per area and $81\times$ lower on-resistance compared to the Current Aperture Vertical Electron Transistor (CAVET) reported in [22], while also reducing production cost by eliminating the need for epitaxial regrowth. The transistor reported in [27] exhibits the highest BV voltage among the lateral devices but also an undesirably low threshold voltage of 0.64V and $\approx 11\times$ higher R_{on} than the other works presented. Both [28] and [29] HEMTs have very low R_{on} values of $0.62m\Omega \cdot cm^2$ and $0.8m\Omega \cdot cm^2$, respectively. The device in [28] has the advantage of a high BV of 1000 V but suffers from low current conduction. In contrast, the device presented in [29] has a BV of 420 V and boasts the highest current conduction among the HEMTs, reaching 0.86 A/mm. Although [22] has

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demonstrated the possibility of co-integrating HEMTs and CAVETs, the lateral device structure is still preferred for GaN monolithic circuit design.

Table 2. Devices Comparison

Param. \ Work	[23](V)	[22](V)	[27](L)	[28](L)	[29](L)
Type	Fin	CAVET	HEMT	HEMT	MIS-HEMT
Substrate	GaN	GaN	Si	SiC	SiC
$Threshold[V]$	1	-2.8	0.64	1.8	3
$R_{ON} \cdot A[m\Omega \cdot cm^2]$	0.2	16.2	9	0.62	0.8
$V_{BR}[V]$	1200	201	1200	1000	420
$I_{DS}[*]$	25	1.08	0.18	0.35	0.86

Notes: L-Lateral, V-Vertical,*kA/cm^2 for V, A/mm for L

3.2. GaN HEMT Model

Due to the structure of GaN transistors and the material-specific properties of GaN technology, standard SPICE models are inadequate for accurately capturing device behavior. To address this limitation, a physics-based compact model, known as the MIT Virtual Source GaN-HEMT (MVSG) model, has been adopted as an industry standard [30]. The equivalent circuit of the model is shown in Figure 4. The schematic illustrates five distinct regions of the device: the intrinsic transistor region under the gate, two field plate regions on the drain side that enhance the BV, and two access regions at the ends of the channel, modeled as implicit gate (gate voltage is V_{IG} on the schematic) transistors. The superimposed components in blue represent the modeled elements that define the device behavior. These components, implemented in Verilog-A, include: resistors modeling contact resistance; C_{GS} and C_{GD} modeling the gate-source and gate-drain capacitances; and $C_{GS,FP1}$, $C_{GD,FP1}$, $C_{GS,FP2}$, and $C_{GD,FP2}$ modeling the capacitances between each field plate and the source or drain.

In [31], the authors emphasize the importance of accurately modeling device-level effects by developing an MVSG model that uses a charge-based approach to compute terminal currents. This model accounts for phenomena such as access-region depletion, dynamic thermal behavior, and charge-trapping effects. Its accuracy was validated through simulations of a HV Buck SC and an RF power amplifier. In the Buck converter case, the model accurately predicted the slew rate of the half-bridge switching node, demonstrating its effectiveness in capturing transient behavior. Further enhancements to the MVSG model have been proposed to include the behavior of the Schottky p-GaN gate. The validity and accuracy of this extension were confirmed through comparisons with experimental data and TCAD simulations [32].

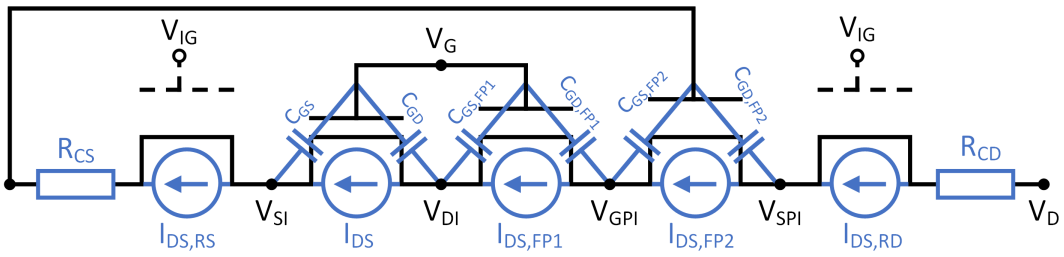

Figure 4. HEMT model equivalent circuit

3.3. GaN Packaging

The power losses in a PCS are converted into heat, which must be effectively dissipated to ensure reliable operation. As the temperature rises, the R_{on} of power transistors increases, leading to even greater power losses. Additionally, excessive temperatures can cause irreversible damage to the device, making thermal management a critical aspect of PCS design. While WBG devices deliver superior performance in smaller die areas, this miniaturization inherently limits heat dissipation. These thermal

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challenges are further intensified by the demand for higher system power densities and reduced PCB footprint, necessitating cooling solutions that do not compromise miniaturization.

To meet these requirements, chip-scale (CS) packages have been adopted for GaN devices [33]. This packaging style improves the package-to-die size ratio, reducing overall packaging costs; which helps compensate for the higher material costs of GaN; and enhances thermal performance by eliminating additional thermal impedances introduced by traditional package methods.

In [34], the thermal performance of commercial chip-scale GaN power transistors was compared to that of Si power MOSFETs housed in various packages. To ensure a fair comparison between the two technologies, Buck converters were developed using each device. When comparing a GaN HEMT to a MOSFET in a CanPAK package, both operating without additional cooling and under a 30 A load, the GaN-based system demonstrated a 35% reduction in power losses at a switching frequency of 300 kHz, and a 40% reduction at 400 kHz. When equipped with a heatsink, the SC using GaN achieves an output current of 30 A while operating at 100°C, whereas its Si counterpart is limited to 20 A under the same thermal conditions. As a result, the GaN-based system delivers 50% higher output power at the same temperature.

Another advantage of CS packaging is the reduction of parasitic resistance and inductance. Thanks to the lateral structure of GaN HEMTs, there is no need for leadframes or bond wires to bring the drain, source, and gate terminals to the same plane. In contrast, Si power transistors typically use vertical structures, which place the drain and source on opposite sides of the die, requiring such interconnections. The reduced parasitic resistance helps further decrease R_{on}, while the lower parasitic inductance enables higher switching frequencies with minimized voltage ringing. Reduced ringing, particularly on the gate signal, is crucial, as excessive oscillation can damage the gate terminal [35].

Ongoing research focuses on advancing packaging methods for emerging semiconductor technologies. In [36], the authors propose replacing traditional bond wires with copper clips and sintered copper paste to improve thermal and electrical performance. Meanwhile, [37] explores embedding the GaN die directly into the PCB and positioning the decoupling capacitor as close as possible to the die, significantly reducing parasitic inductance. These findings highlight that advanced packaging techniques are essential for emerging power semiconductor technologies to minimize parasitic elements and enhance thermal conductivity. Currently, GaN packaging improves performance through reduced thermal impedance enabled by the CS package and the use of redistribution layers with solder bumps or copper pillars, which reduce parasitic resistance and inductance while also providing an additional heat dissipation path.

4. GaN Monolithic Integrated Circuits

The high switching frequencies targeted by GaN devices pose a challenge due to the parasitic inductances inherent in the packaging, bond wires and PCB traces. Such phenomena can induce voltage ringing on the gate of GaN power transistors, potentially leading to destructive overshoot. To address this issue, the first approach was to package GaN HEMTs with Si gate drivers to minimize parasitics. To further reduce these inductances, monolithic integration of the control circuits and power transistor has emerged as a solution [38]. This chapter presents the adopted digital and analog design techniques used in this technology and reports and compares the performances of multiple GaN monolithic circuits.

4.1. Digital Design

The initial step in developing GaN ICs involves designing suitable digital circuits. Since commercial technologies lack a p-type GaN device, primarily due to the added fabrication complexity and the $50 \div 100$ times lower transconductance [38], alternative logic families have been developed to overcome this limitation. These logic families primarily differ in their implementation of the pull-up (PU) network. The main types of logic families used in GaN ICs are presented in Figure 5 and respecting the notation from the figure they are described as follows: a) Resistor-Transistor Logic (RTL): In this family, the load is a resistor [39], b) Direct-Coupled FET Logic (DCFL): Here, the PU is a d-mode GaN

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device [40], c) Pseudo-Complementary FET Logic (PCFL): In this family, the load is an e-mode device controlled by a signal complementary to the input, resembling a push-pull stage [41], d1) Bootstrapped (BS) Logic: This logic family uses an enhancement-mode device as the PU, with its gate bootstrapped through a diode and a capacitor [42]. Due to its complementary control, the PCFL family has the lowest power consumption, while the BS family exhibits better noise margins with smaller devices when compared to DCFL [42]. Additionally, the enhancements to the BS logic family proposed in [43] are illustrated in Figure 5 d2), and consist of the addition of a PD device and a resistor (highlighted in blue), which effectively reduce static current. However, this modification results in a slower rise time.

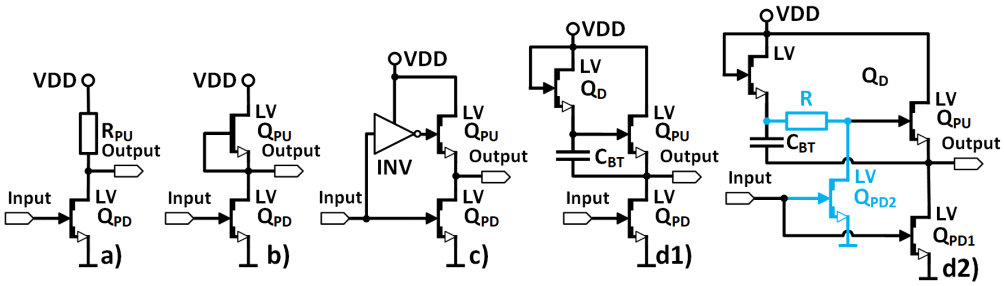

Figure 5. GaN Inverters: a) RTL, b) DCFL, c) PCFL, and d1,d2) BS

Even though the complementary GaN device demonstrates inferior performance compared to its n-type counterpart, novel approaches for its utilization have been proposed, such as in [44]. In this work, the complementary device is employed to block leakage current paths and reduce static power consumption. Moreover, the use of this hybrid topology leads to improvements in both fan-out and propagation delay.

4.2. Analog Design

Power stages and switching regulators often incorporate protection circuits; such as overtemperature, overcurrent, and overvoltage protection; which are typically implemented using analog blocks. Furthermore, as demonstrated in [45–47], control loops in SCs are also realized using analog techniques.

One challenge in GaN analog design stems from the absence of p-type devices. The lack of complementary transistors imposes several constraints: it necessitates the use of resistors as loads, limits current mirrors to sinking-only configurations, and restricts the input common-mode range of differential pairs. Given the p-type current mirrors unavailability, large area resistors are used as loads when designing GaN-based amplifiers. As shown in [48], with only 20dB per amplification stage, multiple stages of differential amplification are required to achieve a gain of 60dB. A similar cascading approach is used in the comparator of the Buck converter presented in [47], where two amplifier stages are employed to attain a gain of 31dB.

The common-mode limitation of e-mode n-type-only GaN technologies comes from the high positive threshold voltage of the devices. As a result, input signals below this threshold require level shifting. Two solutions have been proposed: in [47], diode-connected HEMTs are used in the comparator to shift the input voltage levels, whereas in [45], a switched-capacitor technique is employed for level shifting.

Crystal defects in GaN degrade device matching, imposing an additional constraint on analog design. In [38], the matching performance of various fundamental analog building blocks was evaluated. A resistive divider demonstrated a mismatch standard deviation of $\sigma = 0.76\%$ between its resistors and an absolute resistance variation of $\sigma = 10.9\%$ across the wafer. These resistors are implemented using 2DEG channels formed from HEMTs without gates. However, due to back-gating effects in the upper device, its resistance is consistently higher than that of the lower device. Threshold voltage measurements reported in [10] show that standard HEMT structures exhibit a variation of $\sigma = 229mV$, whereas structures with a modified gate reduce this variation to $\sigma = 63mV$. These

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mismatches significantly impact analog circuits, especially differential pairs, resulting in input-referred offsets as high as $\pm 200mV$.

A solution to mismatch in current mirrors is the use of source degeneration, as resistors are expected to exhibit less variation compared to HEMTs due to the absence of the layers required to form the p-GaN gate [38]. This approach has been implemented in the level shifter of the power stage described in [49], although no data is reported regarding the accuracy of current matching. To address mismatch in differential stages, auto-zeroing and chopping techniques can be applied, as demonstrated in the comparator from [50], which successfully reduces the input offset from 112mV to 1.2mV.

4.3. Power Circuits

To overcome the limitations imposed by parasitic inductance on the switching frequency of GaN transistors, monolithic integration of the driver and the PSs on a single die has been adopted, resulting in a power stage circuit. Various research implementations of such circuits are enabled by one or more of the previously discussed logic families. For example, the GaN half-bridge circuit in [49] employs a combination of RTL and PCFL logic, while the design in [39] exclusively uses RTL gates. Additionally, the commercial GaN IC presented in [51] is based on the BS logic gates family.

The characteristics of multiple power stages are summarized in Table 3. The IC detailed in [52] exhibits the slowest switching frequency and the highest R_{on}, serving as a reference Si power stage. The multi-die approach from [53], which combines Si control with GaN PSs, stands out among the listed circuits by achieving the lowest R_{on} at 4.4 mΩ, the highest drain current of 35 A, and the second-highest switching frequency of 10 MHz.

The power stage presented in [54] integrates switches with an R_{on} of 30 mΩ, the second-lowest value in the table, and supports a high switching frequency of 25 MHz. The design utilizes the modified BS logic gate family shown in Figure 5 d2) to enhance PU speed and reduce static power consumption. While it results in higher power consumption at lower frequencies, it achieves lower power consumption in the 25–30 MHz range compared to a commercial Si driver. It also features a level shifter with high common-mode transient immunity, as well as an adaptive PD switch that prevents signal loss during freewheeling. The circuit presented in [55] employs a segmented, binary-weighted driver to control the voltage slopes of the gate and drain terminals. This approach effectively reduces gate voltage oscillations, thereby preventing the potential damage of this terminal. The power stage presented in [56] exhibits the highest dynamic power loss, due to its RTL driver implementation. Although this work does not propose a complex design, it compares the circuit's performance with simulation results based on the MVSG model for the HV device, showing a maximum error of 21.2% in the t_{ON} switching time parameter. In [49], a novel protection method for the high-side latch in the level shifter is proposed. The drivers are implemented using RTL gates that control two push-pull stages in a PCFL configuration, reducing power consumption in the stages with higher output current capability. Two different supply voltages are used to configure the resistance of the PU devices and mitigate voltage overshoots at the gates of the PSs. The commercial circuit in [51] employs the BS logic family and is the only GaN power stage that integrates a bootstrap switch for the high-side driver; all other implementations use an external diode. It supports a maximum operating current of 40 mA at 3 MHz, while the BS power stage from [54] achieves a current consumption of 20 mA at 5 MHz. The circuit also includes an undervoltage lockout block that enables operation only when the supply voltage exceeds a specified threshold.

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Table 3. Drivers Comparison

Param. \ Work	[54]	[55]	[56]	[49,57]	[51]	[52]	[53]
$V_{DD}[V]$	5	12(1)	6	6(2)	12	24(4)	5
$Freq[MHz]$	25	5	10	6.25	3	1.2	10
$Area[mm^2]$	2	-	4.75	6.6	10.2	-	-
Logic Family	BS	RTL	RTL	RTL, PCFL	BS	CMOS	CMOS
$R_{HS}[m\Omega]$	30	80	-	500	14.5(3)	100	4.4
$R_{LS}[m\Omega]$	30	80	67	500	14.5(3)	100	4.4
$I_{DS}[A]$	1.5	3	10	-	15	9	35
$V_{DSMax}[V]$	25	200	100	650	60	28	90
$P_{Static}[mW]$	100	-	-	-	21	60(5)	22.5
$P_{Dynamic}[mW@MHz]$	≈200@25	-	2070@10	132@30	40@3	-	75@0.5

Notes:
(1) V_{DDLS} is 6.8V and V_{DDHS} is 12V. (2) V_{dd} is 6V and V_{dd+} is 11V.
(3) In the previous datasheet version the value was 8.5$m\Omega$.
(4) The voltage gets internally regulated down to 5V.
(5) The type of power consumption isn't specified. Static power is assumed.

Another promising type of power circuit for GaN monolithic integration is the switching regulator, which is a system that incorporates a power stage and a control loop. Multiple Buck SCs have been reported [45–47].

The circuit presented in [45] is realized in an e-mode 650V GaN technology, occupies an area of 2.1mm^2 and achieves an efficiency of 95.6% for an input of 85V. The control loop operates in boundary conduction mode. It integrates a zero voltage detector (ZVD) and reads the output current through a shunt resistor. When the switching node reaches zero volts, the driver control signal is set high, and when the current reaches a peak value determined by an external voltage reference, the signal is set low. This way, the average current is set by the reference voltage.

A GaN Buck converter for server POL applications is proposed in [46]. It is designed in a 200V GaN-on-SOI technology, and for a load of 3A and a switching frequency of 250kHz, it achieves an efficiency of 84.3% when stepping down from 48V to 1V. The integrated feedback loop employs voltage mode control.

In this work [47], a SC fabricated in a 650V GaN technology is presented. The circuit converts from 400V to 48V, occupies an area of 16.25mm^2, and achieves an efficiency of 93.1%. A peak efficiency of 95.4% is reached when stepping down from 250V to 150V. The converter employs a constant-on-time (COT) control method and integrates a ZVD, which enables soft switching of the low-side transistor, resulting in up to a 5.5% efficiency improvement. The minimum on and off times of the control loop are trimmed using 5-bit and 3-bit resolution, respectively, through adjustment of a binary-weighted capacitor bank. The power stage can operate at frequencies up to 3.5MHz, but the COT controller is capable of generating control signals only up to 1.7MHz.

5. GaN Power Converters Evaluation

In [10], the authors evaluate the performance improvements offered by GaN transistors over their Si counterparts in Boost converters, considering both synchronous and non-synchronous topologies. The non-synchronous converter operates at a frequency of 500 kHz and, in continuous conduction mode (CCM), achieves a peak efficiency of 98.2% with the Si device, while the GaN version achieves 98.5% with a flatter efficiency curve at higher loads. The synchronous Boost converter operates at 100 kHz; the Si version could deliver only 2.4 kW of power due to overheating at higher loads, achieving a peak efficiency of 97%. In contrast, the GaN implementation could deliver 37.5% more power while exhibiting an efficiency of 99%.

The emergence of GaN technology, with its small footprint and high switching frequencies, has enabled a wide range of GaN power converter-based applications, including satellites, augmented

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reality systems, and robotics [10]. The use of GaN devices has also facilitated hybrid SC topologies, such as those in [58] and [11]. The inverter reported in [58] utilizes 10 μH inductors enabled by high switching frequencies, achieving an efficiency of 98.6% and a power density of 35.3 kW/L. This PCS was developed as a lightweight solution for aircraft electrification. Moreover, due to their higher BV and radiation tolerance, these devices are well-suited for space applications, enabling compact, high-efficiency PCS, as demonstrated in [11]. This POL converter achieves a peak efficiency of 90.9% and a power density of 123.3 kW/L. For the same area reduction and efficiency benefits, GaN ICs have been adopted in commercial portable chargers, such as those in [59,60].

The author's forecast for the development of GaN technology is outlined in the following paragraphs. In the case of discrete devices, the advancement of 300 mm GaN wafers is expected to enable the fabrication of vertical devices capable of withstanding BVs exceeding 1200 V. These devices will compete with IGBTs and SiC-based components, positioning GaN technology within the mid- to high-power range of the power semiconductor spectrum.

For IC technologies, GaN-based solutions are anticipated to incorporate a broader variety of devices, including fuse elements, which would allow on-chip parameter calibration directly within the power stage, eliminating the need for external Si based circuitry. Device structures will be optimized for both cost and electrical performance, with particular attention to parameter variation and manufacturing yield. Furthermore, as reported by Intel in [61], hybrid integration of Si and GaN is feasible, suggesting that growing HEMT power devices directly on a Si driver could become a practical approach.

At present, monolithic GaN power stages have gained traction in portable applications such as chargers, drones, and robots. However, wider adoption is anticipated in data center servers and in hybrid or fully electric vehicles, particularly for DC-DC converters between the system's HV and LV batteries. Upon the commercial release of devices with a BV of 1200 V, GaN is expected to be adopted in traction inverters and OBCs as well.

Due to the small form factor of GaN devices and the benefit of enabling smaller reactive components we can expect to see a rise in compact system-in-package (SiP) designs. Regarding packaging, CS packages are widely used across semiconductor technologies due to their low cost, small footprint, reduced parasitics, and goode thermal conduction. Thermal performance can be enhanced by adding thermal pads that facilitate the attachment of heat sinks. A potential implementation has been investigated in [62], where the backside of the die is removed to allow filling with a high thermal conductivity material, such as copper. This technique could be applied to both SiPs mounted on PCBs and chips employing CS packaging.

6. Conclusion

This paper presented the need for efficient, high power density PCS. It showed that, while Si is currently used across a wide range of power applications, its performance is fundamentally limited by its physical properties. As alternatives, several semiconductor technologies were discussed, including WBG and UWB materials, with a focus on GaN. By reviewing key advancements in GaN technology; spanning fabrication processes, device design, compact modeling, packaging, circuit implementation, and converter architectures; this work demonstrated its suitability for next-generation power electronics. Through its high switching frequency, small footprint, and low R_{on}, GaN technology has been shown to meet the demands for high efficiency and power density in applications such as portable chargers, electric vehicles, and satellites. This was supported by reported performance examples, such as a monolithically integrated GaN Buck converter achieving 95.4% peak efficiency when stepping down from 250V to 150V, and a synchronous Boost converter using discrete GaN transistors, which delivered 37.5% more power while maintaining 99% efficiency. GaN devices have also enabled new converter topologies, including hybrid inverters and hybrid POL converters, and have improved the feasibility and cost-effectiveness of topologies like the matrix converter. Thus, GaN power devices, through their superior physical properties, have surpassed Si in low to mid power

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applications. With continued technological advancements, GaN could compete with SiC in the mid to high power range and approach its theoretical limits; eventually to be surpassed by future UWBG materials.

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Abbreviations

The following abbreviations are used in this manuscript:

ADAS	Advanced Driver Assistance Systems
AlN	Aluminum Nitride
BDS	Bidirectional Switch
BE	Body Electronics
BS	Bootstrapped
BV	Breakdown Voltage
CAVET	Current Aperture Vertical Electron Transistor
CCM	Continuous Conduction Mode
COT	Constant-On-Time
CS	Chip-scale
DCFL	Direct-Coupled FET Logic
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HEMTs	High Electron Mobility Transistors
HV	High Voltage
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
INFO	Infotainement
LV	Low Voltage
MIS-HEMT	Metal-Insulator-Semiconductor HEMT
MVSG	MIT Virtual Source GaN-HEMT
OBC	Onboard Battery Charger
PCB	Printed Circuit Board
PCFL	Pseudo-Complementary FET Logic
PCS	Power Conversion System
PD	Pull-Down
PE	Power electronics
POL	Point-Of-Load
PS	Power Switch
PU	Pull-Up
RTL	Resistor-Transistor Logic
RF	Radio Frequency
SC	Switching Converter
SB	Switching Block
Si	Silicone
SiC	Silicone Carbide
SiP	System in Package
UWBG	Ultra Wide Bandgap
WBG	Wide Bandgap
ZVD	Zero Voltage Detector

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