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Article

Combined Effects of TID Radiation and Electrical Stress on n-MOSFET Current Mirrors

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Abstract: The aim of this study is to present the combined effects of total ionizing dose (**TID**) radiation and electrical stress on the performance of n-MOSFET current mirrors. We propose a novel approach to analyze the complex interaction between these two factors by subjecting devices to different doses of **TID** and **electrical stress**. The results indicate that TID radiation gives rise to a threshold voltage shift and degradation in transconductance. Furthermore, we demonstrate that the combined effects of TID and electrical stress lead to a more significant degradation of current mirror characteristics than either stressor alone. These anomalies are explained as due mainly to charge trapping in the oxide layer. The work highlights the importance of considering both **TID** radiation and **electrical stress** in designing and qualifying high performance **n-MOSFET** current mirrors for radiation-hardened environments.

Keywords: n-MOSFET current mirrors; Total Ionizing Dose; Electrical stress; Threshold voltage; Current gain; Input-output impedances

1. Introduction

As semiconductor technology has advanced, integrated circuit (**IC)** applications revealed a signifying progress and the harsh environment of space has also had a significant impact on device performance. According to statistics performed on satellite failures, a major part is found to be arising from electronic circuits rather than mechanical ones **[1-2]**. Space radiation poses a significant threat to the reliable operation of electronic circuits, particularly **MOS** devices. Exposure to radiations can induce single**-event (SE)** and **total-ionizing-dose (TID)** effects. While much of the research has focused on SEE effects, there remains a limited body of work addressing the TID mechanisms. An inverter, as a fundamental building block of a **MOS** circuit **[3]**, is a crucial element to understand the overall system's radiation tolerance. The **TID** effect is characterized by a cumulative degradation of electronic device performance due to exposure to high-energy rays and charged particles **[4-6]**. It is worth noting that the latter **TID** mechanism constitutes the main factor limiting the life time of these devices. Opposed to the **SEE**, the **TID** effect cannot be completely mitigated. Therefore, a comprehensive analysis of the latter **TID** effect is essential for assessing the radiation hardness of an integrated circuit. Even at low doses, **MOS** devices exhibit a higher susceptibility to radiation [**7-9]**. These changes are primarily attributed to the accumulation of positive charges within the oxide layer and the generation of interface traps at the **SiO2/Si** interface **[10-11].** Beyond the immediate impact on device performance, the long-term reliability of devices after exposure to radiation is crucial for ensuring mission success. The device reliability after radiation is important for applications. Knowledge of dependability is also crucial to establish device aging models [**12-15].** Electrical stress exerted on **MOS** devices can lead to shifts in threshold voltage, degradation in transconductance, and other critical parameter variations **[16-20]**.These changes can have cascading effects, causing failures in both analog and digital circuits. To the subject of biasing, integrated circuits **(ICs)** require essentially accurate bias voltages and currents for their proper operations **[21-23]**. Traditional **CMOS** dividers were usually used to realize a suitable biasing. But they again suffer from their dependency

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on the process technology, supply voltage and temperature **[24]**. More recently, current mirrors **(CMs)** have been conceived as new building devices to attain an appropriate biasing. Also, the **CMs** can amplify or attenuate a current from one location to another in an analog **IC**

[25-26]. Hence, an efficient design of a **CM** is mainly to achieve better performance parameters such as current gain, input-output impedances and power consumption.

The present work is aimed to investigate the combined effects of **electrical stress** and **TID** on the electrical aging of **CMs** based on **n-MOSFETs**. The paper is organized as follows: **Section I** is dedicated to a brief introduction and related works; **Section II** presents the electrical aging model for **n-MOSFET** structures; **Section III** describes the reliability analyses of **TID** effects on **n-MOSFET** current mirrors; **Section IV** summarizes conclusions and prospects.

2. Electrical Aging Model for n-MOSFETS Structrues

2.1. Hole Trapping

Due to ionizing radiation, the charge build-up into the oxide layer arises from the generation of electron-hole pairs and a subsequent hole trapping. This supposes that de-trapping of holes is neglected. Another simplifying hypothesis can also be adopted. It consists in assuming that the distribution of hole traps is uniform. Which leads to set up the rate equations that govern the trapping of holes as follows :

$$\frac{\partial p_{Trapped}(x,t)}{\partial t} = \frac{d\gamma}{dt} - v\frac{\partial p_{Free}(x,t)}{\partial x} \quad \textbf{Eq.(1)}$$

$$\frac{\partial p_{Trapped}(x,t)}{\partial t} = \sigma\, v\, p_{Free}(x,t)[N_T - p_{Trapped}(x,t)] \quad \textbf{Eq.(2)}$$

where ɣ denotes the rate of generation of electron-hole pairs per unit volume, v is the velocity of holes, σ defines the capture cross-section of the trap sites and $N_T$is the density of hole traps throughout the oxide layer. Under this form, it is worth noting that Eqs **(1)** and **(2)** can be solved exactly only when the term ɣ is not accounted for. An illustration is given in the report of Ning **[27].**Later, the charge build-up in MOS structures has been undertaken by Viswanathan

[28]. Most interesting, the rate equations were solved for ɣ non null, but in two limiting cases:

i- the density of trapped holes is not large enough compared to the total number of hole traps.

ii- the trapping efficiency is much less lower than the rate of electron-hole generation. The solutions thus adopted in the last case can be combined under a general form:

$$P_{Trapped\ holes}(x,t) = N(1 - e^{-\frac{x}{\lambda}}) \quad \textbf{Eq.(3)}$$

with { **N= ɣ ;λ** $=\frac{1}{N_T}$} in the first limiting case and { **N=N_T;λ=**$\frac{1}{\sigma\gamma}$ }in the second one.

The origin of the x-axis is fixed at the gate-dioxide interface. As has been found, the density of trapped holes shows an exponential amount with a saturated trend going towards the silicon-dioxide interface. In **Eq.(3)** , λ can be interpreted as the probability per unit length of a hole to being trapped within the oxide layer under irradiation.

2.2. Time-Dependent Hole Trap Density and Transconductance

Because of hole trapping, a potential shift can occur at the oxide terminal and whose expression versus trapped holes p(x,t) is given by :

$$\Delta V_{FB}(t_{ox},\lambda) = -\frac{q}{\varepsilon_0\varepsilon_{rox}}\int_0^{t_{ox}} xP_{Trapped}(x,t)\,dx \quad \textbf{Eq.(4)}$$

where q is the electronic charge,ε_{rox}represents the dielectric constant of the oxide layer,$\varepsilon_0$is the permittivity of free space, t_{ox} is the oxide thickness and FB is a subscript meaning flat band. In evaluating the integral as a function of t_{ox}, the mean trapping free length is treated as a parameter. Calculation of $\Delta F_{FB}(t_{ox},\lambda)$under a positive bias voltage leads to the following expression:

$$\Delta V_{FB}(t_{ox},\lambda) = -\frac{qN\,t_{ox}^2}{\varepsilon_0\,\varepsilon_{rox}}F(\frac{t_{ox}}{\lambda}) \quad \textbf{Eq.(5)}$$

with:

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$$\mathbf{F}\left(\frac{\boldsymbol{t_{ox}}}{\lambda}\right) = \frac{1}{2} + \frac{(\frac{\boldsymbol{t_{ox}}}{\lambda} + 1)}{\frac{\boldsymbol{t_{ox}^2}}{\lambda^2}} e^{-\frac{t_{ox}}{\lambda}} - \frac{1}{\frac{\boldsymbol{t_{ox}^2}}{\lambda^2}}$$

For a fixed thickness of the oxide layer and taking the mean trapping free length λ less low than t_{ox} ,the pre-exponential factor N will correspond to the hole trap density N_T. On the other hand, by identifying $\Delta V_{FB}$to the threshold potential shift ΔV_{th} (TID) as measured under irradiation, we can derive the TID-dependent oxide trapped charge density from the relation:

$$\mathbf{N_T\ (TID)} = \frac{\varepsilon_0\ \varepsilon_{rox}}{q\ t_{ox}^2\ F(\frac{t_{ox}}{\lambda})} \Delta \mathbf{V_{th}\ (TID)} \qquad \textbf{Eq.(6)}$$

To further improve the trapping charge model, it is required to assume the existence of an additional sheet charge near the $\mathbf{Si/SiO_2}$ interface,related to surface states or arising from shallow traps .To account for the contribution of all these charge states can be approximately made by defining an effective density of hole traps as: $\mathbf{N_T^{EFF} = (1 + \alpha)N_T}$ where α represents a centesimal percent factor being negative if the additional sheet charge is predominated by electron-traps or positive in the reverse case. Here, this correction is not taken into account.

A deal of interest would also be paid to the transconductance parameter. Let $V_{GS}(t, TID) = V_{GS}(t, TID = 0) + \Delta V_{FB}(t, TID)$ be the gate-to-source bias voltage under gamma radiation. Similarly, to the hole trap density, the time-dependent transconductance is taken under the form:

$$\mathbf{g_m(TID)} = \frac{\mathbf{g_m(TID=0)}}{1 - \eta[\frac{q\ t_{ox}^2}{\varepsilon_0\ \varepsilon_{rox}}\ \mathbf{F}\ (\frac{t_{ox}}{\lambda})\ ]\mathbf{N_T\ (TID)}} \textbf{Eq.(7)}$$

where η is an empirical factor and g_m (TID=0) is the initial transconductance before irradiation. Note, that η can be determined from measured g_m (TID) and calculated N_T(TID) using the relation:

$$\eta = \frac{1 - \frac{\mathbf{g_m(TID=0)}}{\mathbf{g_m(TID)}}}{\frac{q\ t_{ox}^2}{\varepsilon_0\ \varepsilon_{rox}} \mathbf{F}\ (\frac{t_{ox}}{\lambda})\ \mathbf{N_T\ (TID)}} \textbf{Eq.(8)}$$

3. Reliabilityanalyses of Total Ionizing Dose Effects ON n-MOSFET Current Mirrors

3.1. Electrical Aging Behavioral of an n-MOSFET

The n-MOSFET under investigation has been fabricated using **1 μm** channel technology. The thickness of oxide layer is fixed at $\mathbf{t_{ox}}$**=25 nm** . More details on the epitaxial growth and the annealing process are available in **Ref [29].**

Concerning $\mathbf{V_{GS}}$**-**$\mathbf{I_{DS}}$ characteristics, measurements were performed before and after irradiation for V_{DS} fixed at **50 mV** in the linear regime and $\mathbf{V_{DS}}$**=3V** in the saturation regime. As it is seen, the threshold potential shows a negative shift with increased TID and the relevant data are found to be fitted by the polynomial law:

$$\mathbf{\Delta V_{Th}} = \mathbf{1.69 - 124\ 10^{-5} \times TID} \qquad \textbf{Eq. (9)}$$

where $\mathbf{V_{th}}$ **(TID=0)=1.69Volt**.From measured $\mathbf{\Delta V_{th}(TID)}$,we have deduced the density N_T of induced hole traps as a function of **TID** using **Eq(6).** The mean trapping free length is fixed at $\boldsymbol{\lambda}$**=5nm** which corresponds to $\mathbf{e^{-\frac{t_{ox}}{\lambda}} = 6.10^{-3}}$. Results are depicted in **Fig.1**, on an interfacial charge plot $\mathbf{N_T^{2D} = N_T \times t_{ox}}$.It clearly appears that the trapping of holes shows a gradual amount as the total ionizing dose increases. As has also been provided, the interfacial density of hole traps is related to TID by the fitting relation :

$$\mathbf{N_T^{2D}(10^{11} cm^{-2}) = -356 \times 10^{-5} + 238 \times 10^{-5} \times TID - 1.78 \times 10^{-7} \times TID^2}$$ in cm^{-2}Eq. (10)

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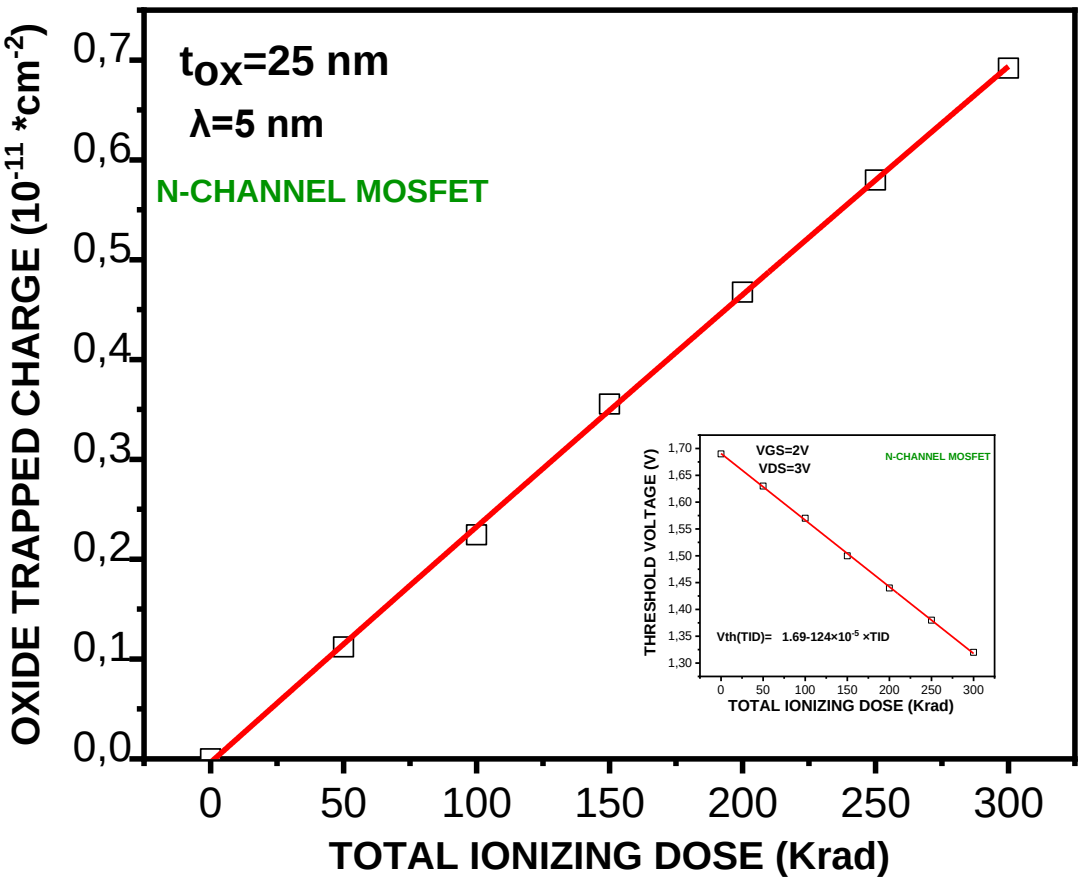

Fig1: The oxide trapped charge versusTID for an n-MOSFET with L=1 µm and W=24 µm

In addition to N_T, the graph shows the corresponding threshold potential versus TID.As a proposal of explanation, exposure to relatively high TID levels induces defects in the MOS capacitance. Which can make it difficult for electrons to flow into the conductive channel. Microscopically, an accumulation of holes reduces switching speed of the **MOSFET**. As a peculiar feature, the threshold potential shift is found to be more significant at lower TID doses. Additionally, an increase in the threshold voltage can enhance the power consumption. Another fundamental parameter of the **n-MOSFET** that is impacted by gamma radiation consists in then transconductance. Measurements of this parameter have led to an increasing trend versus TID. The data points are depicted in **Fig.2** with the obtained fitting:

$$\mathbf{g_m\,(TID) = 1.11 + 1.02\ 10^{-3}\ \times TID}\ \ \text{in } \mu\mathbf{S} \qquad \textbf{Eq. (11)}$$

From measured $\mathbf{g_m}$ **(TID)** and $\mathbf{N_T}$ **(TID)**,we have computed the empirical factor **η (TID)**.Results are found to be fitted by:

$$\eta\left(\mathbf{10^{15}m^{-2}}\right) = \mathbf{-0.042 - 3.35 \times 10^{-5} \times TID + 7 \times 10^{-7} \times TID^2} \\ \mathbf{-1.45 \times 10^{-9} \times TID^3} \qquad \textbf{Eq. (12)}$$

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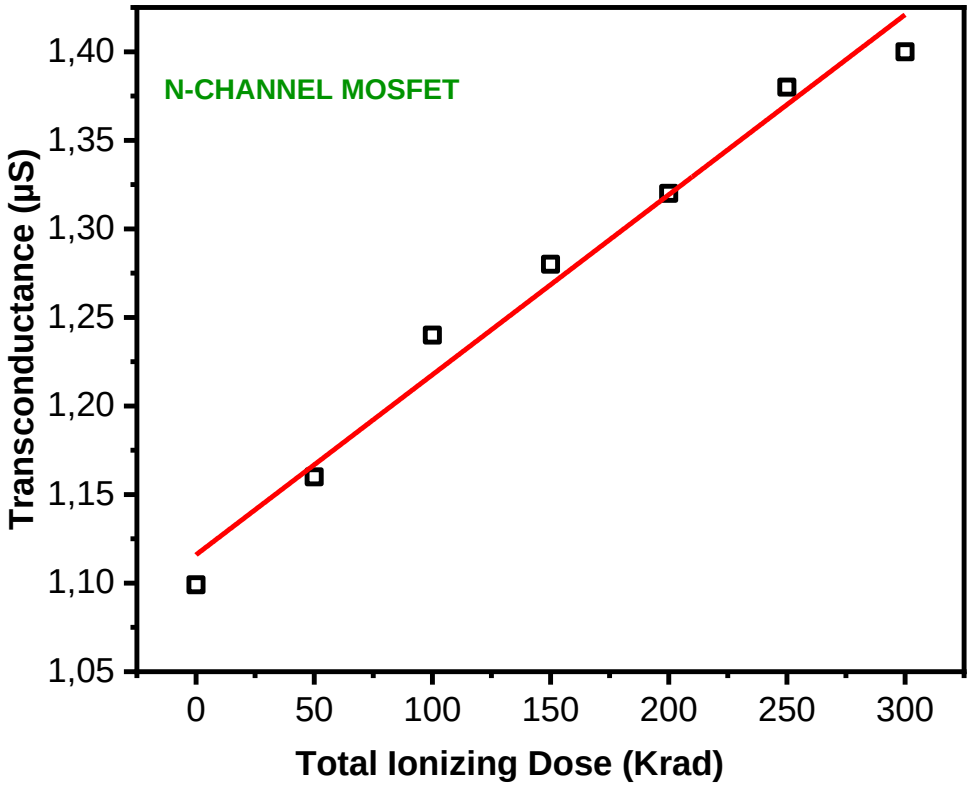

Fig 2: TID-dependent transconductance for an n-MOSFET with L=1µm and W=24µm

For the conductance, however, how we did make in relating this parameter to the charge built-up into the oxide. Calculation has been made using **TID** as an auxiliary variable, which has led to the plot of **Fig.3.** As can be noticed, the conductance increases with TID according to the fitting:

$$\mathbf{g_d(TID) = 1.16\ 10^{-5} + 2.8310^{-8} \times TID - 171\ 10^{-11} \times TID}$$

Eq. (13)

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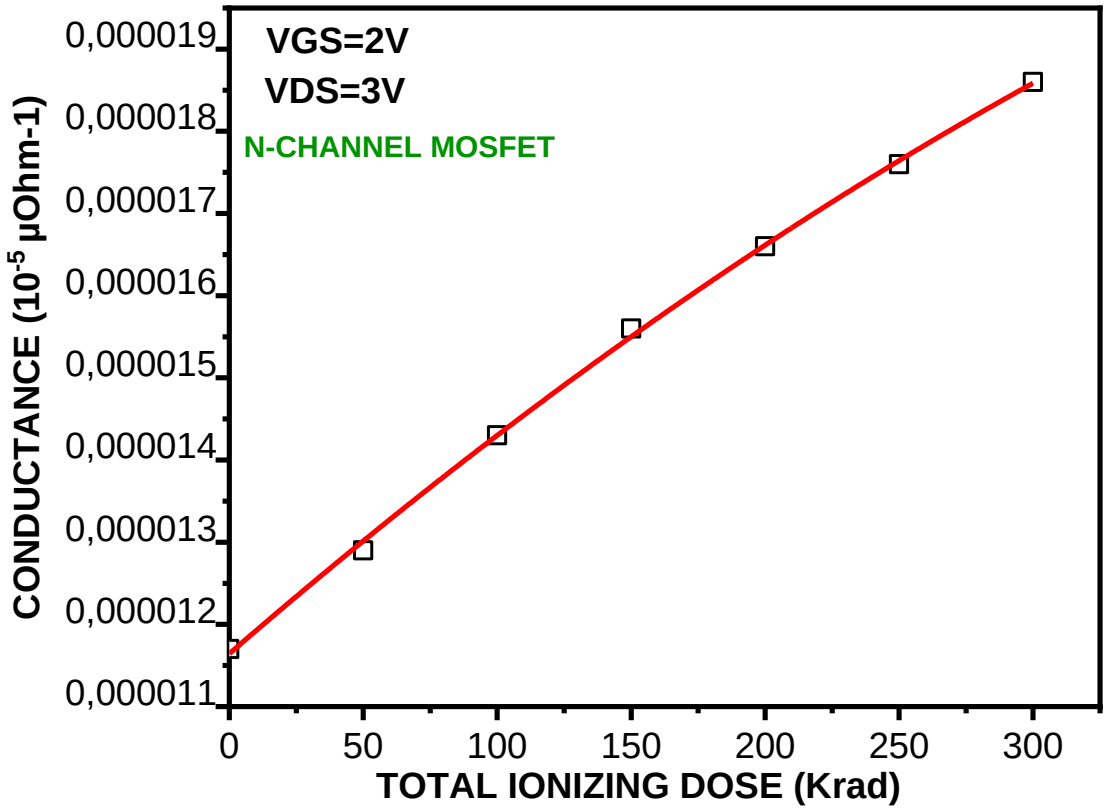

Fig 3: The conductance versus TID of n-MOSFET with L=1µm and W=24 µm

3.2. Electrical Degradation Mechanisms in n-MOSFET Current Mirrors

The biasing CM as it used in AMS integrated circuits **[29]** is shown in **Fig.4** with its dynamical equivalent scheme. It is constructed using two n-MOS transistors labelled M1 et M2.The diode-connected transistor M1 operates in saturation regime and converts the reference current I_{REF} into a corresponding gate-to-source voltage V_{GS1}. The transistor M2 is a regenerating module that gives rise to an output current I_{OUT}. If both the transistors M1 and M2 are matched, the gate-to-source biases V_{GS1} and V_{GS2} are equal and then I_{REF} would be perfectly at the output of CM. Under saturation conditions, the reference and output currents are given by the set of electrical equations:

$$I_{REF} = \frac{1}{2}\,\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 \qquad \textbf{Eq.(14)}$$

$$I_{OUT} = \frac{1}{2}\,\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2 \qquad \textbf{Eq.(15)}$$

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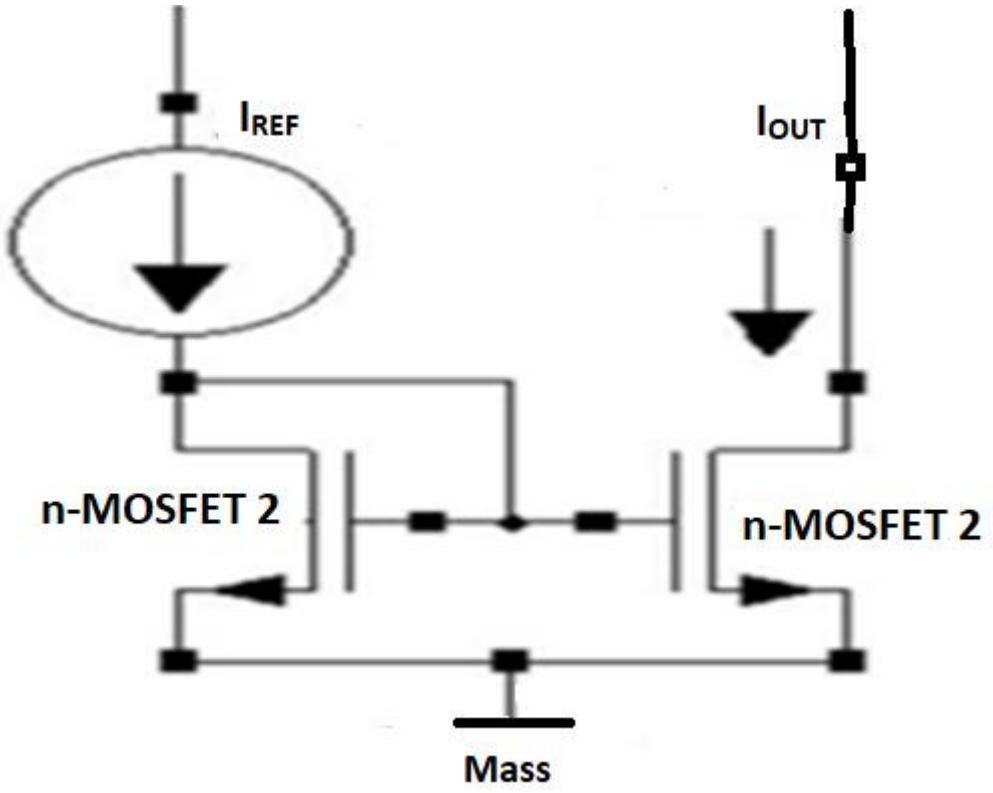

Figure 4. The basic n-MOSET current mirror circuit SCM.

where μ_n is the electron mobility, C_{ox} denotes the MOSFET capacitance per unit area and V_{THi} **=1.2** are the threshold potentials of the n-MOSFETs. From I_{REF} and I_{out} , we can derive the current gain. It is undoubtedly that this parameter is affected by irradiation. Let **TID1=x TID** and **TID2= (1-x)TID** with 0≤ x ≤1 be the total ionizing doses for the **MOSFET1**and **MOSFET2** transistors respectively. The current gain of the SCM reads as:

$$\mathbf{A_{i(x,TID)}^{SCM}} = \frac{(\frac{W}{L})_2}{(\frac{W}{L})_1} \times \frac{V_{GS}-V_{TH}[(1-x)TID\,]}{V_{GS}-V_{TH}[xTID]} \qquad \textbf{Eq.(16)}$$

where x represents a dissymmetric percent that characterizes the **TID** contamination of the **n-MOSFETs**. Calculation of $\mathbf{A_i^{SCM}(x.TID)}$ has led to a graph of the current gain of an **n-MOSCM** versus x for different TIDs as illustrated in **Fig.5**. We note that the current gain is a measure of how much an **n-MOSFET** mirror can replicate a current signal. The plot also shows that the current gain decreases as TID increases. This is because exposure to ionizing radiations damages the **MOSFET's** gate oxide and reduces the ability of the gate to control the flow of current between the source and drain. As a further observation, the decreasing rate in current gain is found to change with the dissymmetric percent. Analytically, the **x-** and **TID-** dependent current gain are fitted according to:

$$\mathbf{A_i^{SCM}(x, TID) = a_0 + a_1 \times TID + a_2 \times TID^2} \qquad \textbf{Eq. (17)}$$

$$\mathbf{a_0(x) = 1.017 + 0.00388 \times x + 2.14\,10^{-17} \times x^2}$$

$$\mathbf{a_1(x) = -0.024 - 0.0088 \times x + 5\,10^{-6} \times x^2}$$

$$\mathbf{a_2(x) = -0.057 + 0.00229 \times x + 8.3510^{-6} \times x^2}$$

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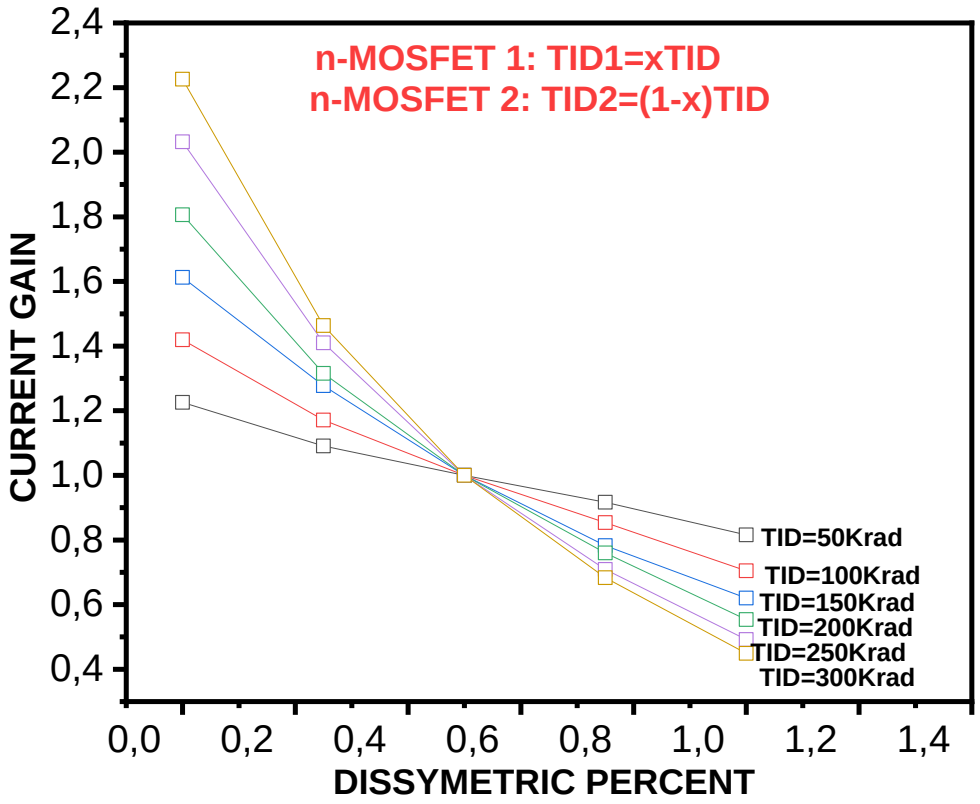

Fig 5: The current gain of a SCM as a function of the dissymetric percent at diffferent TID levels

Usually concerning the dissymmetric percent, it is worth to notice that a relatively high value of this coefficient means that the **n-MOSFET** gate-oxide becomes more asymmetric. This makes it sufficiently susceptible to submit damages from ionizing radiation. Two other important parameters were dialed with an interest. They consist in input and output impedances of the **SCM**. According to that **TD1** and **TD2** were defined above, both impedances read under the forms:

$$\mathbf{R_{in}^{SCM}(x, TID)} = \frac{\mathbf{1}}{\mathbf{g_{m[xTID]}}} \qquad \textbf{Eq. (18)}$$

$$\mathbf{R_{out}^{SCM}(x, TID)} = \frac{\mathbf{1}}{\mathbf{g_{d[(1-x)TID]}}} \qquad \textbf{Eq. (19)}$$

Using **Eq.18** and **Eq.19**, we have calculated R_{in}^{SCM} and R_{out}^{SCM} versus x for different TIDs ranging from 50 Krad to 300 Krad. As can be seen, **Fig.6** shows a clear positive correlation between the dissymmetric percent and input impedance, independently on the TID level. Such an increasing in impedance is assigned to the disruption of conduction paths caused by asymmetry. Moreover, the effect of **TID** is significant, suggesting that defects created by radiation also reinforce the **CM** resistance at input. The graph of **Fig.7**, however, shows how the output impedance is affected by the two factors. As it is seen, the impedance at output decreases with increased asymmetry percentage and total ionizing dose. In terms of analytical fitting of $\mathbf{R_{in}^{SCM}(x, TID)}$ and $\mathbf{R_{out}^{SCM}(x, TID)}$, it is provided by the following set of expressions:

$$\mathbf{R_{in}^{SCM}(x, TID)} = \mathbf{a_0 + a_1 \times TID + a_2 \times TID^2} \qquad \textbf{Eq. (20)}$$

$$\mathbf{a_0(x) = 1.11 - 1.55\ 10^{-18} \times x}$$

$$\mathbf{a_1(x) = -7.91\ 10^{-4} - 0.00157 \times x}$$

$$\mathbf{a_2(x) = 0.047 - 6.45\ 10^{-4} \times x}$$

$$\mathbf{R_{out}^{SCM}(x, TID)} = \mathbf{a_0 + a_1 \times TID + a_2 \times TID^2} \qquad \textbf{Eq. (21)}$$

$$\mathbf{a_0(x) = 86295.45 - 0.63 \times x}$$

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$$\mathbf{a_1(x) = -1679.69 - 173.37 \times x}$$
$$\mathbf{a_2(x) = -4684.79 + 83.85 \times x}$$

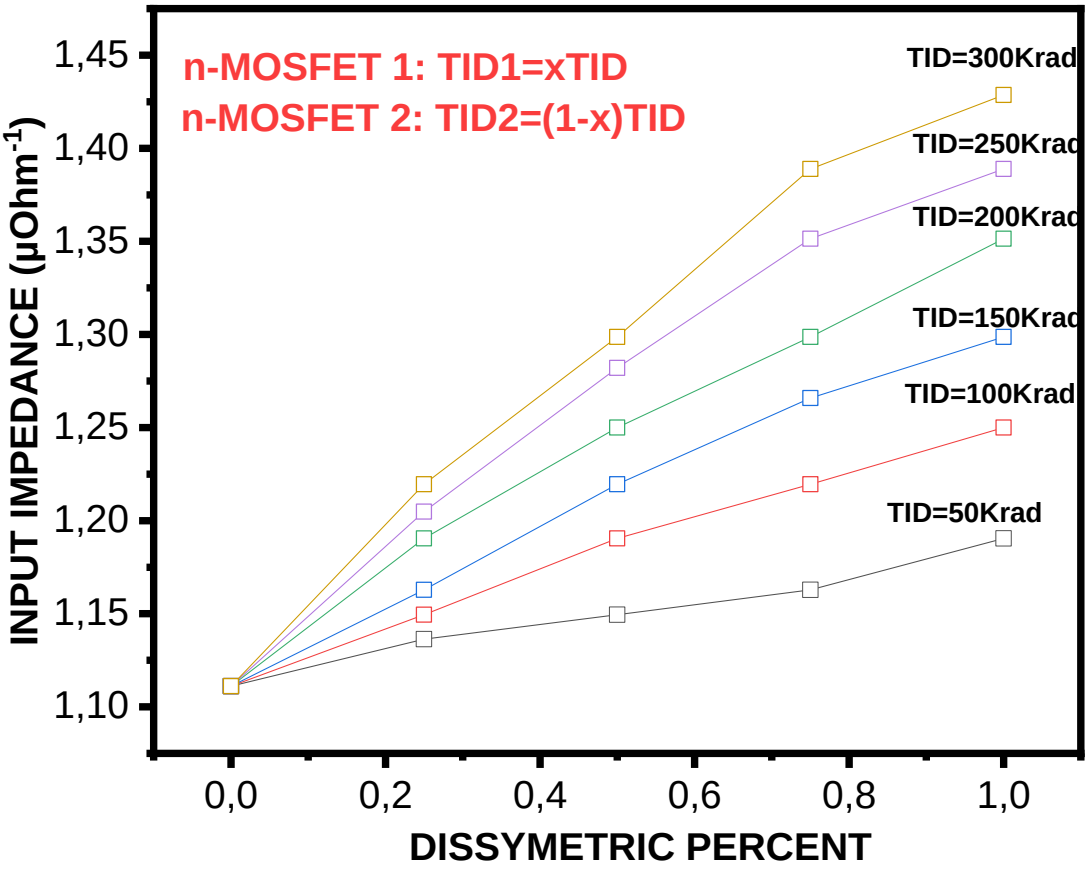

Fig 6: The x- and TID-dependent input impedence of a SCM

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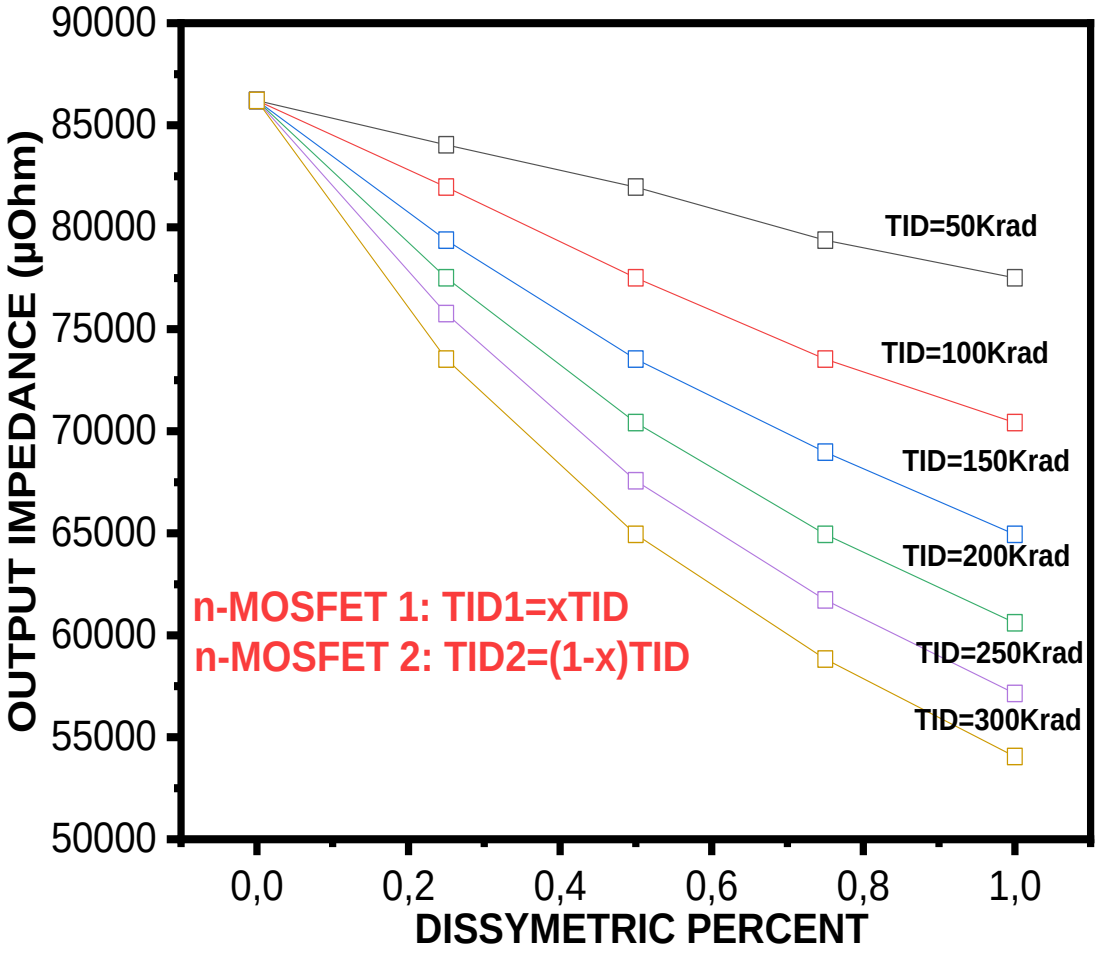

Fig 7: The x- and TID-dependent output impedence of a SCM

In a concluding remark, input and output impedances of a perfect current mirror should be very low and large enough respectively. This suggests that degradations induced by geometric dissymmetry and the effect of ionizing radiation, have a negative impact on CM' ability to deliver more current to the load. It is then required to characterize these degradations in an attempt to develop an equivalent model that includes the parameter related to a radiation-hardened environment. In practice, SCMs are suitable for low voltage applications. Technologically, the limited usage of SCMs is contributed to their low output impedances. Some remedies were conceived to further improve the impedance at output. They consisted in widlar CM [26] and cascade CM [25-26] designs. As has been found, the output impedance of a SCM is increased due to Widlar and Cascade arrangements with respective ratios.

$$\frac{R_{out}^{WMC}}{R_{out}^{SCM}} = 1 + Rg_{m2} \text{ and } \frac{R_{out}^{Cascode\ CM}}{R_{out}^{SCM}} = r_{ds3}g_{m3}r_{DS2}g_{DS1} \qquad \textbf{Eq.(22)}$$

In closing this subsection, it is worth to mention that the cascade technology can open a promising way to construct electronic applications with low voltage operation and low power consumption. But the use of complexed configurations needs a multitude of elementary transistors. Because of different operating regimes, the cascade **CMs** could exhibit a mismatching in current and voltage between input and output. Exposure to ionizing radiations would lead to further degradations as well.

4. Conclusions

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In this study, we have investigated the combined effects of **TID** radiation and electrical stress on the performance of **current mirrors** based on **n-MOSFETs**. Through experimental measurements and simulations using LTspice, we analyzed both **TID** radiation and electrical stress independently contribute to a degradation of the current mirror's accuracy, matching, and electrical performance. Our results demonstrate that both TID radiation primarily causing charge trapping in the gate oxide leading to a threshold voltage shift, while electrical stress provokes these effects by a further altering device characteristics such as transconductance and current gain. Consequently, **current mirrors** subjected to both **TID** radiation and **electrical stress** show significant changes in their characteristics, leading to a loss of precision and reliability. The findings highlight the importance of considering both radiation and electrical stress in the design and qualification of **n-MOSFET** current mirrors for radiation-hardened applications. To mitigate these effects, it is essential to explore design optimizations such as improved radiation-hardened materials, fault-tolerant circuit topologies, and enhanced device shielding techniques. Further research should focus on developing a complete model to predict the combined impact of **TID** radiation and **electrical stress**. This undoubtedly allows to design more accurate **MOSFET-circuits** against high gamma-ray doses.

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