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Posted Date: 24 May 2024

doi: 10.20944/preprints202405.1611.v1

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Article

Study of the Leakage Current Transport Mechanisms in Pseudo-Vertical GaN-on-Silicon Schottky Diode Grown by Localized Epitaxy

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Abstract: In this work, a GaN-on-Si quasi-vertical Schottky diode was demonstrated on a locally grown n-GaN drift layer using Selective Area Growth (SAG). The diode achieves a high current density of 2.5 kA/cm², a specific on-resistance $R_{ON,sp}$ of 1.9 mΩ.cm² despite the current crowding effect in quasi-vertical devices and on/off current ratio (I_{on}/I_{off}) of 10^{10}. Temperature-dependent current-voltage characteristics have been measured in the range of 313 - 433 K to investigate the mechanisms of leakage conduction in the device. At near zero bias, thermionic emission (TE) was found to dominate. At voltage range from -1 to -10 V, electrons gain enough energy to excite into trap states, leading to the dominance of Frenkel-Poole emission (FPE). For a higher voltage range (-10V to -40V), the increased electric field promotes electron hopping along the threading dislocations in the "bulk" GaN layers, and thus, Variable Range Hopping becomes the main mechanism for the whole temperature range. This work provides an in-depth insight into the leakage conduction mechanisms on vertical GaN-on-Si Schottky barrier Diodes (SBDs) grown by localized epitaxy.

Keywords: gallium nitride; pseudo-vertical p-n-diodes; localized epitaxy; leakage mechanisms

1. Introduction

Wide band gap (WBG) materials are gaining popularity due to the increasing need for high-power, efficient, and reliable semiconductor devices in sectors like transportation, consumer electronics, and renewable energy. Currently silicon (Si) reaches its technological limits, WBG materials such as silicon carbide (SiC) and gallium nitride (GaN) are gradually replacing silicon-based technologies.

Gallium Nitride (GaN) has become increasingly popular in the world of power devices due to its remarkable properties such as wide bandgap, high electron mobility, and a strong breakdown field strength. These factors collectively enable GaN-based devices to offer low on-resistance (Ron) and the ability to operate at high frequencies in high-voltage applications [1,2].

Today, commercial GaN high-electron-mobility transistors (HEMTs) are based on lateral AlGaN/GaN heterostructures grown on foreign substrates such as Si, SiC, or sapphire. These lateral devices benefit from the two-dimensional electron gas (2DEG) that forms at the interface of the AlGaN and GaN heterostructures. However, commercial HEMT devices are limited in terms of voltage capability and cannot exceed 1kV [3]. Since the current is more determined by the distance between the source and drain contacts, lateral dimensions of the device must be increased significantly to achieve such a high breakdown voltage BV impacting the on resistance (Ron). HEMT devices typically operate in a normally-on state, which requires special structures such as recess gate, p-GaN gate, or ion implantation to discontinue the 2DEG and enable normally-off operation [3]. Nonetheless, normally-off HEMT devices still face challenges such as high threshold voltage instability due to charge trapping and current collapse, which require further attention. An

 doi:10.20944/preprints202405.1611.v1

alternative structure that addresses these issues involves using vertical GaN devices grown on native GaN substrates [4–7]. Vertical GaN devices offer several advantages over lateral GaN devices, such as increased scalability, improved heat dissipation, reduced surface sensitivity, enhanced reliability and high-voltage capability (BV > 600 V).

However, the use of free-standing GaN substrates holds the potential for strain-free GaN epitaxy and the development of fully vertical device geometries [8]. However, challenges such as high production costs, variable quality, small wafer size, and limited availability hinder their widespread adoption. Consequently, there has recently been a heightened focus on fabricating vertical power devices on foreign substrates such as silicon, sapphire and QST™ [9,10]. Silicon substrates, highly favored from a commercial point of view, encounter a significant challenge during GaN growth due to the difference in coefficient thermal expansion between GaN and silicon. Although this can be managed by strain engineering, total layer thickness is limited to ~ 14μm, with lower drift layer thickness [11–14]. In order to overcome this limitation and increase the maximum achievable Breakdown Voltage (BV), Selective-Area Growth (SAG) or localized epitaxy is a promising approach. It has been shown that during SAG of GaN micro pillars [13], stress is effectively reduced by elastic relaxation and thus the maximum epitaxial layer thickness can be increased. Other advantages of using selective epitaxy approach include reduced growth time due to higher growth rates and simplified fabrication for quasi-vertical diodes [13].

In this work, we demonstrate quasi-vertical GaN Schottky barrier diodes (SBDs) grown on Si substrates using localized epitaxy [15], and we investigate their electrical performance in forward and reverse mode. The leakage current transport of GaN quasi-vertical SBDs on Si are likely to be different from freestanding GaN-on-GaN SBDs. The high dislocation density, caused by the mismatch of lattice constant between GaN and Si, can lead to different conduction modes. Therefore, it is necessary to understand the leakage current transport mechanism of GaN quasi-vertical SBDs on Si. Many researchers have reported that variable range hopping (VRH) by dislocations is the main off-state leakage mechanism in vertical GaN diodes on Si, sapphire and GaN substrates [16]. Others have found that the dominant leakage mechanisms in GaN-on-Si SBDs are different at different reverse biases, and depend on the presence of Edge Terminations (ET) [17,18]. This work aims to understand the carrier transport processes in pseudo-vertical Schottky barrier diodes (SBDs) GaN on Si obtained by selective area growth (SAG). In this work, we carried out a comprehensive study on the current transport mechanism of quasi-vertical GaN SBDs on Si at various bias conditions by current–voltage I–V measurements in a wide temperature range from 313 to 433 K.

2. Materials and Methods

In this study, as presented in Figure 1a, samples were grown on a single-wafer fully automated AIXTRON Crius-R200 metal-organic vapour phase epitaxy (MOVPE) tool, on 200 mm-diameter Si(111) wafers. The structure from the bottom to the top, consists of AlN and AlGaN buffer layers, an undoped 300 nm-thick GaN layer and three 350 nm thick n+-GaN layers acting as current spreading layers (5 x 10^{16}, 5 x 10^{17} and 5 x 10^{18} cm^{-3} Si doping densities respectively increasing from bottom to top). The spreading layer is separated into different doping levels so that they can be used as calibration layers in other studies to examine the doping level in the drift layer on cross-section analysis [15]. A 50 nm-thick Al_2O_3 mask was deposited on these layers by atomic layer deposition at 300 °C, and was then patterned with photolithography and etching.

Localized epitaxial growth of the drift layer was subsequently performed in the openings of this mask, demonstrating a doping concentration of N_D-N_A~ 1.5 x 10^{16} cm^{-3} as showed in Figure 1b (evaluated by capacitance-voltage C-V measurements according to Equation (1). A built-in voltage Vbi = 0.95 V was also obtained from the linear extrapolation of the values of (A^2/C^2) versus the reverse voltage).

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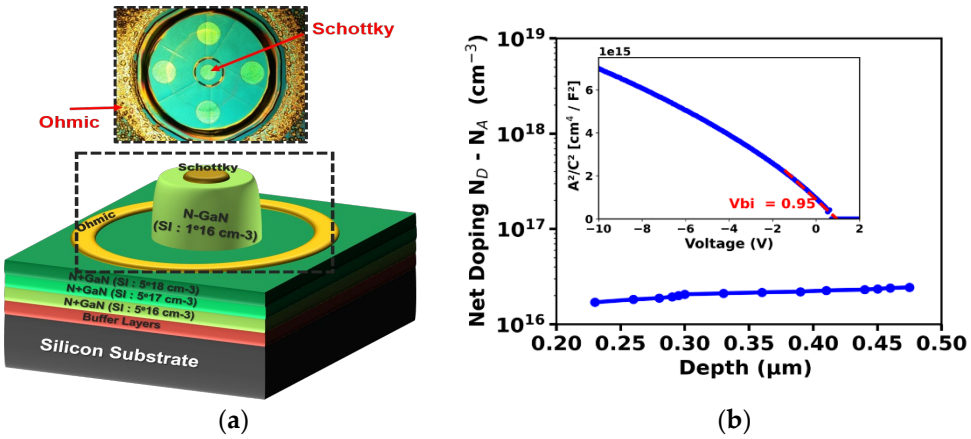

Figure 1. (**a**) Schematic cross-section of quasi-vertical Schottky diode using localized epitaxy, Inset: optical microscopy of the circular measured devices. (**b**) net doping concentration (N_D - N_A) in the n-GaN drift layer from the C-V curve at 1MHz. Inset: (A^2/C^2) versus the reverse voltage.

To go into more details, an intentionally doped GaN layer was grown at 1040 °C, with a nominal growth rate of 1.5 µm/h (for full wafer growth). The pressure of the chamber was 400 mbar, the NH_3 flow set at 10 slm and the growth time was 2 hours. The dopant of the layer was Si and its intended doping concentration was 1 x 10^{16} cm^{-3}. The precursors for gallium and silicon were tri-methyl gallium (TMGa) and silane (SiH_4), respectively. The SiH_4 flow value was set as that for a full wafer growth. The Al_2O_3 mask was not removed after the growth.

After that, the Al_2O_3 mask around the mesa was etched by Cl_2 and Ti/Al/Ni/Au (95 nm/200 nm/20 nm/165 nm) metal stack was deposited on the n+ GaN as the cathode contact, followed by rapid thermal annealing (RTA) at 750 °C, to form the ohmic contacts. Finally, circular Ni/Au (50 nm/150 nm) Schottky contacts were formed on the n−GaN drift layer by a liftoff process followed by 5 min of thermal annealing at 400 °C.

$$N_D - N_A = \left[-\frac{2}{q\varepsilon_s\varepsilon_0} \frac{1}{\frac{d\left(\frac{A^2}{C^2}\right)}{dV}} \right], \quad (1)$$

where ND, NA, q, $\boldsymbol{\varepsilon_s}$, $\boldsymbol{\varepsilon_0}$ and A denote the donor and acceptor concentration in n− GaN, the electron charge, the relative permittivity of GaN, the vacuum permittivity and the area of the anode, respectively.

3. Results

3.1. Forward Bias

Electrical characterization of devices was performed using a 4156C Precision semiconductor parameter analyzer and a Keithley K2657 Tesla GPIB 24 parameter analyzer. The measured diodes have a diameter of 90 µm and an anode diameter of 50 µm. The current in this study was normalized using an area of $A = 3.14 \times 25^2 \times 10^{-8}$ cm^2.

Figure 2a shows the typical forward J-V characteristics in semi-log scale obtained on a GaN pseudo-vertical Schottky diode, showing a low turn-on voltage of ~ 0.6 V defined at J = 1 A/cm^{-2} and a good On/Off current ratio of 10^{10}. The device achieves an output current density of ~ 2.5 kA/cm^2 and low differential specific on-resistance $R_{ON,sp}$ of 1.9 mΩ.cm^2 at 5V as shown in Figure (b), despite the expected current crowding effect at the edges in quasi-vertical structures [19]. The ideality factor n of 1.03 and the Schottky barrier height $\emptyset_B$ of 0.95 eV (consistent with the extracted schottky barrier height from C-V measurement ~ 1.02 eV) were extracted from Equation (2), at room temperature (RT = 300K). The high current on/off ratio and near-unity ideality factor indicate the excellent quality of the Ni/n-GaN interface. These characteristics suggest efficient electron flow when the device is on and minimal leakage when the device is off, showcasing the interface's effectiveness in controlling

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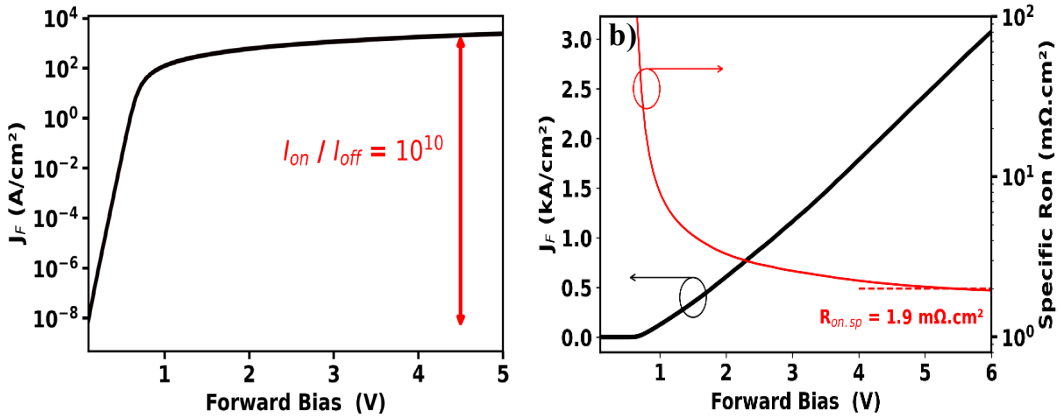
current. Additionally, the near-unity ideality factor implies that the diode closely follows ideal diode behavior, indicating that the dominant current is Thermionic Emission TE.

$$I_{TE} = I_s\left[\exp\left(\frac{qV}{nkT}\right) - 1\right], \text{where } I_s = AA^*T^2\exp\left(-\frac{q\emptyset_B}{kT}\right) \quad (2)$$

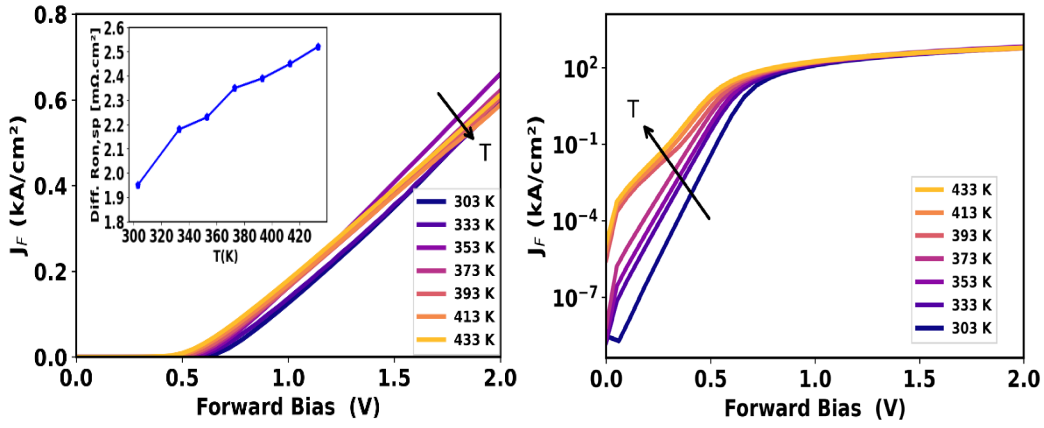
Where I_s is the saturation current, A is the area of the anode contact, A^* is the effective Richardson's constant (theoretically 26.4 A/cm².K² for GaN), $\emptyset_B$ is the Schottky barrier height, q is the elementary charge (1.6×10^{-19}), k Boltzmann's constant, T is the temperature and n is the ideality factor.



(a) (b)

Figure 2. Typical forward J-V curves obtained GaN pseudo-vertical SBD diode in (**a**) semi-log and (**b**) Linear scale, respectively.

Figure 3a,b show the typical temperature-dependent forward characteristics of the SBD. For all measured samples, the T-J-V characteristics show two trends when the forward voltage V is lower (V < ~0.6 V) and higher (V > ~0.6 V). When V is low, the current is dominated by hot electron emission from GaN to Ni/ contact across the Schottky barrier. The higher the temperature, the more electrons have enough energy to cross the Schottky barrier, and the higher the current. On the other hand, when V is higher, the current is limited by electron transport in the n-GaN drift region following the ohmic conduction law. As the temperature increases, the mobility of electrons decreases and the differential Ron,sp increases from 1.9 mΩ.cm² at 25 °C to 2.5 mΩ.cm² at 160 °C, probably due to the reduced electron mobility, attributed to thermally enhanced phonon scattering as shown in the inset of Figure 3a [21].



(a) (b)

Figure 3. (**a**) Temperature-dependent forward J-V characteristics on a linear scale (Inset: differential specific on-resistance $Ron_{,sp}$ as a function of temperature T) and (**b**) in semi-log scale.

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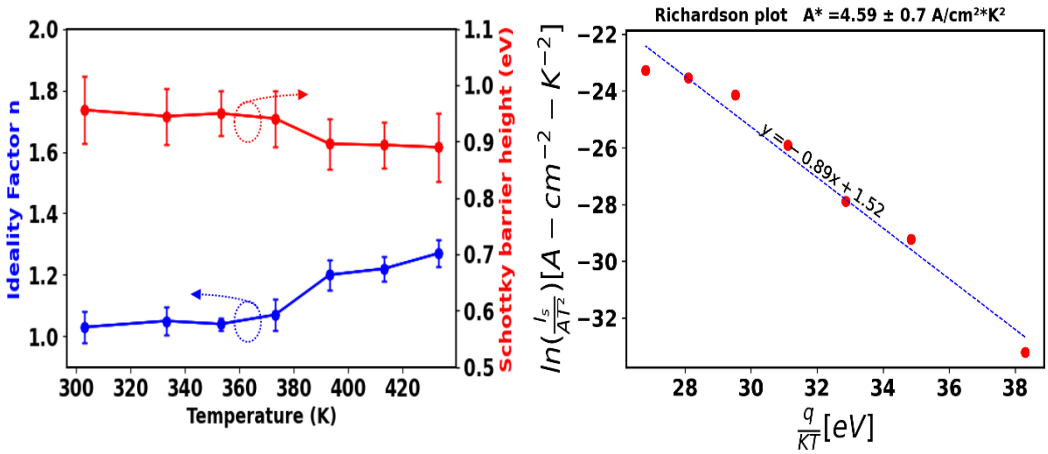
From Equation (2), I_s and n can be determined from the intercept and the slope of the linear region of ln (J)-V plot respectively. In Figure 4a, the ideality factor n of several devices increases from 1 to ~ 1.3 ± 0.05 at higher temperature which may indicate the impact of the surface traps on device performance [20], the extracted n suggest that the current transport mechanism is dominated by the thermionic emission (TE) at low temperature (from 300 K to 375K) and by thermionic field emission (TFE) at higher temperature (T > 375 K). The variation of barrier height $\emptyset_B$ when the temperature is between 375 and 425 K as shown in Figure 4a, confirms the impact of traps on the Ni/GaN interface. These results suggest the thermal instability of the Schottky contact of the SBD at high temperatures. [22]

From calculations as illustrated in Figure 4b, the experimental Richardson's constant for several devices determined from the intercept of the linear fitting of Equation (2) of 4.6 ± 0.7 A cm^{-2} K^{-2}. It is suggested that the discrepancy from the theoretical value of 26.64 A K^{-2} cm^{-2}, is due to the quality of the epitaxial layers and inhomogeneity in the barrier [23].

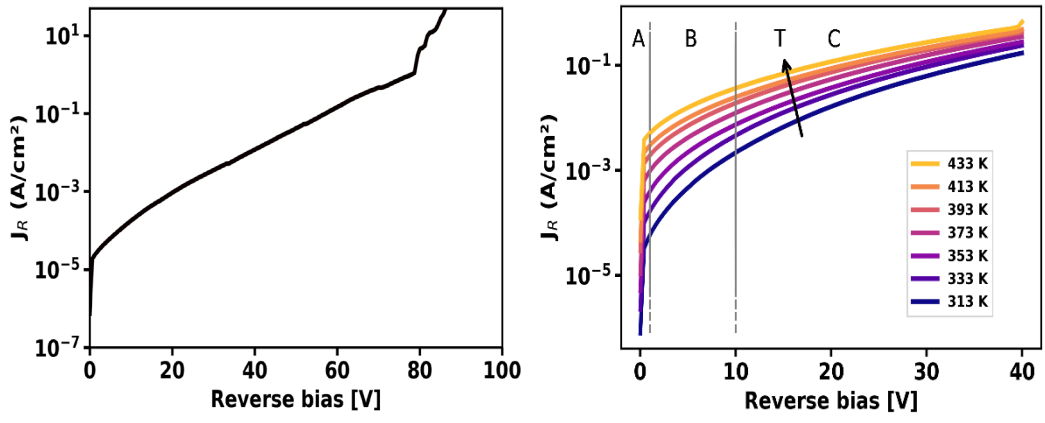


(**a**) (**b**)

Figure 4. (**a**) Extracted ideality factor n and Schottky barrier height as a function of temperature for several measured devices, and (**b**) the experimental Richardson's plot.

3.2. Reverse Bias

Figure 5a shows the typical reverse J-V characteristics of the GaN pseudo-vertical SBD. The destructive Breakdwon Voltage BV of the schottky barrier diode is around 80 V, this low voltage capability is mainly related to the absence of edge termination [17,18], and in particular due to expected high electric field at the edges of the Schottky contact.



(**a**) (**b**)

Figure 5. (**a**) Typical breakdown characteristic of the fabricated pseudo-vertical GaN and (**b**) Typical temperature-dependent reverse J–V characteristics on the log scale.

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Leakage current in vertical devices has typically been associated with defects in the active layers since the dislocation density is high [11,24], in particular for GaN on Si devices.

The physical origin leakage current leakage in Schottky barrier diode SBDs can be either based on the electrical properties at the electrode - Semiconductor interface. These are referred to as electrode - limited conduction mechanisms. Other mechanisms which depend only on the properties of the Semiconductor material itself, These conduction mechanisms are called bulk - limited conduction mechanisms or transport - limited conduction mechanisms. It is crucial to distinguish between these mechanisms, as multiple conduction processes can simultaneously contribute to current flow through the GaN drift layer. Measuring temperature-dependent conduction currents can provide insights to reveal the origin of these currents, given that different mechanisms respond differently to temperature changes. The electrode-limited conduction mechanisms include (1) Schottky or thermionic emission _TE, (2) Fowler-Nordheim tunneling _FNT, (3) direct tunneling or field emission _FE, and (4) thermionic-field emission _TFE. On the other hand, the bulk-limited conduction mechanisms include (1) Poole-Frenkel emission _FPE, (2) hopping conduction, (3) ohmic conduction, (4) space-charge-limited conduction _SCLC, (5) ionic conduction _IC and (6) grain-boundary-limited conduction [16].

To investigate the reverse leakage mechanisms, temperature dependence of reverse J-V curves for Ni/Au SBDs was measured from 313 to 433 K with voltage up to – 40 V, as shown in Figure 5b. The characteristics can be divided into three different voltage regions. Region "A"is near zero bias, while region "B" is from -1 to -10 V and region "C" is -10 to -40 V. For Schottky devices under a reverse regime, the voltage is supported across the drift region, forming a depletion layer, with a maximum electric field located at the metal-semiconductor contact. The breakdown voltage is constrained by breakdown at the edges. Edge terminations are necessary to reduce the electric field at their location, leading to behaviour closer to parallel-plane breakdown.

Table 1 summarizes only the possible current transport mechanisms and their electric field and temperature dependencies of Schottky barrier diodes SBDs grown with localized epitaxy, many process were excluded as the most investigations already reported for GaN on Si devices are focused on few mechanisms such as Thermionic emission TE, Frenkel- Poole Emission FPE, Variable Range Hopping VRH, and finally Trapped or Phonon – Assisted Tunneling TAT, PAT [16].

Table 1. Summary of the possible leakage mechanisms for SBDs [25], where J is current density, E is the electric field, E_c the characteristic field, n is the ideality factor, T is absolute temperature, k is Boltzmann's constant, $\emptyset_t$ is barrier height for the electron emission from the trap state associated with FP emission, ε_s is the relative dielectric constant of GaN, C is a constant of the order of unity, a is the localization radius of the electron wave function, T0 is characteristic temperature, and W_D is the depletion width. The electric field can be obtained from the following expression:.

Mechanism	Expression	E-field dependence	Temperature dependence
Thermionic emission [20]	$J_{TE} = J_s\left[\exp\left(\frac{qV}{nkT}\right) - 1\right]$	$\ln(J_{TE}/T^2) \propto \sqrt{E}$	Yes
Frenkel–Poole [26]	$J_{FPE} = CE\exp\left(-\frac{q(\emptyset_t - \sqrt{qE}/\pi\boldsymbol{\varepsilon_s})}{kT}\right)$	$\ln(J_{FPE}/E) \propto \sqrt{E}$	$\ln(J_{FPE}) \propto 1/T$
Variable-range-hopping [27]	$J_{VRH} = J(0)\exp\left(C\frac{qEa}{2kT}\left(\frac{T_0}{T}\right)^{-0.25}\right)$	$\ln(J_{VRH}) \propto E$	$\ln(J_{VRH}) \propto (1/T)^{0.25}$
Phonon-assisted tunneling [28]	$J_{PaT} = \exp\left(\frac{E^2}{E_c{}^2}\right)$	$\ln(J_{PAT}) \propto E$	Insensitive

$$E = \sqrt{\frac{2q(ND - NA)}{\boldsymbol{\varepsilon_s}}\left(V + V_{bi} - \frac{kT}{q}\right)}, \quad (3)$$

Where V_{bi} and $N_D - N_A$ were extracted from CV measurements as mentioned above.

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In Region A, the leakage current can be limited by the Schottky contact, for which the conduction mechanism is dominated by Schottky emission. Electrons can gain sufficient energy by thermal excitation; electrons from the metal will overcome the Schottky barrier towards the conduction band. The Figure 6. Illustrate the Ni / n-GaN energy band diagram when the metal is under negative bias. Thermionic emission mechanism is one of the most observed conduction process in Schottky barriers diodes (SBDs).

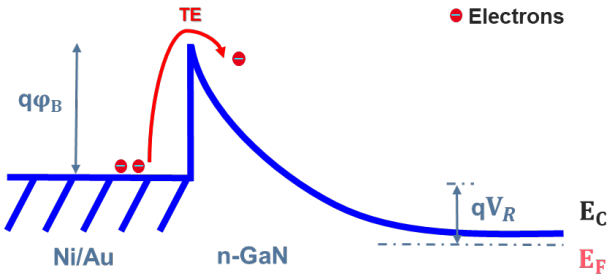

Figure 6. Schematic energy band diagram of Schottky emission in metal-semiconductor structure.

Figure 7a shows the reverse ln (J) versus V obtained at different temperatures at voltages from 0 to -0.4 V. The good fit between the experimental data and the Thermionic Emission (TE) model suggests that TE is the main mechanism at near zero bias with barrier lowering of $\Delta_{\phi b} = 0.1 \pm 0.05$ eV (The barrier lowering due the image force phenomenon is called Schottky effect). Furthermore, the linear relation between ln (J/T^2) and $E^{1/2}$, as shown in Figure 6b, confirms the dominance of this mechanism in this region.

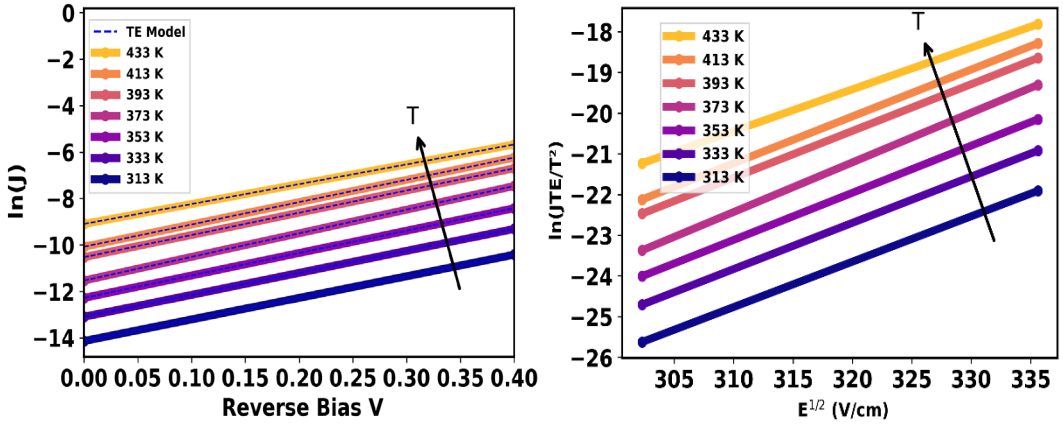

Figure 7. (**a**) Typical reverse ln (J) versus V with the fitting model and (**b**) ln (JTE/T^2) versus $E^{½}$ at the voltage range of 0 to -0.4 V.

In Region B, by increasing the reverse bias, the leakage current increases with temperature as observed in Figure 5b. This can be caused by the Frenkel–Poole emission (FPE), which is a process similar to Schottky emission or thermionic emission (TE), involving the thermal excitation of electrons from traps into the semiconductor's conduction band. This similarity often leads to FPE emission being referred to as internal Schottky emission. In this context, when an electron is in a trap, an applied electric field across the dielectric film can reduce the electron's Coulomb potential energy. This reduction in potential energy may increase the probability of an electron being thermally excited from the trap into the conduction band. The schematic energy band diagram of the FP emission is shown in Figure 8.

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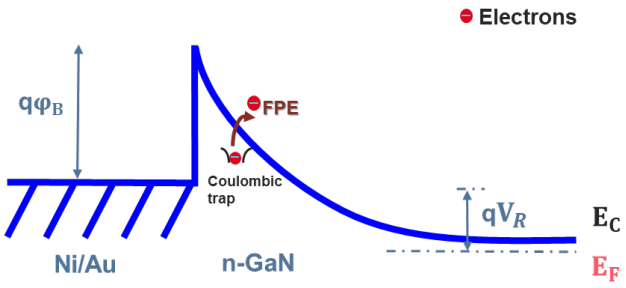

Figure 8. Schematic energy band diagram of FP emission in metal-semiconductor structure.

According to the FPE equation, ln (J/E) should have a linear relationship with the square root of electric field (Note that the electric field strength (E) was calculated using the Equation (3)) as shown in Figure 9, which indicates that FPE is the dominant leakage process in region B.

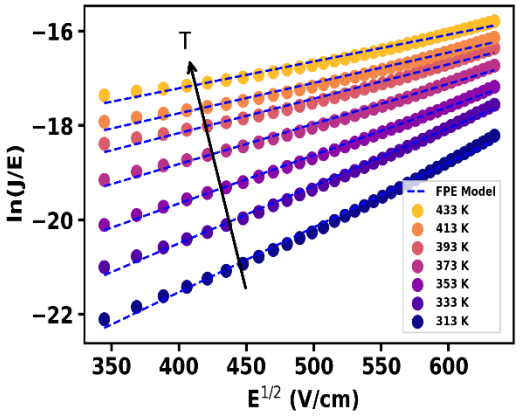

Figure 9. Typical ln (J/E) versus $E^{1/2}$ fitted with FPE model in range voltage from 0.5 to 10 V.

In such a case, $A(T)$ and $B(T)$ are the intercept and slope of the ln (J / E) versus $E^{1/2}$ plot and are defined as:

$$A(T) = -\frac{q\emptyset_t}{kT} + \ln C, \tag{4}$$

$$B(T) = \frac{q}{kT}\sqrt{\frac{qE}{\pi\varepsilon_s\varepsilon_r}}, \tag{5}$$

From Figure 10a, the trap level for FPE extracted from the linear fitting of Equation (4) is found at 250 ± 20 meV below the conduction band. They could be possibly related to nitrogen or gallium vacancies V_N-V_{Ga} and nitrogen antisite N_{Ga}- related defect [29]. However, further experiments like characterization by deep level transient spectroscopy DLTS are needed to confirm these observed traps. In addition, the relative dielectric constant of GaN has been extracted, $\varepsilon_s = 5.9 \pm 0.63$ from the linear fitting of Equation (5) as shown in Figure 10b. Furthermore, this was confirmed by the extracted Frenkel Poole coefficient β_{FP} of 3.13 x 10^{-4} eV $V^{-1/2}$ $cm^{1/2}$. These values are in good agreement with reported values for GaN (5.4 and 7 x 10^{-4} eV $V^{-1/2}$ $cm^{1/2}$ for ε_s and β_{FP}, respectively) [28,29], and confirm the domination of FPE at region B with voltage range -0.5 to -10 V.

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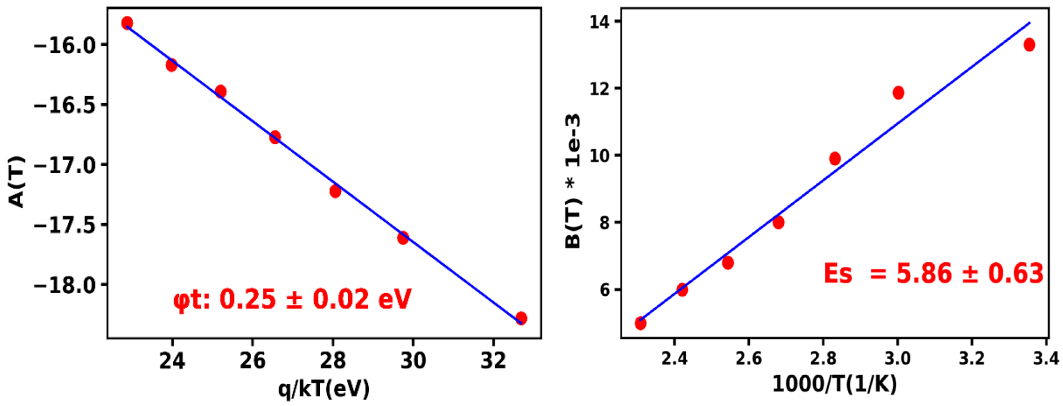


Figure 10. (**a**) The slope of the ln (*J* / *E*) versus $E^{1/2}$ A (T) as a function of $\frac{q}{kT}$. (**b**) The intercept B (T) as a function of 1000/T.

Finally, in region C, when the reverse bias increases up to -40 V with a corresponding Electric field up to 1.1 MV/cm, the leakage current becomes insensitive to the temperature. This indicates that the reverse leakage is mainly dominated by variable range hopping (VRH), for which the increased electric field distort the energy band and make it steeper. The steeper VRH band results in a shorter hopping from the Schottky Fermi level and the VRH level in GaN. Therefore, electrons could hop more easily from the Schottky metal to the GaN drift layer [30,31]. The schematic energy band diagram of the FP emission is illustrated in Figure 11.

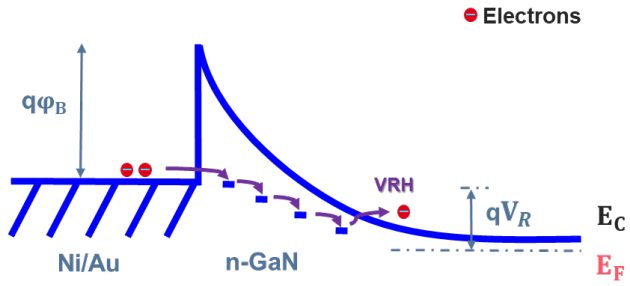
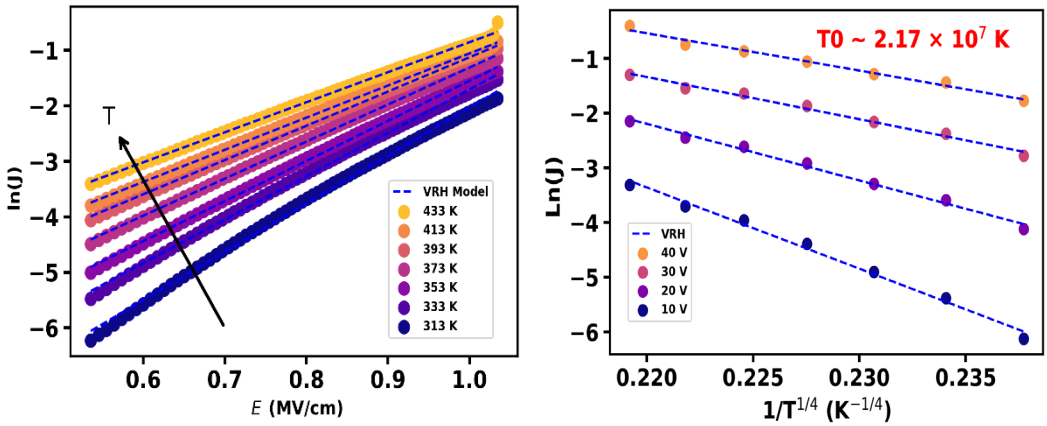


Figure 11. Schematic energy band diagram of VRH emission in metal-semiconductor structure.

The clear linear relationship between ln (J) and E is demonstrated, as shown in Figure 12a, suggest the dominance of VRH. Figure 12b shows an Arrhenius plot of the reverse current at several voltages versus the inverse of the temperature. At high field, the current has a lower temperature dependency and follows Mott's law [$\ln(J) \propto (1/T)^{1/4}$]. The extracted characteristic temperature T_0 is 2.2 ± 1.1 x 10^7 K, which is within the typical range of 10^6- 10^9 K and is consistent with reported values in the literature (4.92 x 10^7 for N_D ~ 3 x 10^{16} cm^{-3}) [32,33].



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(**a**) (**b**)

Figure 12. (**a**) ln (J) as a function of applied electric field E. (**b**) ln (J) versus $(1/T)^{1/2}$ at reverse voltage of −10, −20, -30 and −40 V.

The investigated mechanisms were further confirmed by having the differential slope d[log(ln(J))] / dlog(E) as presented in Figure 13, where J is the current density and E is the applied electric field in the depletion region. When d[log(ln(J))]/dlog(E) is around 0.5, the Frenkel – Poole emission (FPE) process is the dominant leakage mechanism. On the other side, if d [log (ln(J))] / dlog(E) is close to 1, the variable range hopping (VRH) dominates the leakage current [26].

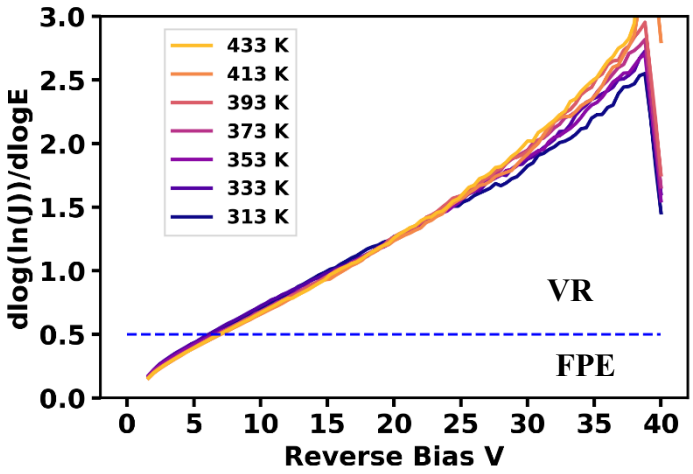

Figure 13. d[log(ln(J))]/dlog(E) of GaN on Si SBD as a function of applied voltage [26].

Figure 14, summarizes and illustrates the different leakage mechanisms revealed by temperature dependent study of GaN-on-Si quasi-vertical SBD grown by localized epitaxy. At region A, Thermionic Emission (TE) dominates the leakage current since the applied voltage has a negligible impact on the Schottky barrier, which electrons transport from metal to the n-GaN layer. As the bias increases, trapped electrons gains sufficient energy to surmount the trap state, which can be referred to the Frenkel-Poole Emission (FPE) process. Finally, at region C, the increasing electric field reduces the hopping distance from the metal to trap states, which allows the electrons to hop easily from the Schottky metal to the conduction band of GaN drift layer, which is referred to Variable Range Hopping (VRH). These leakage mechanisms are in agreement with previously reported studies for GaN devices [34–36].

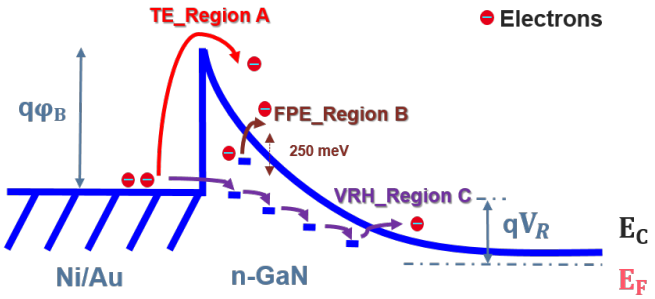

Figure 14. Schematic depicts the determined leakage processes under reverse bias for GaN-on-Si SBD grown by localized epitaxy [29,34].

5. Conclusions

In this work, GaN-on-Si quasi-vertical Schottky barrier Diodes SBDs were fabricated with Selective Area Growth (SAG). The SBDs achieved good forward performance, with a high current

 doi:10.20944/preprints202405.1611.v1

density of 2.5 kA/cm², a low turn-on voltage of 0.6 V and a $R_{ON,sp}$ of 1.9 mΩ.cm². A limited breakdown voltage of ~ 80 V was found, probably related to the absence of edge termination. Temperature-dependent reverse bias I–V characteristics in a range of 313–433 K were analysed and the leakage current transport mechanisms were investigated. At near zero bias (0 V to -0.5 V), the current density (J) follows a linear relationship with 1/T and the characteristics correspond to the Thermionic Emission (TE) leakage process. By increasing the reverse voltage up to -10 V, Frenkel-Poole emission (FPE) with an emission barrier $\emptyset_t$ of 0.25 $\pm$ 20 meV becomes dominant. At higher voltage (-10 V to -40 V), the leakage current becomes insensitive to the temperature which suggests that the Varaible Range Hopping (VRH) mechanism dominates. This work gives an in-depth insight for the leakage mechanisms and provides a useful guidance to improve GaN vertical power devices on silicon substrates.

Author Contributions: Conceptualization, E.M., J.B., D.A., T.K., D.P-A., H.E and M.C.; formal analysis, E.M.; funding acquisition, J.B. and M.C.; investigation, E.M, J.B. and D.A.; methodology, E.M.; project administration, J.B. and M.C.; resources, D.P-A. and H.E.; software, E.M, J.B. and M.-A.J.; supervision, J.B. and D.A.; validation, J.B., D.A. and M.C.; visualization, E.M.; writing—original draft, E.M.; writing—review and editing, J.B., D.A. and M.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work is part of the **ELEGaNT** project (ANR-22-CE05-0010).

Data Availability Statement: Data are contained within the article.

Acknowledgments: This work is part of the **ELEGaNT** project (ANR-22-CE05-0010).

Conflicts of Interest: The authors declare no conflict of interest.

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