Article

Low Cost Source Measure Unit (SMU) to Characterize Sensors Built on Graphene-Channel Field-Effect Transistors

Ashley Morgan Galanti * and Mark Haidekker *

Posted Date: 19 March 2024

doi: 10.20944/preprints202403.1169.v1

Keywords: source meter unit (SMU); graphene-channel field effect transistor (G-FET); light sensing

Article

Low Cost Source Measure Unit (SMU) to Characterize Sensors Built on Graphene-Channel Field-Effect Transistors

Ashley Galanti [1] and Mark A. Haidekker [2,*]

[1] School of Chemical, Materials and Biomedical Engineering, College of Engineering, University of Georgia; amg19523@uga.edu
[2] School of Electrical and Computer Engineering, College of Engineering, University of Georgia
* Correspondence: mhaidekk@uga.edu

Abstract: This study introduces a low-cost solution provided by a specialized source measure unit (SMU), offering an alternative to conventional source meter units. Through precise IV curve measurements for graphene-channel FETs, the SMU demonstrates its capability in accurately characterizing these devices with minimal noise and high accuracy. This cost-effective solution presents a promising avenue for researchers and developers seeking reliable tools for sensor development and characterization, providing valuable insights into the behavior of graphene-channel FETs and the effect of surface illumination without the need for expensive equipment. Additionally, the SMU was validated with known passive and active components, along with probe station integration for microscale connection, ensuring its effectiveness in capturing accurate measurements. The SMU's focus on collecting IV curves, coupled with its ability to identify device defects, such as Schottky junctions, contributes to its utility in quality testing for semiconductor devices. Its low-cost nature makes it accessible for various research endeavors, enabling efficient data collection and analysis for graphene-based sensor applications.

Keywords: source meter unit (SMU); graphene-channel field effect transistor (G-FET); light sensing

1. Introduction

Nanomaterial-based field-effect transistor technology is a growing research area because of their wide sensing ability through the use of semiconducting nanostructures and surface recognition elements for selective detection of target analytes. Analytes can range from clinical biomarkers to light illumination, and the nanomaterial utilized in the active gate region may include silicon nanowires, transition metal dichalcogenides, or carbon-based materials, such as graphene [1]. Graphene is a two-dimensional, single carbon atom layer material found as a hexagonal lattice known for its high electrical properties and thermal conductivity, along with excellent optical and chemical properties [2]. Microchips that use graphene are influenced by the gate potential with higher electron mobility and off/on ratios, but also by environmental factors, such as photons and chemical reactants. Graphene-channel FETs have also been demonstrated to have excellent device stability, high carrier density, large surface to volume ratio, low-power and high-speed operation, as well as low-cost fabrication [3–5].

Graphene-FETs are used for a variety of gas, environmental, and bio-sensing applications, from liquid-biopsy detection of exosomes for early cancer diagnosis [3], nitrate detection in water for quality monitoring [4], to virus detection of SARS-CoV-2 [5]. Typically, these devices monitor the shift of the Dirac point as a result of molecular binding on the sensor surface with the assistance of receptors that bind specifically to the detection target [6]. Other changes on the surface can cause a Dirac point shift, such as light source variation. As a result of graphene's optical transparency, allowing up to 97.7% of light transmission in the visible range [7], its use in optical sensing

 doi:10.20944/preprints202403.1169.v1

applications is prominent. Graphene-channel FETs can detect and measure light intensity, converting light rays to electrical signals. When exposed to incident photons light comes in, the device begins conducting and results in a shift of the electric field acting on the graphene. This shift changes the graphene's conductivity, reflected in on a changed characteristic relationship between the voltage across the sensor channel, V_{DS} and the drain current, I_D [8]. Applications of graphene-channel FET photodetection include high-speed communications, ultra-sensitive photodetectors, radiation sensors, along with sensing applications for wearable electronics [8–10].

Similar to traditional FETs, the gate of the graphene-channel FET controls the flow of electrons or holes across the channel; all of the current flows across the graphene deposited between drain and source (Figure 1). The graphene is exposed to the electrostatic field from the gate through a thin SiO_2 layer. Graphene-channel FETs allow conduction through both electrons and holes, thus resulting in their ambipolar behavior in which the majority carriers are holes during negative gate bias and electrons during positive gate bias. The two conduction bands meet at a neutrality point, known as the Dirac point, where the drain current, I_D, is lowest. The drain current should be zero; however, this point often shifts up (i.e., measurable drain current) due to doping, surface impurities, contamination from the atmosphere, and – the desirable case -- for sensing applications.

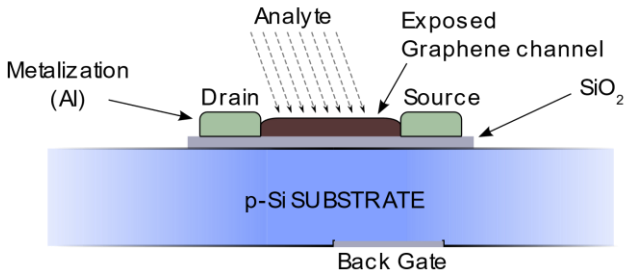


Figure 1. Schematic cross-section of a graphene-based sensor FET. The drain-source channel is formed of a graphene nanolayer, whose conductance is influenced by the gate electric field. The entire bulk silicon forms the gate, and a back-gate connection allows to apply the gate potential. When the graphene is functionalized and binds the target analyte, the conductivity changes (specifically: the Dirac point shifts), which, in turn, allows detection of the analyte.

The typical sensing application, therefore, aims to find the Dirac point by measuring the drain current I_D as a function of the drain-source voltage V_{DS} and with varying gate potential V_G. A shift of the Dirac point indicates the presence of the analyte; however, graphene FETs may face sensing challenges due to the highly sensitive gate channel and uncontrollable properties of graphene which can cause nontargets to be detected adding undecipherable noise levels or preventing device functionality altogether. Another challenge is the Debye screening problem as the response of the graphene-channel FET is strongly dependent on phenomena occurring at the nanoscale interface paired with additional complexity from target sample and detection molecules [11]. To fully characterize a graphene-channel FET as sensor, the basic curve of I_D over V_{DS} needs to be acquired, and the acquisition repeated with different gate voltage levels. Here, I_D needs to be acquired with sub-microampere precision, and at the same time the gate voltage varied over tens of volts [13].

In this paper, we are presenting such a device for acquiring the FET characteristic curves. A source measure unit (SMU) is an instrument that can precisely source voltage or current while simultaneously measuring voltage and/or current; in other words, it combines a sourcing and measurement function on the same pin or connector. Such SMUs are available commercially, but at costs that range from typically $5,000 to $30,000 with no low current options available. We introduce the hardware components, which are primarily analog components for voltage and current measurement, and for voltage and current control. Material costs are below $100, even though a separate probe station needs to be available when the FET sensors need to be probed at the die level. The interface side of our hardware is flexible enough to be adapted to a variety of DAC cards or data

 doi:10.20944/preprints202403.1169.v1

loggers. We demonstrate the performance of our device in a variety of contexts with conventional components to highlight its functions and with graphene FET application examples.

2. Materials and Methods

2.1. Probe Station

The key measurement apparatus to be integrated with the SMU is a probe station that allows for contact with micron-sized electrode pads on the target DUT. The Signatone S-1160 Series 1160 Manual Probe Station (Signatone Corp. Gilroy, CA, USA) was selected for this purpose [12]. The probe station is designed for accurate analytical testing of the desired IV curve collection through the presence of a vertically adjustable conductive center chuck, 3 micro-positioners with rectilinear X-Y-Z motion capable of probing down to 1 micron attached magnetically to the stage and tungsten needle tips, a low power microscope with LED illumination for surface magnification up to 7.5X-50X, as well as a mounted probe triaxial connector panel. Our design allows the sensor semiconductors to be probed at the die level and at the chip level. As shown in Figure 2, the S-1160 connects to the acquisition electronics via three BNC connectors. These are connected with standard RG-58 BNC cables to our hardware.

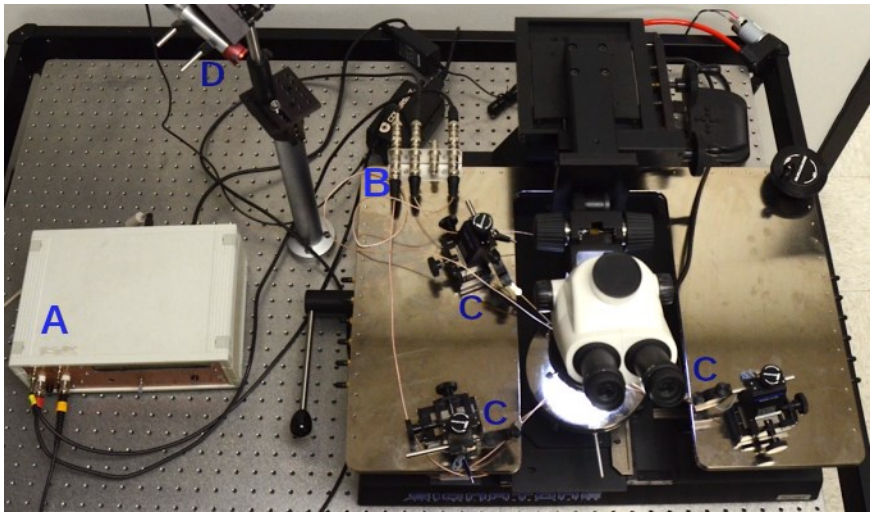


Figure 2. Photo of the semiconductor probe station connected to the source measure unit (SMU) hardware (A) presented in this paper. The probe station offers BNC terminals (B) for each contact micropositioner (C). A red laser (D) is mounted on a post and allows to illuminate the device under test with varying light flux levels.

2.2. Source Measure Unit (SMU)

2.2.1. Design Constraints

The first step towards design of the SMU was determining current and voltage ranges to be sourced and measured for graphene-channel FET. We also aimed at giving the device enough flexibility to be used on different types of FET sensors. To achieve a high level of flexibility, we decided on a symmetrical driver capable of applying both negative and positive polarity, which allows us to measure the characteristic curves of, for example, n- and p-channel FETs and NPN and PNP transistors, and to allow flexible choice of gate and drain voltage in FET sensors. Since one electrode is always the reference electrode (referred to as ground), three probes require two active and independent drivers. Both outputs, together with the reference ground, also comprise the three electrodes of a three-point measurement station. Whereas discrete transistors conduct comparatively high currents (several amperes for power transistors), the drain current for sensor FETs is typically in the order of several μA. We therefore decided to limit the voltage range to 10V to 10V and the current range to 100μA to 100μA. The range limits hold for both the active output and for the measurement range. The voltage range allows us to use conventional, off-the-shelf, symmetrical

 doi:10.20944/preprints202403.1169.v1

linear power supplies and, in our case, connect the SMU to the linear ±12V regulated power supply of the data logger. The choice of a linear supply was made to avoid switching noise. We also provided digitally-controlled, selectable gain for each probe station to further reduce the voltage and current ranges and better use the dynamic range of the digital-to-analog converters (DAC) and analog-to-digital converters (ADC).

2.2.2. Device Overview

The presented device is described in detail in this section. The hardware of the device was designed to be used in conjunction with general-purpose SMU hardware. Our lab is using a custom SMU, but any combined analog-digital interface system, such as National Instrument's DAC cards are suitable as acquisition back-ends. A schematic block diagram of the probe station hardware and its interface is shown in Figure 3. Two active channels A and B can be configured either as controlled-voltage or controlled-current sources, and their nominal output is determined by the control voltage V-CTL. Actual voltage and current are sensed at the probe output and provided as analog signals (V-OUT and I-OUT) that can be recorded by the SMU. In a typical configuration, a MOSFET source would be connected to BNC connector C, its drain to connector A, and the gate to connector B. The control voltage for Probe A is then swept repeatedly with varying voltage levels for the gate at connector B. The ability to configure a channel as controlled-current source was provided to extend the application range to non-FET semiconductors, including bipolar junction transistors, diodes, and even more exotic devices, such as, e.g., unijunction transistors. Moreover, sensor FETs often use very low V_{DS}, often in the upper mV range. In such a case, it is more accurate to impose a constant current and measure the voltage needed to drive this current.

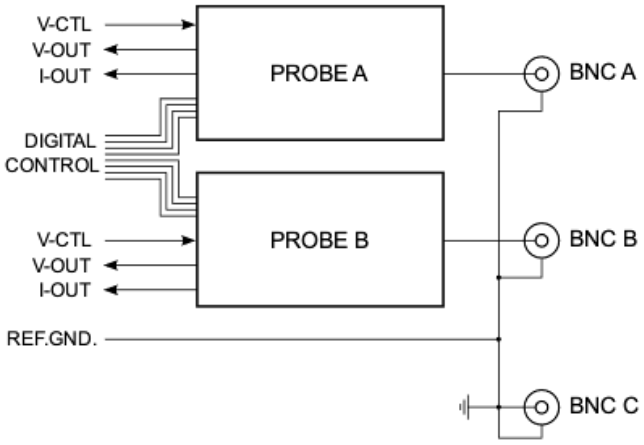


Figure 3. Overview of the probe station functional groups. Two identical active channels (A and B) serve either as a controlled voltage or current source with respect to the reference ground and probe C. Each channel's actual voltage and current are sensed and provided to the SMU.

A detailed functional block diagram for one of the two identical active probe channels is shown in Figure 4. At the center of each active probe channel is an amplifier that drives the load at the probe terminal. It is configured as a feedback amplifier that follows its input voltage either with the probe output voltage or with the voltage drop across Rs, which is proportional to the current, and which is sensed with an instrumentation amplifier. Analog electronic switches, each controlled with a digital signal, allow to select voltage- or current-controlled mode and allow to introduce different gain factors that determine the measurement range and allow to make full use of the SMU's dynamic range.

 doi:10.20944/preprints202403.1169.v1

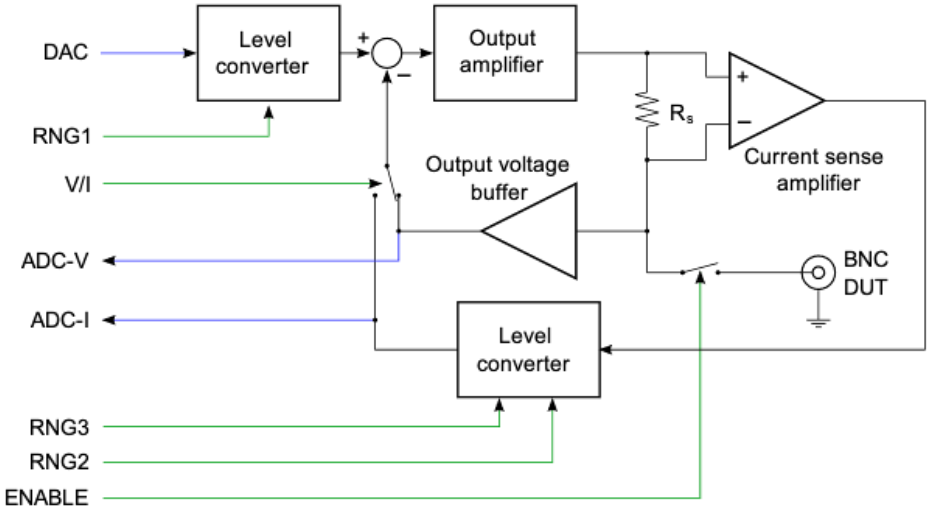


Figure 4. Detailed overview schematic of one of the two identical active channels. At the center is the output amplifier, which is configured in a feedback loop to either provide a controlled current or a controlled voltage. V- or I- mode is selected with an electronic switch. The current is sensed with the resistor Rs, and the proportional voltage is presented at the interface, as is the actual probe voltage. Additional digital signals allow selection of the current or voltage range, and a physical relay is provided to separate the device under test (DUT) from the circuit until it has been fully configured.

The interface to the SMU in Figure 4 is labeled with blue arrows for analog signals and green for digital signals. The interface is straightforward to connect to a vide range of SMUs or analog interface cards, and to further increase compatibility, the analog signals are level-shifted to a range from 0 to 5V, which can be provided by single-supply devices. The full circuit schematics are provided in the supplemental materials.

2.2.3. Modes

To make full use of a SMU's dynamic range, digital inputs allow to select one of several sensitivity ranges, which were implemented as part of the level shifter circuitry. For example, a voltage range of ±1.25V would be mapped to the ADC range of 0 to 5V with a gain of 2 and an offset of 2.5V. To measure the typically very low drain current in graphene-channel FET, our device is capable of delivering and measuring only up to ±100µA. The key factor in this design limitation is the sense resistor Rs with 2430 Ohms. The resulting high impedance also acts as a protective factor for the attached device under test, since it limits the maximum current to 10V/2430Ω = 4.1mA under worst-case circumstances. An overview of the modes and measurement ranges is provided in Table 1. It is noteworthy that the current limitation can be modified in a straightforward way: we placed the current sense resistor Rs in a socket. By replacing this resistor, the current range can be modified with low effort. For example, by using a resistor of 243Ω, the current sensitivity changes to ±1mA, ±250µA, ±50µA, and ±10µA, respectively. The upper limit is primarily imposed by the output driver, which is limited to approximately 20mA. In such a case, however, the device under test would be stressed with 200mW, which causes considerable power dissipation in a graphene channel. In fact, such power levels may already cause irreversible damage.

 doi:10.20944/preprints202403.1169.v1

Table 1. Current- and voltage controlled modes with built-in sensitivity ranges.

Combined control bits (binary)	Bit 0: Control mode	Bits 1, 2: Current sensitivity and range	Bit 3: Voltage range	Bit 4: Voltage sensitivity§	Resolution (per LSB), 12-bit DAC and ADC
10xx0	0 (voltage)	†	0: ±10V	(1)	4.88mV
01xx0			1: ±1.25V	(0)	0.61mV
x1001	1 (current)	00: ±100µA	‡	0: ±10V or 1: ±1.25V	48.8nA
x1011		01: ±25µA			12.2nA
x1101		10: ±5µA			2.44nA
x1111		11: ±1µA			0.49nA

† Can be combined with any of the current ranges below. ‡ Must be 1 (±1.25V) for current-controlled modes. § Must be opposite of Bit 3 in voltage-controlled modes. In current-controlled modes, either can be selected.

From the SMU perspective, the modes are presented as 5-bit groups of digital signals (Table 1). A combination of these bits allowed for different voltage and current ranges to be selected. For example, if the target DUT gate is driven with ±10V, the gate current, which should be zero, is monitored with the highest sensitivity (± 1µA) . The sweep range would be set to ±10V (+8), and the output range is also kept at ±10V (+0 in Bit 4). The highest current sensitivity is selected with binary '11' in bits 1 and 2 (+6), and Bit 0 remains 0 for the voltage-controlled mode. The sum is binary 01110, decimal 14 – this is the probe's mode.

Conversely, if trying to measure the I_D - V_{DS} curve with current control to obtain higher precision when the I-V curve becomes very steep while also limiting the current to 10µA with V_{DS} below 1V, the current-controlled mode would be selected (+1), and the current sweep range would be ±20µA (binary 01, +2). The voltage sweep range would be forced to ±1.25V by the firmware, and Bit 3 is not utilized (+0). The higher voltage sensitivity of ±1.25V with Bit 4 (+16) is selected, and the sum yields the bit pattern 10011, decimal 19. After determining the appropriate bit/mode relationship, calibrating them into the SMU program was the next step.

2.2.4. Calibration

Component tolerances require per-channel calibration. Calibration equations linearly map voltage or current values to unitless digital values. If we denote the digital value as Z, an analog value (for example, output voltage V_a of the active probe driver A) would be mapped through,

$$V_a = m_{a,M} \cdot Z + n_{a,M} \quad (1)$$

where $m_{a,M}$ is the slope for mode M (in this case, modes with voltage ranges of either ±10V or ±1.25V) and $n_{a,M}$ is the intercept. Component selection would allow to calculate theoretical values for the mapping equations. For example, to map a 12-bit digital value Z to the voltage range of ±1.25V, a slope of $m = 0.61\,\mathrm{mV/LSB}$ and an intercept of $n = -1.25\,\mathrm{V}$ would be expected. Due to component tolerances, deviations from the theoretical values can be expected, and a calibration regression provides more accurate values for the mapping slope and intercept.

We used a Keysight 34461A Digital Multimeter as reference and connected it between the probe output and ground. To calibrate each of the SMU's modes, different DAC values were input manually. The associated ADC read-out for both current and voltage was recorded. Actual voltage and current was then read from the Keysight 34461A digital multimeter and also recorded. For each mode, we collected 9 data points over the whole range of digital values (from 0 to 4095 in increments of 512) and performed linear regression to obtain slope and intercept. For each active probe, the calibration data set therefore contained six data pairs of slope and intercept for the ADC (two voltage ranges and four current ranges) and six data pairs for the DAC.

 doi:10.20944/preprints202403.1169.v1

Applying the digital data words and converting the digital read-out to actual V and I values is the task of the SMU back-end, and the calibration data were programmed into the SMU. To apply a desired voltage V_a, Equation ***Error! Reference source not found.*** is inverted to provide the DAC value Z,

$$Z = m'_{a,M} \cdot V_a + n'_{a,M} \quad (2)$$

The SMU then reads both analog outputs (Figure *3*) and converts the digital values for voltage and current, Z_V and Z_I, to physical quantities through

$$V = m_M \cdot Z_V + n_M \quad (3)$$

And

$$I = m_M \cdot Z_I + n_M \quad (4)$$

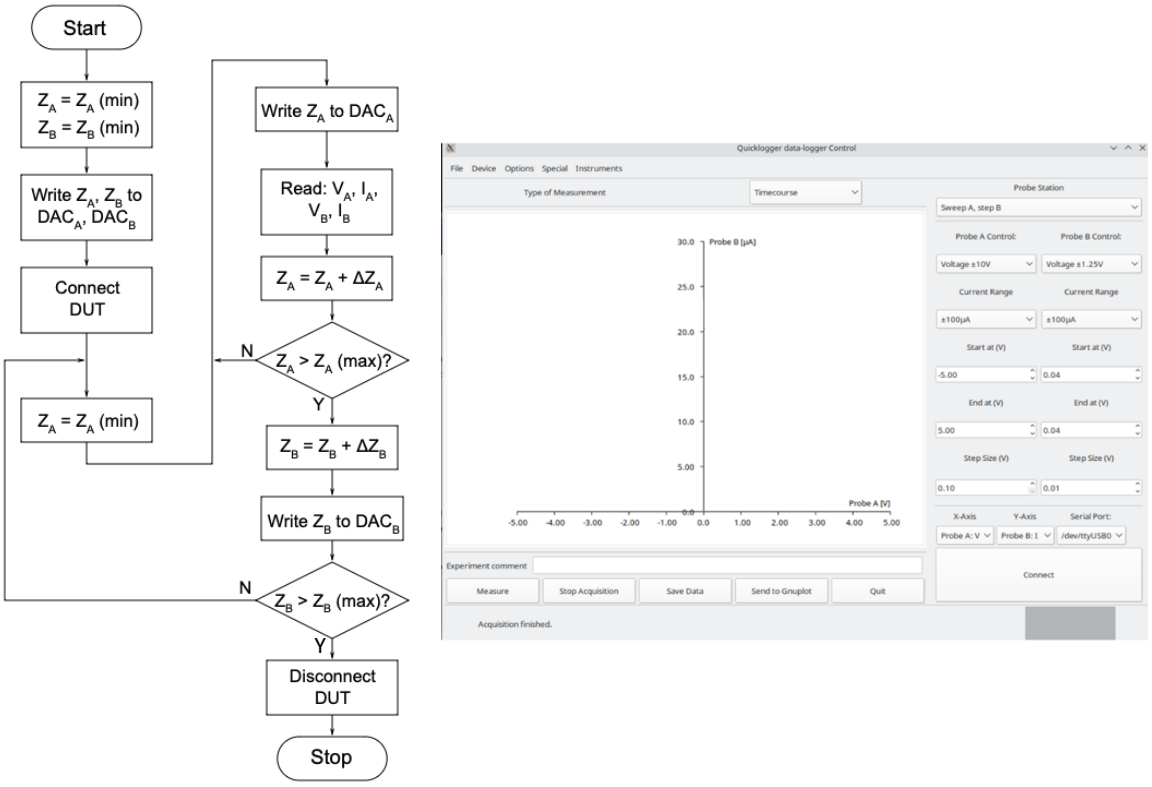
where again the index M stands for the mode.

2.3. Software Interface

To automate acquisition of the V-I curves, the SMU needs to be programmed with a measurement loop that successively applies voltage or current values to the probe outputs and then takes a measurement for each probe's actual voltage and current. Depending on the SMU, the automated measurement loop can be programmed through some form of macro language (e.g., LabView). In our case, it was added to the SMU's GUI software. A flow diagram is shown in Figure 5a.

As discussed with the linear regression used for calibration, Z represents the actual voltage or current that the SMU is set to, with ZA representing the inner loop and ZB representing the outer loop. After values have been input, the program reads the actual voltage and current of both probes for confirmation as the setpoint values may not be reached due to saturation. The step size, $\frac{\Delta}{Z'}$, is then applied, and the software is programmed to run through the inner then outer loop, replacing the present value until the set voltage or current value has been reached. Once the final value is detected, the DUT is disconnected from the SMU, and the process is complete. The associated GUI can be seen in Figure 5b.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 19 March 2024 doi:10.20944/preprints202403.1169.v1



(**a**) (**b**)

Figure 5. Software Interface for source and measurement control of the SMU data collection: (**a**) Flowchart; (**b**) GUI during Measurement. The controls shown on the right side of the GUI act as spin-dials to trigger the flowchart from start to end. Current ranges from ±100µA and voltage ranges from ±10V.

2.4. Data Collection

The features of the SMU software and hardware allow for the key data collection required by the target DUT: V_{DS} v I_D and V_{GS} v I_D curves. The device setup allows for a flexible selection of looking at current or voltage data for Probe A or Probe B before or after each measurement. As discussed, current and voltage can be set to various source and measurement range modes for greater accuracy. Probe A is set for a continuous measurement while Probe B is set to collect a different curve per input at the specified step sizes and can be set to a constant if only 1 curve is desired. The data collected can be exported as a raw data file with 4 columns associated with Probe A voltage/current and Probe B voltage/current. It can also be exported through gnuplot for quick data visualization.

For each test run, the modes for voltage and current are selected prior to inputting the start/end ranges and step size for the voltage or current supply. For V_{GS} v I_D, Probe A is connected to gate with Probe B connected to drain and GND connected to source; Probe A is set to sweep across negative and positive voltage ranges for ambipolar curve visualization while Probe B is set to a constant voltage. For V_{DS} v I_D, Probe A is set to sweep across varying voltage ranges used as constants during V_{GS} v I_D collection while Probe B is set to step across different voltages to observe curve variation. Voltage is reflected on the y-axis with current on the x-axis, and leakage currents can be checked by selecting different probe I/V options to be reflected on the GUI measurement plane. Additional expected behavior for transfer and output characterization can be found in the results and discussion section below.

 doi:10.20944/preprints202403.1169.v1

3. Results and Discussion

3.1. Source Measure Unit (SMU) Functionality Testing

The basic function of acquiring V-I curves was first tested with standard electronic components with known responses. For semiconductors, the measaured response was cross-referenced with its datasheet containing the identified curve behavior. The first device used was a 1 MΩ resistor used to verify the calibration discussed in the previous section before investigating more complex components. The resistor was tested for Probe A and Probe B at each current and voltage mode: Voltage Mode 8/16 + Current Mode 1/3/5/7 for a total of 16 tests. In accordance with Ohm's law, the expected response for each MΩ resistor test was a linear curve through the origin with a slope of 1. As exemplified in Figure 6, when testing the 1 MΩ resistor across Probe A and GND for Mode 8 (Voltage control = +/- 10V) and Mode 5 (Current range = +/- 5 μA), a linear curve from -5V to 5V and -5 μA to 5 μA through the origin with a slope of 1 was the result, confirming data logger functionality and validating calibration. The same data was collected for the remaining modes and Probe B.

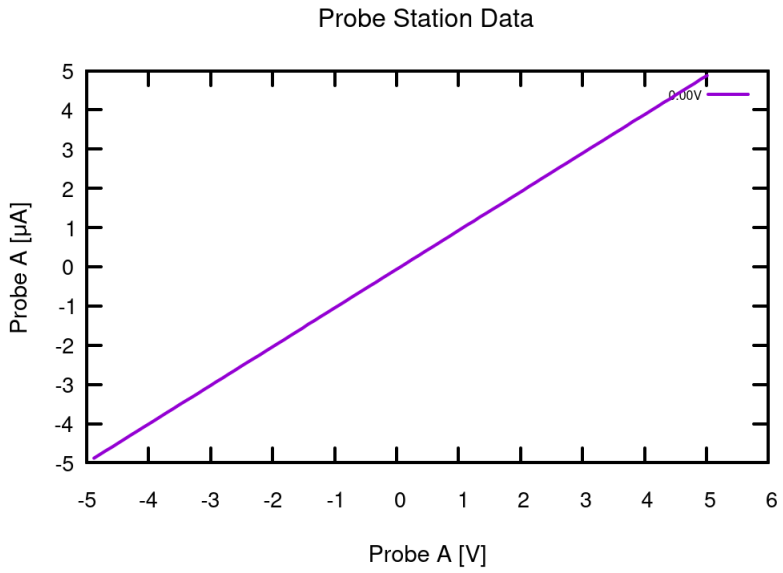
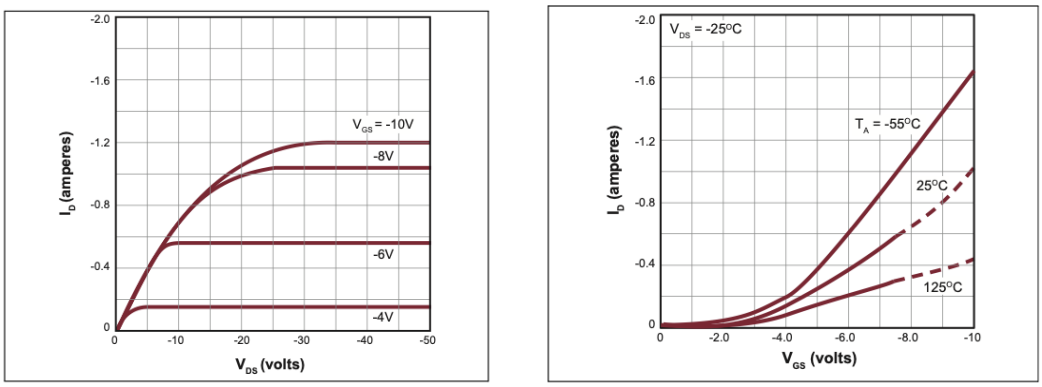


Figure 6. 1 MΩ Resistor Test. The IV curve shows the expected linear behavior of the resistor through the origin with a slope of 1 (spanning across ±5μA – Current Mode 5) based on an input of ±5V (Voltage Mode 8). The response validated the calibration and SMU functionality to allow for additional testing.

Based on the data collected for the 1 MΩ resistor in Figure 6, the signal-to-noise ratio (SNR) was calculated using the voltage and current values from Probe A. The SMU was proven to have an excellent SNR of about 63 dB, making it comparable to commercial devices on the market. After the 1 MΩ resistor testing confirmed that the SMU was functioning properly, active components were introduced to observe whether the device could accurately measure their expected output characteristics as well. The first device tested was the TP2540, a low-threshold p-channel enhancement-mode transistor with a vertical DMOS structure [14]. This device is known for its high current carrying capacity; therefore, a 1 MΩ resistor was placed between the drain electrode and associated probe for data collection due to the SMU's 100 μA maximum current range, specified for the target DUT. The effect of the resistor can be seen on the output curves, demonstrating the device's sensitivity. The datasheet for this component was referenced to identify the general transfer characteristics for the device, as seen in Figure 7.

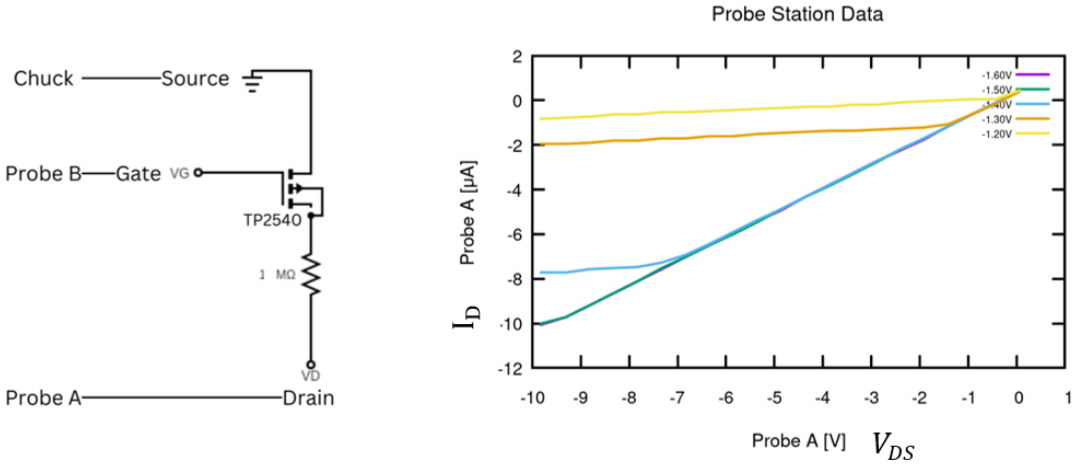
Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 19 March 2024 doi:10.20944/preprints202403.1169.v1



(**a**) (**b**)

Figure 7. TP2450 p-channel MOSFET Datasheet for Output and Transfer Characteristics [14]: (**a**) Output Characteristics; (**b**) Transfer Characteristics. The IV curves serve as the gold standard for the measurements collected in Figures 8 and 9.

The SMU was first used to confirm the I_D v V_{GS} and I_D v V_{DS} curves for the TP2540. For the I_D v V_{DS} curves, the output characteristics were measured by looking at I_D across V_{DS} over various V_{GS} values. Probe A was connected to a 1 MΩ resistor then to the drain and set to Mode 8 for observation of V_{DS} from -10V to 0V and current range Mode 3, +/- 20 μA, the calculated range for the output response. As mentioned, the 1 MΩ resistor was used to decrease the overall current output so that it was in a range that the SMU was capable of measuring since the target DUT utilizes the μA range. Probe B was attached to the gate and set to Mode 8 to observe V_{GS} at -1.6V, -1.5V, -1.4V, -1.3V and -1.2V, by inputting the voltage range as -1.6V to -1.2V with a step size of 0.1V. These V_{DS}values were selected in order to achieve this max current for testing device capability, and current range Mode 3 was again utilized. Probe A voltage (V_{DS}) was reflected on the x-axis and Probe A current (I_D) was reflected on the y-axis. As seen in Figure 8, the device was able to accurately measure the V_{GS} curves with the same overall behavior at lower current levels due to resistor impact.

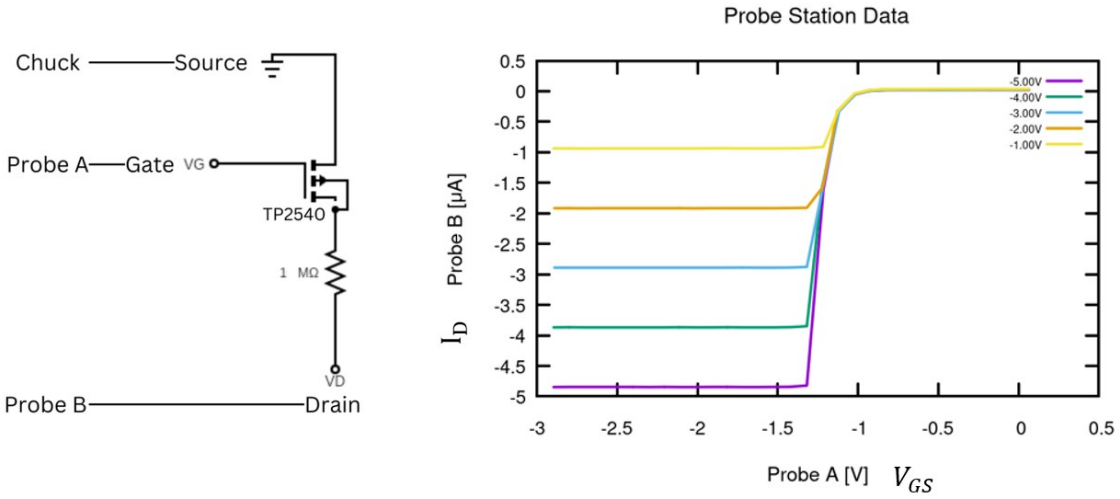


(**a**) (**b**)

Figure 8. TP2540 P-Channel MOSFET using SMU. (**a**) Schematic for V_{DS} v I_D Curve. The source is connected to the SMU ground, Probe B is connected to the MOSFET gate, and Probe A is connected to the MOSFET drain. A 1 MΩ resistor was attached across drain and Probe A to limit the current to the SMU max range; (**b**) V_{DS} v I_D Curve. The collected curve was compared to the datasheet in Figure 7 to confirm device accuracy.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 19 March 2024 doi:10.20944/preprints202403.1169.v1

Following the output characterization of the TP2540, the transfer characteristics were collected for the I_D v V_{GS} curve, identified from the vertical cross section of the I_D v V_{DS} plot to ensure measurements were taken across adequate voltage ranges. Probe A was attached to the gate at Mode 8 to test from -3V_{GS} to 0V_{GS}, as selected from the I_D v V_{DS} curves, and Mode 5 for an expected current range of +/-5 μA. Probe B was attached to the 1 MΩ resistor for the discussed current suppression then to the drain at Mode 8 to test across -5V_{DS} to -1V_{DS} at 1V step size, with current range set to Mode 5. Probe A was set for the x-axis voltage (V_{GS}), while Probe B was set for the y-axis current (I_D). As seen in Figure 9, the effect of the resistor is prominent, as seen by the steep L-shaped bend in the V_{DS} curves. Without the presence of this additional resistance, the curves would continue to the maximum I_D the device is capable of measuring at +/- 100 μA, as observed by the datasheet. This confirms the device's ability to accurately measure the V_{GS} v I_D curve needed for future DUT data collection within programmed parameters. After testing both passive and active components with the SMU, device functionality at low resolution was confirmed across voltage and current modes; therefore, the next step prior to target DUT data collection was integrating the SMU with a probe station to confirm testing integrity with an open-face BJT IC, as described in the section below.



(**a**) (**b**)

Figure 9. TP2540 P-Channel MOSFET using SMU. **(a)**The source is connected to the SMU ground, Probe B is connected to the MOSFET drain, and Probe A is connected to the MOSFET gate. A 1 MΩ resistor was attached across drain and Probe A to limit the current to the SMU max range; (**b**) V_{GS} v I_D Curve. The collected curve was compared to the datasheet in Figure 7 to confirm device accuracy.

3.2. Source Measure Unit (SMU) and Probe Station Integration Testing

The SMU was integrated with a 3-point probe station using the BNC connection ports located on the probe station's base in order to ensure the sensitivity of the SMU was still high when the probe station tungsten tips were used as the data collection points of contact rather than traditional cables. A bipolar junction transistor (BJT) IC was utilized as the DUT for this purpose, carefully sawing off the top of the protective shielding to be able to access the base and emitter terminals on the surface. Prior to testing, the exact device was unknown; however, the SMU was used to identify BJT behavior, with NPN vs PNP structure investigated below. The DUT can be seen in Figure 10, the inside of the star-like shape is the emitter, the outside is the base, and the collector is the exterior of the device. For the test setup, one probe was allocated to the base and emitter terminals, with the final probe touching the probe station's grounded chuck as the contact between the component and chuck with the SMU's ground port allows for the collector to be assigned to GND.

 doi:10.20944/preprints202403.1169.v1

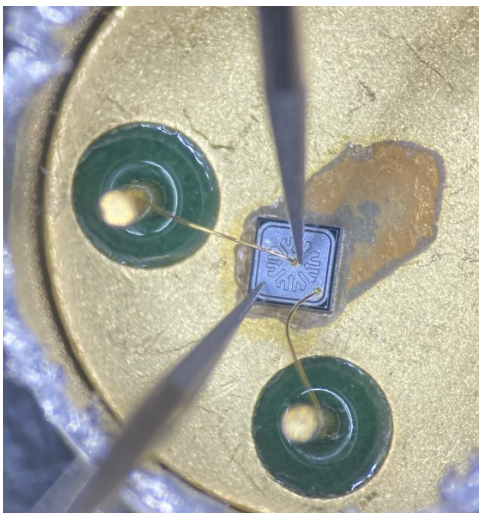


Figure 10. BJT IC DUT with Top of Shielding Removed. The BJT shielding was removed in order to probe the base (outside of star shape) and emitter (inside of star shape) to the SMU. The measurement was performed to test the integration of the SMU with the probe station.

Similar to the p-channel MOSFET testing, the first measurement carried out was the V_{GS} v I_D curve, in this case the V_{CE} v I_C curve, to gain insight of data collection points for the secondary curve measurements since the BJT operates by controlling the flow of current between the emitter and collector rather than source and drain. Another key difference is that the base is current-controlled rather than voltage-controlled seen with FETs as applying voltage across the base-emitter junction would weaken the built-in junction voltage in forward bias mode, eliminating the equilibrium between drift and diffusion currents; therefore, the base was set to current source mode to allow for the net flow of charge carriers across the BE junction to remain at zero [15] and higher current gain.

For the V_{CE} v I_C curve collection, the emitter terminal was connected to Probe A set to Mode 16 for +/-1.25V and Mode 1 for a current range of +/- 100 μA to capture the entire range of I_C curves generated at the following specified base currents. Probe B was connected to the base with Mode 1 also selected for the current range, but Mode 5 was selected for the source control to provide a base current of +/- 5 μA. To determine whether the device was a NPN or PNP BJT, negative values were first selected, keeping in mind the typical curve behavior of each type. The measured curves showed reverse polarity, resulting in the conclusion of a NPN structure as turning on a NPN BJT requires a base current that is more positive than the emitter with a positive voltage supply provided to collector rather than the PNP settings that were selected since NPN transistors use electrons as the majority charge carriers [15]. With this in mind, the settings were adjusted to provide Probe A (emitter) with 0V to 1V and Probe B (base) with 0 μA to 5 μA at 1 μA steps, with GND remaining connected to the chuck (collector). Probe A was set for the x-axis voltage (V_{CE}) and y-axis current (I_C).The resulting curve can be seen below in Figure 11, with the saturation region seen at about <0.3V_{CE}, active region at about 0.3V<V_{CE}<0.8V, and cut-off region below the -1 μA curve.

It should be noted that the maximum SMU current is set to read 100 μA, based on mentioned DUT design specifications; therefore, the 0 μA - 2 μA curves are somewhat cut off past 0.15 V_{CE}, once entering the active region, and remaining curves would be better reflected with 0.5 μA current steps. However, overall the BJT IC has similar low signal emission at lower base currents (-3 μA and -4 μA) to the target DUT, making it a great choice for SMU sensitivity testing at these I_B values. Taking the vertical cross section of the V_{BE} curves would result in the corresponding V_{BE} v I_C curve.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 19 March 2024 doi:10.20944/preprints202403.1169.v1

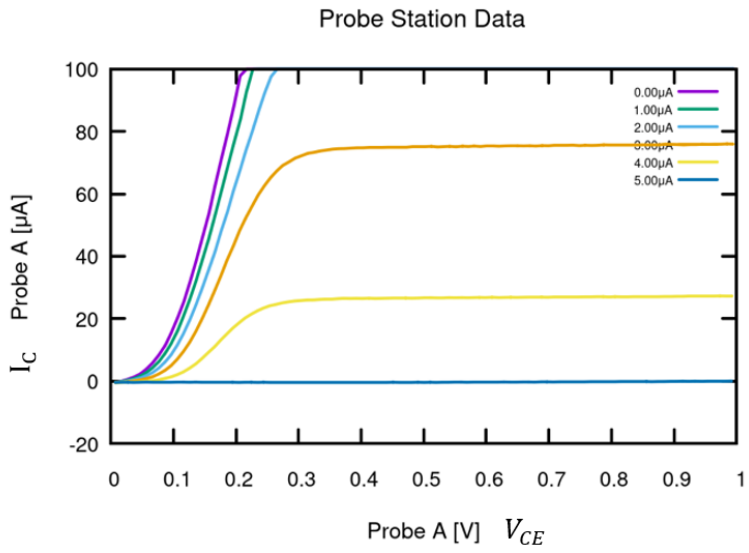
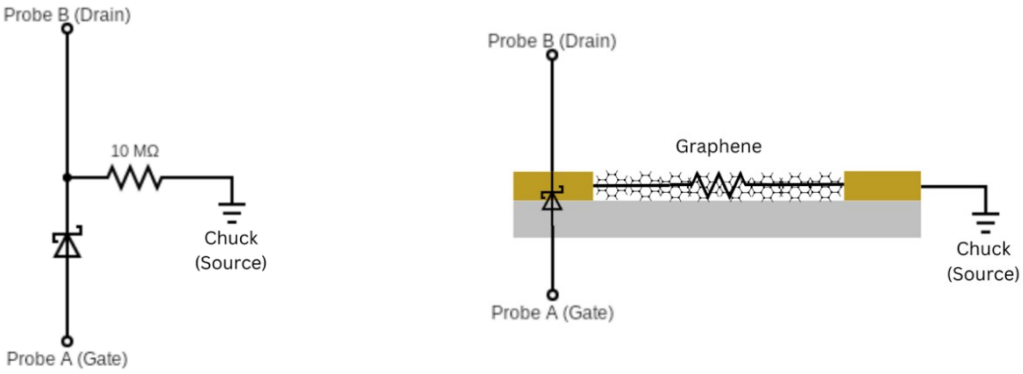


Figure 11. BJT IC V_{CE} v I_C. Probe A was connected to the emitter terminal with Probe B connected to the base and collector to GND. The curve was validated by comparing it to typical NPN BJT V_{CE} v I_C curve behavior.

3.3. Quality Testing: Accidental Schottky Junction Formed by Oxide Breakdown

Another example prior to testing the target DUT was a quality check to see if the device was capable of picking up errors with the graphene-FET structure. The DUT has metal source and drain electrodes on its surface with a metal back gate located underneath the insulating oxide layer. If the oxide layer were to be compromised, this would result in the metal source/drain electrodes to be in contact with the metal gate electrode creating a Schottky junction. The oxide could be compromised as a result of a fabrication error, probe punctures, or too high of a current through the gate channel; therefore, by testing the expected response for the Schottky junction, errors during DUT testing could be better diagnosed. The schematics for each can be seen in Figure 12.



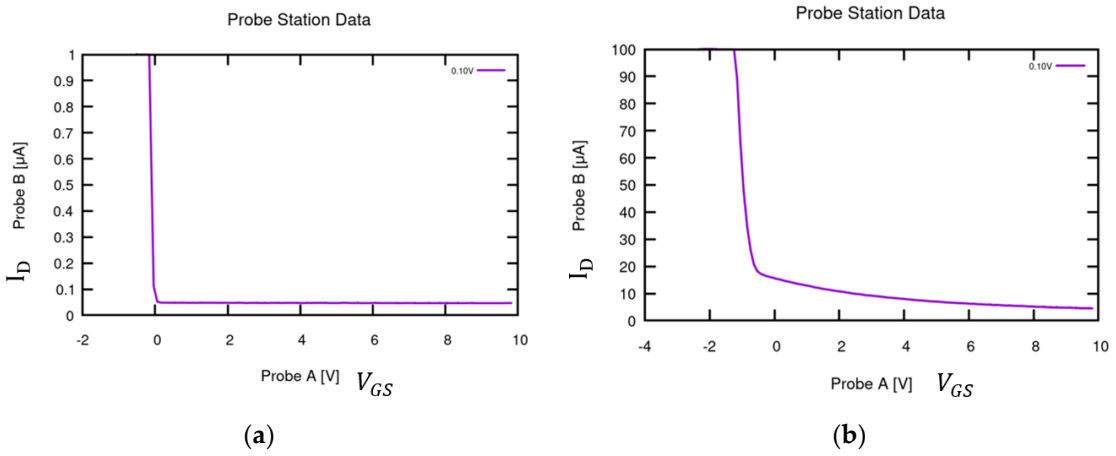
(**a**) (**b**)

Figure 12. Schottky Junction Test Schematics. (**a**) Testing schematic. A Schottky diode was connected to Probe A in reverse polarity, Probe B was connected to the other side of the diode and a 10 MΩ resistor which was also connected to GND; (**b**) DUT schematic. The graphene-channel FET with a breached oxide layer on the drain electrode was compared to the testing setup for quality testing. Probe A was connected to gate, Probe B to drain, and GND to source.

For the Schottky diode and resistor test, the gate was connected to Probe A and voltage Mode 8 from -10V to 10V at current Mode 7 (1 µA) with the Schottky diode in reverse polarity. The drain was connected to Probe B at voltage Mode 16 with a constant 0.1V and current Mode 7. As seen in the schematic, a 10 MΩ resistor was connected across drain and source, which was connected to GND

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 19 March 2024 doi:10.20944/preprints202403.1169.v1

through the probe station chuck in order to maintain a current in a range capable of device measurement and component parameters at 1 μA. Probe A was set for the x-axis voltage (V_{GS}), while Probe B was set for the y-axis current (I_D). The expected response can be seen in Figure 13a. The diode drains the current to the gate driver; the horizontal line shows the current through the resistor, and when the voltage is negative I_D shoots up the reach the current level that the gate is driving. The key insight provided by the test setup is that the diode conducts earlier than 0.7V much like the silicon of the target DUT back gate due to the exponential relationship between the diode voltage and current.



(**a**) (**b**)

Figure 13. Schottky Junction Quality Test Results. (**a**) Testing IV curve. The curve shows the steep increase in I_D to reach the current level that the gate is driving at the negative V_{GS} range on account of the Schottky diode; (**b**) DUT IV curve. The graphene-channel FET with breached oxide layer (Schottky junction) curve was compared to the testing curve in order to ensure that the results could be collected in the case of a structural device issue.

After the test was completed, it could be compared to a defect on one of the target DUT sensors, whose surface was punctured during a step of the fabrication process. The test setup above was replicated – gate was connected to Probe A and voltage Mode 8 from -10V to 10V at current Mode 7 (1 μA). The drain was connected to Probe B at voltage Mode 16 with a constant 0.1V and current Mode 7. The oxide breach was located on the drain electrode, as seen on the schematic in Figure 12(b), and the source electrode was connected to GND through the probe station chuck. Probe A was set for the x-axis voltage (V_{GS}), while Probe B was set for the y-axis current (I_D). The expected response can be seen in Figure 13(b). The curve shows the current shooting up right before the 0 V_{GS} mark seen during the test setup and drop down to ~0 μA by 10 V_{GS}. Now that device quality testing is complete, evaluating the target DUT is the next step.

3.4. Target DUT Testing

The graphene FET used as the target DUT was created using a p-doped silicon substrate with a thin oxide layer and gold source/drain electrodes on the sensor surface. The device has a back gate structure with a thin gold layer on top of the silicon serving as the gate and graphene across source and drain electrodes serving as the gate channel. The G-FET schematic can be seen in Figure 14.

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 19 March 2024 doi:10.20944/preprints202403.1169.v1

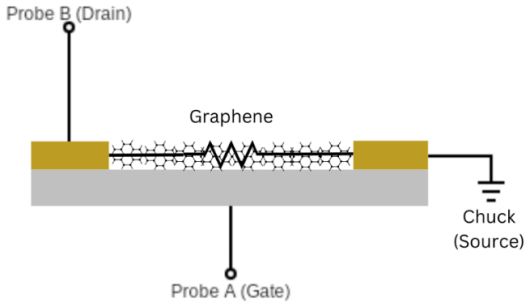


Figure 14. Graphene-channel FET Schematic. As seen in Figure 1, the graphene is located across the source and drain electrodes for analyte detection. For the V_{GS} v I_D curve, the gate is connected to Probe A, drain is connected to Probe B, and source is connected to GND.

As discussed, graphene FETs have ambipolar behavior in which holes are majority carriers in the negative V_{GS} region while electrons are majority carriers in the positive V_{GS} region. The expected V_{GS} curve is therefore a U-shape with the Dirac point located at the lowest I_D. In order to test the expected V_{GS} v I_D curve, the gate was connected to Probe A and voltage Mode 8 from -0.2V to 0.7V at current Mode 1 (100 μA) by placing the device on the probed chuck. The drain was connected to Probe B at voltage Mode 16 with a constant 0.2V and current Mode 1. Probe A was set for the x-axis voltage (V_{GS}), while Probe B was set for the y-axis current (I_D). The expected response can be seen in Figure 15, the Dirac point is located at ~0.25 V_{GS} at ~30 μA I_D. As discussed in the G-FET challenges, the ultra-sensitive nanoscale surface is reflecting noise caused by the uncontrollable nature of the graphene itself; however, the overall curve behavior remains [13].

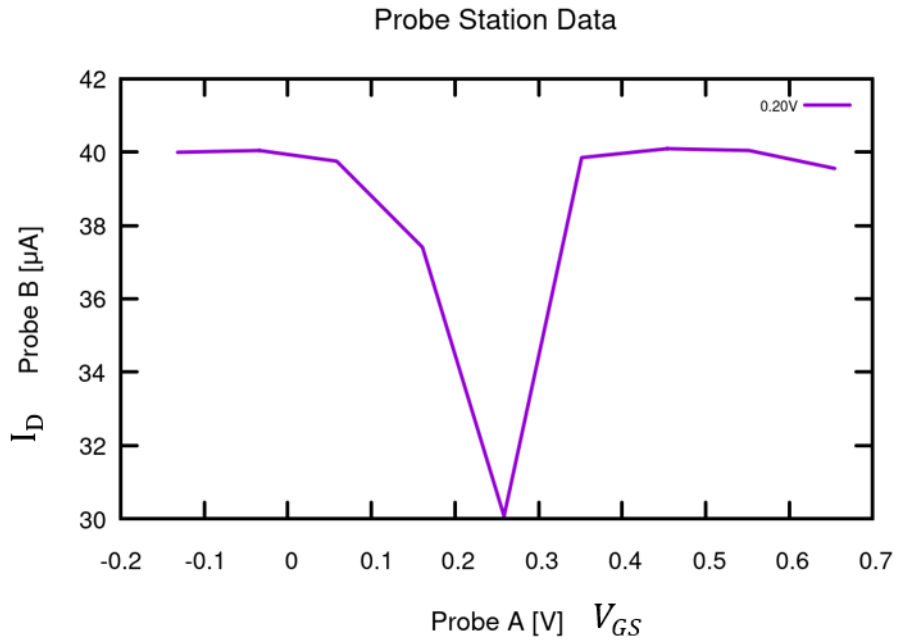


Figure 15. Graphene-channel FET V_{GS} v I_D Curve. The expected ambipolar response from the graphene channel is shown with a Dirac point at ~0.25 V_{GS} at ~30 μA I_D. The curve represents holes as majority carriers in the negative region and electrons in the positive region as current travels through the gate channel.

Photodetection is a key research area for improvement of FET optical sensing applications. Improvement of the sensing mechanism for these devices would allow for optical communication, remote sensing, spectrum analysis, biomedical imaging [16]. Researchers have investigated the

 doi:10.20944/preprints202403.1169.v1

transfer characteristic curves generated by photodetection on the G-FET surface, specifically that excitons are generated in graphene under various light conditions with response intensity influenced by symmetry in design and the wavelength of light source. These excitons are separated to electrons and holes near source and drain electrodes as a result of their corresponding electric fields [17]. For the design of the target DUT discussed here, the graphene was deposited closer to the source electrode, thus resulting in asymmetric behavior on the V_{GS} v I_D curve when compared to the control in Figure 15. This is due to the photovoltaic effect which generates increased photocurrents compared to a gate channel with symmetric orientation [17] at the site of asymmetry. Since the graphene is deposited closer to the source, the negative gate bias generated a stronger drain current and ambipolar response is no longer observed as the positive gate bias does not have an increased photocurrent. This leads to the conclusion that holes are the majority carriers present and reflected on the curve due to their relationship with the negative gate bias.

For testing, the same probe connections and test setup used for the control G-FET V_{GS} v I_D curve discussed above; however, a different device was used for repeatability purposes; therefore, a separate control V_{GS} v I_D curve was collected prior to laser illumination. Similar to the V_{GS} v I_D testing above, the gate was connected to Probe A and voltage Mode 8 from -1V to 4V at current Mode 1 (100 μA) by placing the device on the probed chuck. The drain was connected to Probe B at voltage Mode 16 with a constant 0.01V and current Mode 1. Probe A was set for the x-axis voltage (V_{GS}), while Probe B was set for the y-axis current (I_D). The expected response can be seen in Figure 16, the Dirac point is located at ~2.8 V_{GS} at ~2.3 μA I_D. The curve reveals that different devices have different responses, required V_{DS}, and noise presence based on the orientation and concentration of graphene in the gate channel. The Dirac point for this device in comparison to the first decreases by over 28 μA and is shifted to the right by over 2.5V.

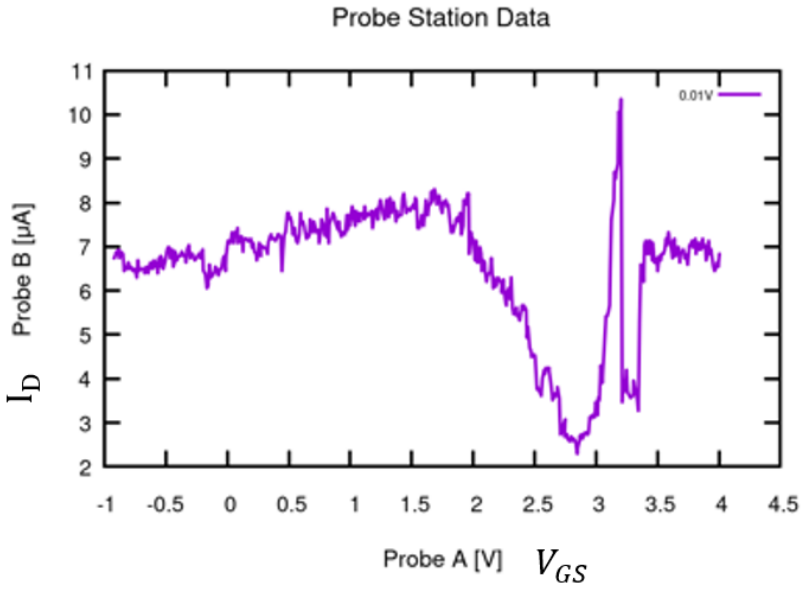


Figure 16. Graphene-channel FET V_{GS} v I_D Control Curve to Juxtapose against Laser Response. The curve shown in Figure 15 was recollected using a different device in order to confirm functionality and prepare for laser illumination testing. The Dirac point shifts to the right drops much lower than the first device tested (~2.8 V_{GS} at ~2.3 μA I_D).

Once the control curve for this device was collected, a 632nm, 0 - 10mW solid-state laser (Coherent LabLaser series, Coherent Corp., Saxonburg, PA, USA) was used and pointed at the surface of the device angled ~45°. The gate was connected to Probe A and voltage Mode 8 from -1V to 2.5V at current Mode 1 (100 μA) by placing the device on the probed chuck. The drain was connected to Probe B at voltage Mode 16 with a constant 0.01V and current Mode 1. Probe A was set for the x-axis voltage (V_{GS}), while Probe B was set for the y-axis current (I_D). The expected response can be seen in Figure 17, the Dirac point is not as present due to the asymmetric gate channel; however, the curve

Preprints.org (www.preprints.org) | NOT PEER-REVIEWED | Posted: 19 March 2024 doi:10.20944/preprints202403.1169.v1

seems to have a sharp decline at ~0.5 V_{GS} with similar noise present due to the sensitivity challenges of the G-FET itself. Additionally, the increase in I_D is extremely prominent in comparison to the control response, shifting upwards by ~48 μA due to electron excitation.

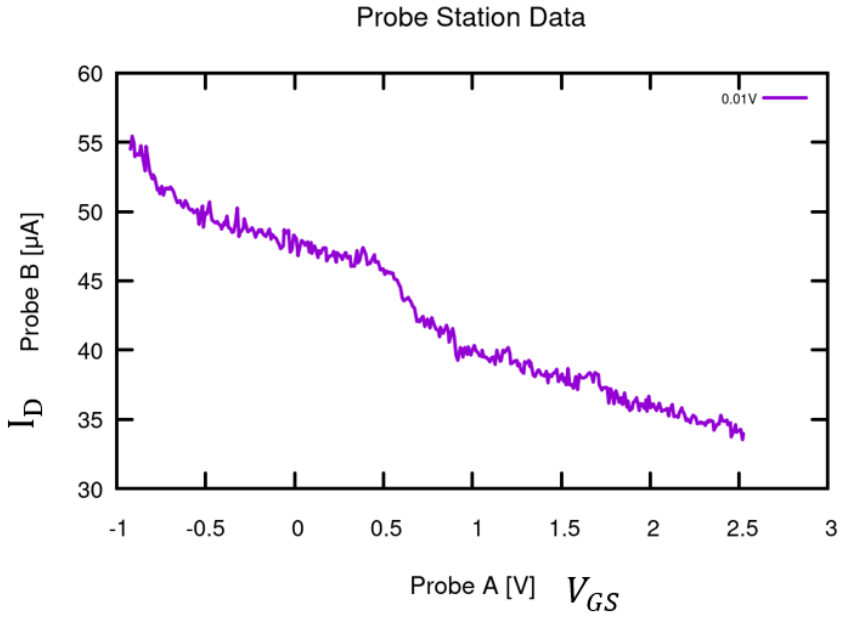


Figure 17. G-FET V_{GS} v I_D Curve Laser Response. The same device used in Figure 16 was used with a laser light of wavelength 632 nm illuminating the graphene channel. The excitation resulted in the response shifting upwards by ~48 μA.

The V_{DS} v I_D curve was collected next with the drain connected to Probe A and voltage Mode 16 from -1V to 0.5V and 0.5V steps at current Mode 1 (100 μA). The gate was connected to Probe B at voltage Mode 16 with from -0.5V to 0.5V and current Mode 1. Probe A was set for the x-axis voltage (V_{DS}) and y-axis current (I_D). The expected response can be seen in Figure 18, with variation between curves at about a 0.05V range. Due to the ultra-sensitivity of the device, challenges were presented in the data collection; however, with increased V_{GS}, the curves should continue to decrease then begin to increase again after passing the V_{GS} value associated with the Dirac point.

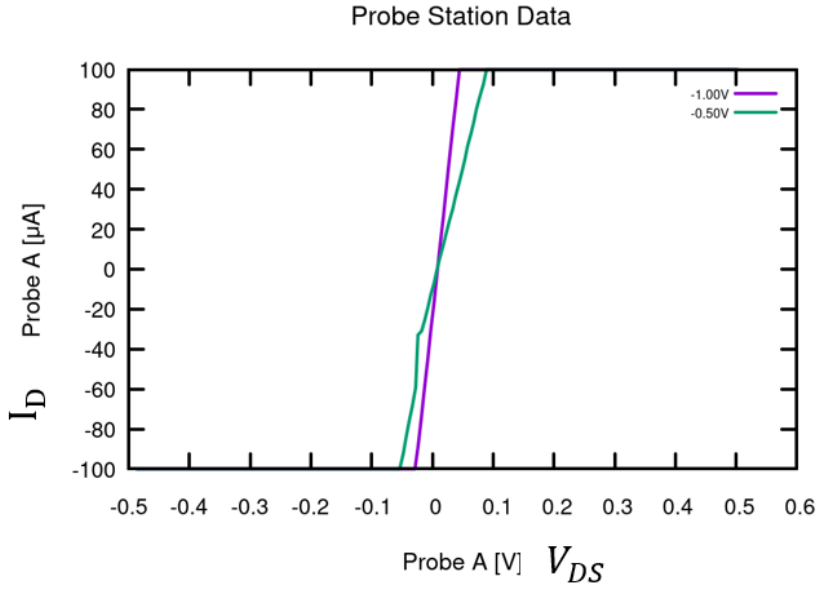


Figure 18. G-FET V_{DS} v I_D Curve. The curve shows slight variability across V_{DS} values as expected for graphene-channel FETs. The drain is connected to Probe A, gate is connected to Probe B, and source is connected to GND.

 doi:10.20944/preprints202403.1169.v1

4. Conclusions

As the nanomaterial-based FETs are growing in popularity due to their sensitivity and selective detection capabilities, graphene implementation has been largely investigated due to its tolerance for electron transfer through the entire FET structure, improving surface change response. Graphene-channel FETs utilize their sub-nanometric thick sensing layer to measure electric field changes deeper within the gate channel, substantially improving sensitivity. Additionally, the ease of recognition molecule attachment to the graphene channel surface allows for target analyte selectivity. The presence of noise in the form of undesired analyte attachment in part due to the ultra-sensitivity of the device has presented challenges in Graphene-FET development thus contributing to the need for a specialized measurement device that is tailored to its electrical characteristics. A source meter module has been presented to interface with a probe station for the Graphene-FET with optimized parameters at low cost. The device has shown the capability to measure responses in the sub-1 μA range, supported by curve collection for known devices prior to target DUT testing with an excellent SNR. Through the use of this device, the increase in I_D due to laser illumination was observed on the $\boldsymbol{V_{GS}}$ v I_D curve for the Graphene-FET device. Optical sensing through the use of Graphene-FETs has been proven with the construction of a specialized SMU, and future applications can be explored with the measurement device.

Author Contributions: M.H. designed and built the source measure unit prototype hardware and wrote the control software. A.G. provided the design criteria, performed calibration and testing, and acquired the data presented in the Results section. A.G. and M.H. about equally contributed to writing this manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The original contributions presented in the study are included in the article/Supplementary Material, further inquiries can be directed to the corresponding author/s.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Syedmoradi, L., Ahmadi, A., Norton, M. L., & Omidfar, K. A review on nanomaterial-based field effect transistor technology for biomarker detection. *Microchimica Acta* **2019**, *186*(11).
2. Geim, A. K. Graphene: Status and prospects. *Science* **2009**, *324*(5934), 1530–1534.
3. Kwong Hong Tsang, D., Lieberthal, T. J., Watts, C., Dunlop, I. E., Ramadan, S., del Rio Hernandez, A. E., & Klein, N. Chemically Functionalised Graphene FET Biosensor for the Label-free Sensing of Exosomes. *Scientific Reports* **2019**, *9*(1).
4. Chen, X., Pu, H., Fu, Z., Sui, X., Chang, J., Chen, J., & Mao, S. Real-time and Selective Detection of Nitrates in Water using Graphene-based Field-effect Transistor Sensors. *Environmental Science: Nano* **2018**, *5*(8), 1990–1999.
5. Sengupta, J., & Hussain, C. M. Graphene-based Field-effect Transistor Biosensors for the Rapid Detection and Analysis of Viruses: A Perspective in View of Covid-19. *Carbon Trends* **2021**, *2*, 100011.
6. Kim, J. E., No, Y. H., Kim, J. N., Shin, Y. S., Kang, W. T., Kim, Y. R., Kim, K. N., Kim, Y. H., & Yu, W. J. Highly Sensitive Graphene Biosensor by Monomolecular Self-assembly of Receptors on Graphene Surface. *Applied Physics Letters* **2017**, *110*(20).
7. Kitadai, H., Yuan, M., Ma, Y., & Ling, X. Graphene-based Environmental Sensors: Electrical and Optical Devices. *Molecules* **2021**, *26*(8), 2165.
8. De Sanctis, A., Mehew, J., Craciun, M., & Russo, S. Graphene-Based Light Sensing: Fabrication, Characterisation, Physical Properties, and Performance. *Materials* **2018**, *11*(9), 1762.
9. Patil, A., Koybasi, O., Lopez, G., Foxe, M., Childres, I., Roecker, C., Boguski, J., Gu, J., Bolen, M. L., Capano, M. A., Jovanovic, I., Ye, P., & Chen, Y. P. Graphene Field Effect Transistor as Radiation Sensor. In Proceedings of the 2011 IEEE Nuclear Science Symposium Conference, Valencia, Spain, 23-29 October 2011.
10. Foxe, M., Lopez, G., Childres, I., Jalilian, R., Patil, A., Roecker, C., Boguski, J., Jovanovic, I., & Chen, Y. P. Graphene Field-effect Transistors on Undoped Semiconductor Substrates for Radiation Detection. *IEEE Transactions on Nanotechnology* **2012**, *11*(3), 581–587.
11. Ono, T., Okuda, S., Ushiba, S., Kanai, Y., & Matsumoto, K. Challenges for Field-Effect-Transistor-Based Graphene Biosensors. *Materials* **2024**, *17*(2), 333.

 doi:10.20944/preprints202403.1169.v1

12. Signatone. Available online: https://signatone.com/static/6cf63861cc95452ca1cea5d8e6bb9257/s-1160-data-sheet-v1.5.pdf (accessed on 5 March 2024)
13. Rodriguez, S., Vaziri, S., Smith, A., Fregonese, S., Ostling, M., Lemme, M. C., & Rusu, A. A comprehensive graphene FET model for circuit design. *IEEE Transactions on Electron Devices* **2014**, *61*(4), 1199–1206.
14. Microchip. Available Online: https://ww1.microchip.com/downloads/en/DeviceDoc/TP2540-P-Channel-Enhancement-Mode-Vertical-DMOS-FET-Data-Sheet-20006371A.pdf
15. Nowlin, R. N., Enlow, E. W., Schrimpf, R. D., & Combs, W. E. Trends in the total-dose response of modern bipolar transistors. *IEEE Transactions on Nuclear Science* **1992**, *39*(6), 2026–2035.
16. Lemme, M. C., Koppens, F. H., Falk, A. L., Rudner, M. S., Park, H., Levitov, L. S., & Marcus, C. M. Gate-activated photoresponse in a graphene P–N junction. *Nano Letters* **2011**, *11*(10), 4134–4137.
17. Li, J., Niu, L., Zheng, Z., & Yan, F. Photosensitive graphene transistors. *Advanced Materials* **2014**, *26*(31), 5239–5273.