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*Article*

# Modeling, Simulation, and Experimental Validation of Broad Input Output Range Three Voltage Level Rectifier

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**Abstract:** A power factor correction (PFC) rectifier is compulsory for any electronic circuitry connected to the electrical grid. The majority of PFCs that are utilized are based on a step-up converter that supplies high DC voltage at its output terminal. Electric vehicle battery voltage varies from a few hundred to almost a thousand volts. Thus, an additional conversion step is obligatory when designing an all-brand universal charger. This paper presents a new type of front-end versatile step up / down three voltage level PFC. The rectifier can operate in continuous conduction mode or discontinuous conduction mode. First, the rectifier's principle of operation is described, and then an innovative rectifier is analyzed for continuous and discontinuous conduction modes. Finally, the proposed theory is experimentally validated in a multiplier-less dual loop mode at discontinuous conduction modes. It was shown that although there is no multiplier use in the control circuitry, the power factor is near unity. It was revealed that the rectifier could swing the output voltage from 50 V to 900 V while the input voltage was 230 Vrms. The innovative topology suits any standard PFC rectifier, three-level voltage supplement, and dual-stage low-voltage power supply.

**Keywords:** AC-DC; EV charger; power factor correction; rectifier; three voltage levels

## 1. Introduction

Rectifiers are a primary tool for delivering electrical energy from the electric grid to the local consumer by converting AC voltage to DC voltage. Most switch mode power converter topologies can be utilized as a single-phase PFC rectifier [1]. The basic idea is to impose a pure resistance input impedance at the rectifier input terminal. Thus, the rectifier is required to operate continuously to keep a near unity power factor and eliminate all harmonics. This principle of operation is valid for single-phase or three-phase rectifiers [2]. The boost converter is the most widespread rectifier; still, it imposes a minimum DC bus voltage of ~375 V (to preserve continuous operation at the maximum amplitude of the sine wave). Most residential and commercial loads are electronic circuitry that consumes DC power. However, the grid supplies average and pulsating power components; therefore, an additional element is required to balance the power equation. The electrolyte capacitor is commonly used as a PFC output terminal balancer. This element is responsible for about thirty percent of PFC failure [3] due to heat and high average operating voltage with ripple. Nevertheless, this issue could be addressed by implementing an electronic capacitor [4]. The boost rectifier [1] is highly efficient, low-cost, and relatively simple. Nonetheless, a typical single-phase load consumes energy under a certain (much lower) voltage supply and consequently requires an additional conversion stage. As a result, the cost, volume, weight, and efficiency are negatively affected.

The buck is a step-down converter that may solve the necessity for lower voltage applications. In this topology, the output voltage must be lower than the input source voltage. Thus, the buck rectifier cannot sustain continuous operation throughout the line cycle [1], and the input current is discontinued. Therefore, it cannot maintain the required power factor and total harmonic distortion. The buck-boost rectifier, by contrast, is much more versatile since it supports a voltage step-up and step-down; consequently, a wide output voltage range is available. Nevertheless, a buck-boost rectifier is relatively less efficient; the reversing output voltage can cause a conflict with the neutral point, and the inductor peak current is higher than in a similar power boost rectifier [1]. The Vienna rectifier introduced a new approach for three-phase rectifiers. Compared with a conventional two-level converter system, the three-level Vienna rectifier reduces the voltage stress on power semi-conductors and the rated power of inductance connected on the side of the mains. The three-level DC bus is more applicable for inverters since the three-level inverter enables higher efficiencies and better harmonics immunity referring to two-level inverters [5]. However, the Vienna rectifier's output voltage is twice as high as a standard boost PFC rectifier with bus voltages of  $\sim 400$  V, 0 V (neutral), and  $\sim +400$  V. This rectifier type may fit applications such as low harmonics three-level inverters and high-voltage, high-power electric motors. Applications with low-power motors, such as air-conditioners, refrigerators, etc., may require lower amplitude sine waves, where the high-voltage three-level DC bus reduces the resolution; therefore, the accuracy of the inverter may also harm the inverter's efficiency. In such a case, an additional conversion step is the preferred option for decreasing the DC bus voltage. The emergence of electric vehicles (EVs) brought new challenges for power electronics engineers and pushed the battery energy density limits to new levels; although optimization of battery size was made [6], the battery capacity remains over tens of kilo watts hours and requires powerful chargers [7–9]. Nonetheless, applications with low-power motors, such as air-conditioners, refrigerators, etc., may require lower amplitude sine wave, where the high-voltage three-level DC bus reduces the resolution and, therefore, the accuracy of the inverter and may also harm the inverter's efficiency. The nominal charging voltage in EV applications varies between 1000 V and 100 V [1,10]. Thus, the available rectifiers can't support universal charging in a single conversion step. A wide output voltage range could be achieved by utilizing an additional conversion step; however, overall efficiency is negatively affected. Moreover, the system cost, volume, weight, and component failure rate increase when employing two-stage conversion.

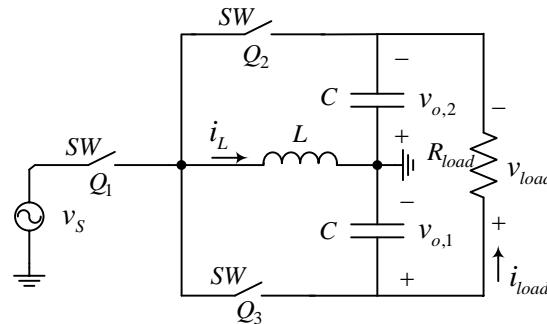
The contribution of this paper compared to [11,12] is as follows.

- Unlike [11,12], where the rectifier runs in open-loop mode, a dual-loop controller (for the inductor current and output voltage) was implemented here;
- Experimental results are given in this paper ([11,12] was accompanied by simulation only); it was shown that some of the results reported in [11,12] could be more unachievable as a result of practical driving limitations;
- Elaboration on the optional utilization of the bi-directional switch and the analysis of the required control command for each case.
- The average current mode control method for DCM operation is implemented here;

This paper presents a new topology for a single-step universal three-level PFC rectifier (UTPR) operating in dual-loop mode. The output voltage range can deviate from 50 V up to 900 V while keeping the UTPR elements at half the size of a standard buck-boost rectifier. Unlike standard buck-boost [1,13], the UTPR creates three output voltage levels that directly fit three-level inverters for improved voltage total harmonic distortion (THD<sub>v</sub>). The UTPR employs fewer components than a standard dual-step converter. Therefore, the UTPR overall efficiency is higher, and the component count is lower than in a similar traditional system. The UTPR is relevant to applications such as EVs [14], battery storage systems [15], inverters [16,17], and front-end rectifiers [18]. First, the principles of operation and circuit analytics are introduced. Then, the UTPR circuit simulation and experimental results are provided, presenting the proposed circuit performance in a multiplier-less dual loop and validating the proposed theory of the innovative topology.

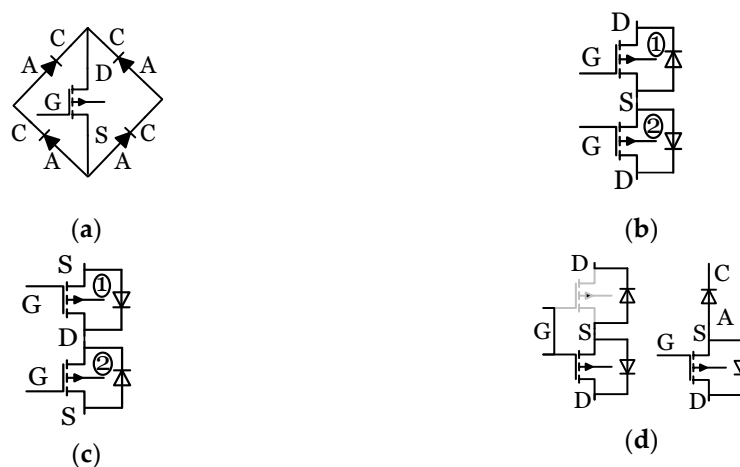
## 2. Circuit Topology and Analysis

In the meaning of the broad input and output voltage range of a three-level PFC rectifier, the UTPR can fulfill all required properties. The proposed rectifier can operate in a single phase for low to medium loads or a three-phase topology for high-power loads. The single-phase UTPR is based on one power inductor ( $L$ ), two storage capacitors ( $C$ ), and three bi-directional switches ( $SW$ ), as presented in Figure 1. The UTPR can operate in continuous conduction mode (CCM) [11,19] and discontinuous conduction mode (DCM) [12,20].



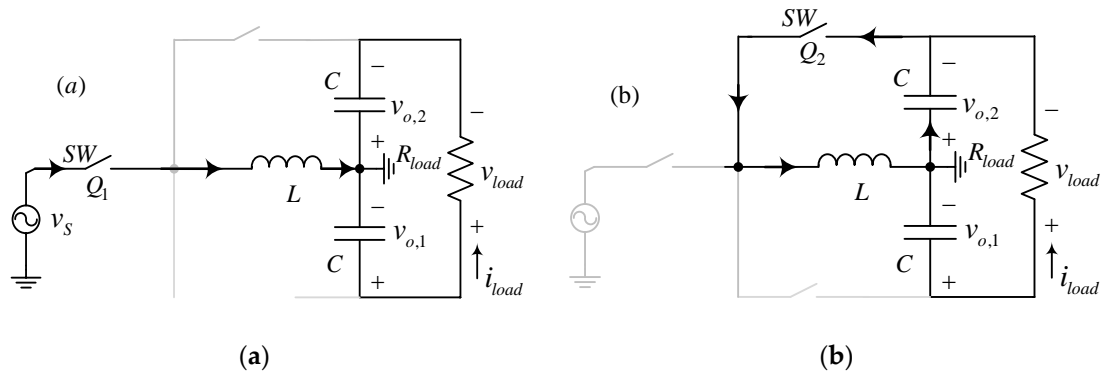
**Figure 1.** UTPR circuit.

Several methods could be employed for a bi-directional SW. The most straightforward technique for AC-connected SWs is by four diodes and a single Transistor (MOSFET, GaN FET, or IGBT). The diodes are connected in a rectifying fashion where the transistor drain is attached to the common cathode and the source to the common anode, as exhibited in Figure 2a. Another option is a series connection of two transistors with a common source or drain connection, as presented in Figure 2b and Figure 2c, respectively. In many applications, the switching timing sequence is crucial; consequently, particular logic circuitry or high computational switching effort is required. A possible solution is a semi-open bidirectional SW, where the opposing flow transistor is turned on before the inductor current is “looking” for a possible path; the second transistor anti-parallel diode blocks the unwanted flow. Next, when the inductor voltage reverses, the diode polarity turns ON and conducts (the SW is ON now). To reduce the losses, the active diode transistor can be turned ON. The same results could be achieved by a semi-open SW, where a drain of the transistor is series connected with the diode anode, as given in Figure 2d. The drawback of this switch is the unidirectional current flow; thus, its utilization is limited to specific cases.



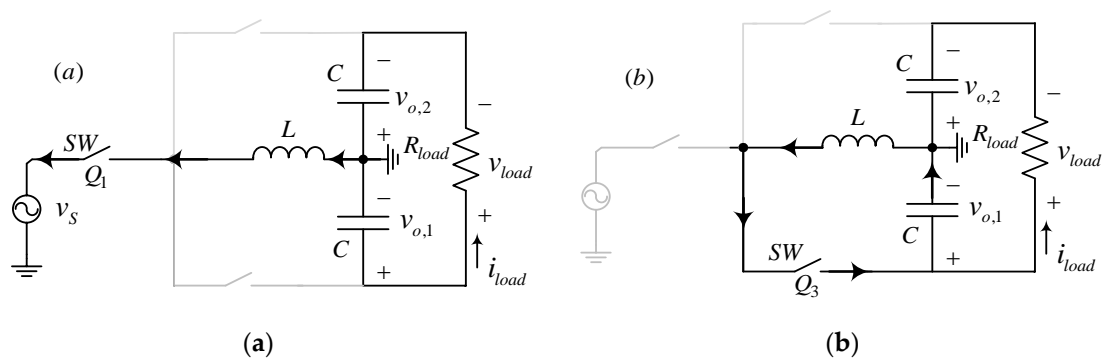
**Figure 2.** Implementation of the bidirectional SW (a) four diode and transistor; (b) common source two transistors; (c) common drain two transistors; (d) Semi-active transistor and diode.

The principle of operation for the positive half-sine wave includes a charging period and a discharging interval of the power inductor. The charge path (marked as (a)) begins at the AC source throughout the main SW ( $Q_1$  at the middle), goes to the power inductor, and goes back to the neutral, as presented in Figure 3a. The discharge path (marked as (b)) at the positive half-sine wave continues with the same current direction, discharging the inductor throughout the upper capacitor and the top SW ( $Q_2$ ). In the discharge period, the upper capacitor is charged within the current flow direction, as marked in Figure 3b. The logic signals for driving the SWs are as follows: the main SW ( $Q_1$ ) is governed by the PWM signal, and the upper SW ( $Q_2$ ) is ruled by the complementary PWM signal with the condition of operating in the sine positive half wave  $\overline{PWM} \& \text{sign}(v_s(t))$ .



**Figure 3.** The UTPR operates at grid positive half sine wave for an inductor (a) charging path and (b) discharging path.

In the negative half sinewave, the charge path (marked as (a)) begins at the neutral and goes through the power inductor, to the main SW ( $Q_1$ ), and back to the AC source, as exhibited in Figure 4a. The discharge path (marked as (b)) continues in the same direction as the current flow, discharging the inductor's stored energy through the bottom capacitor and the lower SW ( $Q_3$ ). The bottom capacitor is charged within the current flow direction, as marked in Figure 4b. The logic signals for driving the SWs are as follows: the PWM signal governs the main SW ( $Q_1$ ), the bottom SW ( $Q_3$ ) is controlled by the complementary PWM signal with the condition of operating in the sine negative half wave  $\overline{PWM} \& \text{sign}(v_s(t))$ .



**Figure 4.** The UTPR operates at grid negative half sine wave for an inductor (a) charging path and (b) dis-charging path.

As stated earlier, the bidirectional SW has multiple implementation methods. The components count, conduction losses, and static losses differ on each topology. The main SW ( $Q_1$  - connected to the source  $v_s$ ) could be implemented by the SWs from Figure 2a, Figure 2b, or Figure 2c (but not by Figure 2d). The static and dynamic losses and the control instructions for each case are presented in Table 1. The upper and lower SWs ( $Q_2$  and  $Q_3$ , respectively) are suitable to be utilized by all SWs from



Figure 2. The static and dynamic losses, alongside the control instructions for each case, are presented in Table 1.

**Table 1.** Control signals for different types of bidirectional SW utilization and losses per each case.

Title 1	Title 2	Title 3	Title 4	Title 5	Title 6	Title 7
Figure 2a	1 Transistor 4 Diodes	$I_{rms}r_{ds} + I_{avg}2V_D$	$Q_GV_Gf_{SV}$	PWM	$\overline{PWM} \& sign(v_s(t))$	$\overline{PWM} \& \overline{sign(v_s(t))}$
Figure 2b	2 Transistors	$2I_{rms}r_{ds}$	$2Q_GV_Gf_{SV}$	PWM	$\overline{PWM} \& sign(v_s(t))^{(2)}$ Or $\overline{PWM} \& sign(v_s(t))^{(2)}$ $\overline{PWM(-)} \& sign(v_s(t))^{(1)}$	$\overline{PWM} \& sign(v_s(t))^{(1)}$ Or $\overline{PWM} \& sign(v_s(t))^{(1)}$ $\overline{PWM(-)} \& sign(v_s(t))^{(2)}$
Figure 2c	2 Transistors	$2I_{rms}r_{ds}$	$2Q_GV_Gf_{SV}$	PWM	$\overline{PWM} \& sign(v_s(t))^{(1)}$ Or $\overline{PWM} \& sign(v_s(t))^{(1)}$ $\overline{PWM(-)} \& sign(v_s(t))^{(1)}$	$\overline{PWM} \& sign(v_s(t))^{(2)}$ Or $\overline{PWM} \& sign(v_s(t))^{(2)}$ $\overline{PWM(-)} \& sign(v_s(t))^{(1)}$
Figure 2d	2 Transistors Or 1 Transistor + 1 Diode	$I_{rms}r_{ds} + I_{avg}V_D$	$Q_GV_Gf_{SV}$	Not Applicati ve	$\overline{PWM} \& sign(v_s(t))$	$\overline{PWM} \& \overline{sign(v_s(t))}$

(\*) transistor number in Figure 2b and Figure 2c; (-) – is the PWM signal with a short delay to allow the antiparallel diode to start the conduction phase.

The analysis of UTPR is made for two operation modes, the CCM and the DCM. In CCM, the UTPR output voltage is in three-level mode, and the converter transfer function is:

$$v_{o,avg}/v_{s,rms} = -d_{rms}/(2 \cdot (1 - d_{rms})) \quad (1)$$

where  $v_{s,rms}$  is the input terminal connected to the electrical grid r.m.s voltage ( $v_s(t) = V_m \sin(\omega t)$ ), the  $2 \cdot v_{o,avg}$  is the load voltage (where  $v_{load,avg} = v_{o,1,avg} + v_{o,2,avg} = 2 \cdot v_{o,avg}$ ), and the  $d_{rms}$  is the rectifier's duty-cycle for r.m.s values. The inductor's current ripple is derived from the inductor voltage balance equation and from (1), where the current ripple is:

$$\Delta i_L = (v_{s,rms}/(L \cdot f_{sw})) \cdot 2 \cdot v_{o,avg}/(2 \cdot v_{o,avg} + v_{s,rms}) \quad (2)$$

where L is the inductance of the power inductor, and  $f_{sw}$  is the switching frequency. Thus, the average inductor current is:

$$\langle i_L \rangle_T = 2 \cdot v_{o,avg} \cdot i_{load,avg}/(d_{rms} \cdot v_{s,rms}) \quad (3)$$

where  $i_{load,avg}$  is the load average current ( $i_{load,avg} \cong i_{load,rms}$ ). Therefore, the inductor peak current is:

$$i_{L,m} = 2v_{o,avg} \cdot \left( \frac{i_{load,avg}}{d_{rms} \cdot v_{s,rms}} + \frac{v_{s,rms}}{L \cdot f_{sw} \cdot (2v_{o,avg} + v_{s,rms})} \right) \quad (4)$$

and the minimum inductor for CCM is

$$L_{crit} = (v_{s,rms} \cdot d_{rms})^2 / (4 \cdot f_{sw} \cdot P_{load}) \quad (5)$$

where  $L_{crit}$  is the inductor value of critical mode, and  $P_{load}$  is the average output load power. As for DCM, since the UTPR shares similar characteristics as the buck-boost converter, the input average current exhibits a perfect linear relationship with its input voltage given by

$$i_L = 4P_{load}/(v_{s,rms} \cdot d_{1,rms}) \quad (6)$$

where  $d_{1,rms}$  is the inductor's duty cycle for the conduction interval when operating at DCM for the r.m.s values. From power equality and (6), the converter transfer function is revealed in (7), where the DCM duty-cycle ( $d_1$ ) can be revealed.

$$v_{o,avg}/v_{s,rms} = -(d_{1,rms}/i_{load,avg}) \cdot \sqrt{P_{load}/(2 \cdot L \cdot f_{sw})} \quad (7)$$

In standard rectifiers, under the assumption of unity power factor, the output capacitor value is set by the following rules of power equality, where  $p_s(t)$  is the instantaneous input power, and  $p_c(t)$  is the instantaneous capacitor power:

$$p_s(t) = P_{load} + p_c(t) = P_{load} \cdot \frac{1}{2}(1 + \cos(2\omega t)) \quad (8)$$

The capacitor energy balance is derived from (8)

$$E_c = E_0 - P_{load}|\sin(2\omega t)|/(2\omega) \quad (9)$$

From (9), the capacitor value is revealed as

$$C_{ripple} = P_{load}/(4 \cdot \omega \cdot \Delta v_o \cdot v_{o,avg}) \quad (10)$$

where  $C_{ripple}$  is the rectifier output filter capacitor and  $\Delta v_o$  is the capacitor voltage ripple. Nevertheless, the UTPR operating principle resembles a single-phase Vienna rectifier [19]. Each capacitor on UTPR is charged only in a one-half cycle and supplies energy for a whole period, as presented in Figures 3 and 4. Both capacitors must contain a holdup energy for a half-cycle time to fulfill the energy requirements as shown in (11).

$$C_{h.up} = \pi \cdot P_{load}/(4 \cdot \omega \cdot \Delta v_o \cdot v_o) \quad (11)$$

where  $C_{h.up}$  is the capacitor holdup time. Thus, an increased output capacitance is mandatory to support the required output voltage ripple when employing a three-level rectifier. Applying a proportional integral and Notch voltage controller decreases output capacitance, as presented in [21]. The output capacitor is set by the maximum value of (10) and (11)

$$C = \max\{C_{ripple}, C_{h.up}\} \quad (12)$$

It is easy to obtain that the holdup capacitor is more significant than the ripple capacitor ( $C_{h.up} \gg C_{ripple}$ ); thus, the output capacitors are set by  $C_{h.up}$  value. Since a half-cycle energy hold-up time is a standardization requirement for every grid-connected system at a specific power rating, the capacity of UTPR or any other rectifier is equal. In the case of a three-phase rectifier, the low-frequency power signals are shifted at 120°, and the summation of all three voltage components is near zero ripple; thus, the required output capacitance is much lower than in a single phase.

### 3. UTPR Average Model and Control Approach

A cascade dual control loop [22] is a standard methodology to tackle converter stabilization tasks [23]. An internal loop to shape the inductor current for PFC properties creates a sinusoidal envelope shape and an external outer voltage loop for the rectifier output voltage adjustment, as presented in Figure 5. The rectifier output voltage contains a slight sinusoidal fluctuation at double line frequency; therefore, the controller output command ( $i_{ref}$ ) is a dc signal. However, the required current shape in the line frequency is sinusoidal; thus, an analog multiplier is necessary, as presented in Figure 5.

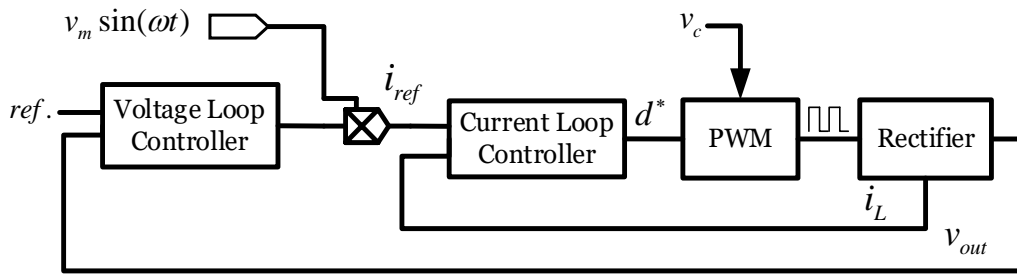


Figure 5. Standard rectifier control scheme.

The converter state equations present a non-linear system that is uncontrollable. The standard method to confront this issue is by transferring the converter's continuous form by utilizing an average model. It is important to note that this model describes each half-sine wave separately; however, since the overall circuit activity is the same, both circuits are presented as a single model in Figure 6. On the input side, the input voltage is marked as  $v_s$ , the  $r_s$  reflects the output active load multiplied by the operating point duty ratio divided by the square of the output-to-input voltage transfer function, and the last element is the average input current ( $\langle i_s \rangle_T$ ) multiply by the operating point duty ratio. The output side is affected by the input voltage multiplied by output to input voltage transfer function divided by the output active load, and the next element is the average input current multiplied by the operating point duty ratio; the other elements are the state operating capacitor ( $C_x$ ) according to the positive or negative sequence, and the output active load. A small signal state equation is accomplished by applying Kirchhoff's voltages and currents laws on the UTPR average model and splitting the parameters into intermediate components and perturbations. The state equations can be constructed by applying Kirchhoff's voltages and currents laws on the UTPR average model and separating the parameters into average components and perturbations.

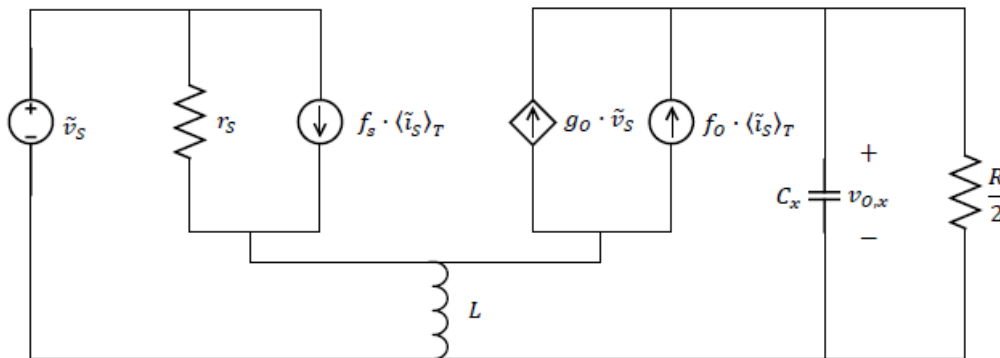


Figure 6. UTPR average model.

When operating in DCM in UTPR, the input current is a function of the input voltage and other parameters; thus, a self-PFC is an automatic outcome. Since the switching frequency is higher than the line frequency in several magnitudes, the line voltage is assumed to be almost constant in a single switching cycle. Under the steady-state operation assumption, the output voltage and the duty ratio variation are slight. By performing an analysis on the UTPR, the line average current and voltage present a perfect linear relationship, which proves that the UTPR has excellent self-PFC properties as given in (13). Consequently, the UTPR control schematics do not necessitate a multiplier, simplifying the control effort (analog or digital) and reducing the control circuitry cost.

$$\langle i_s(t) \rangle_T = (d_1^2 T_s \langle v_s(t) \rangle_T) / (2L) \quad (13)$$

The state equations can be constructed by applying Kirchhoff's voltages and currents laws on the UTPR. However, these state equations produce an uncontrollable non-linear system (with



common compensators). The standard method to confront this issue is by transferring the converter's continuous form using an average model. It is important to note that this model describes each half-sine wave separately; however, since the overall circuit activity is the same, both circuits are presented as a single model. Then, by employing a mathematical workout, the average model and separating the parameters into DC component, intermediate (1<sup>st</sup> order) components, and perturbations (2<sup>nd</sup> order). The inductor state equation is revealed in (14) by applying mathematical workouts. The plant is dismantled into coefficients utilized for system input parameters. The functional block diagram includes the transfer function of the inductor current to the duty-cycle input signal ( $G_{id}$ ), where the input voltage vector is set to zero.

$$\tilde{i}_L(s) = \left( \frac{(I_s - I_o) \left( \left( \frac{V_s}{L} - \frac{1}{T_s} \right) \cdot T_s + 1 \right) + 2I_o}{\left( \frac{V_s}{L} - \frac{1}{T_s} \right) \cdot T_s d_1 (2I_s - I_o)} \cdot \left( 2(I_s - I_o) + I_o \frac{1}{\left( 1 + s \frac{CR}{2} \right)} \right) \right) \tilde{d}(s) \quad (14)$$

where the  $I_s$  and the  $I_o$  are the rms input and output current, respectively,  $V_s$  is the rms input voltage,  $L$  is the inductor value,  $T_s$  is the switching cycle period,  $d_1$  is the duty-cycle (ON time),  $C$  is the capacitor value, and  $R$  is the load resistance (ohmic). The UTPR output voltage state equation is unveiled in (15). It is important to note that the output of the voltage controller is not multiplied by the absolute value of the sinusoidal waveform as in standard rectifiers.

$$\tilde{v}(s) = \left( \frac{I_o R}{\left( \frac{I_s V_s T_s}{V_s T_s - L} - I_o \right)} \cdot \frac{1}{\left( 1 + s \frac{CR(I_s - I_o)}{(2I_s - I_o)} \right)} \right) \tilde{v}_c(s) + \frac{\frac{I_o}{d_1} R}{\left( 1 + s \frac{CR}{2} \right)} \tilde{v}_s(s) \quad (15)$$

The state equation includes the UTPR output voltage transfer function to the inductor current reference input signal ( $G_{vc}$ ), where the input voltage vector is set to zero, and the input state vector coefficient ( $G_{vs}$ ), where the input reference voltage vector is set to zero. Unlike a standard rectifier, the control scheme does not require a multiplier, as presented in Figure 7, where the  $G_{vc}(s)$  is the voltage loop compensator and the  $G_{ci}(s)$  is the current loop compensator.

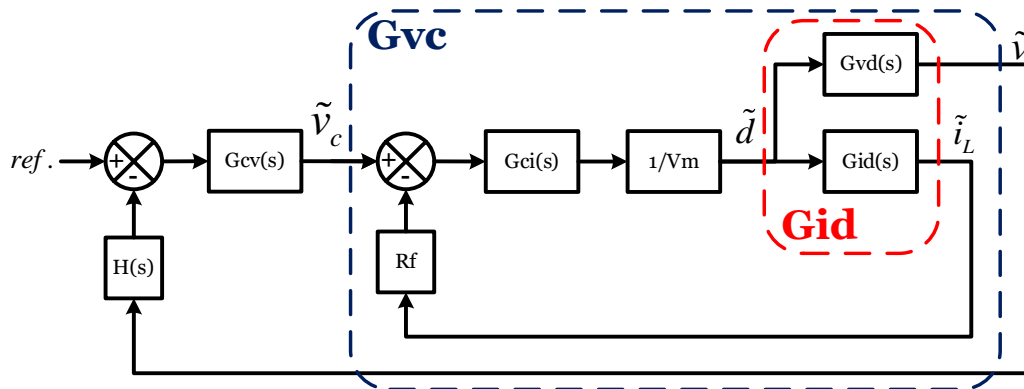
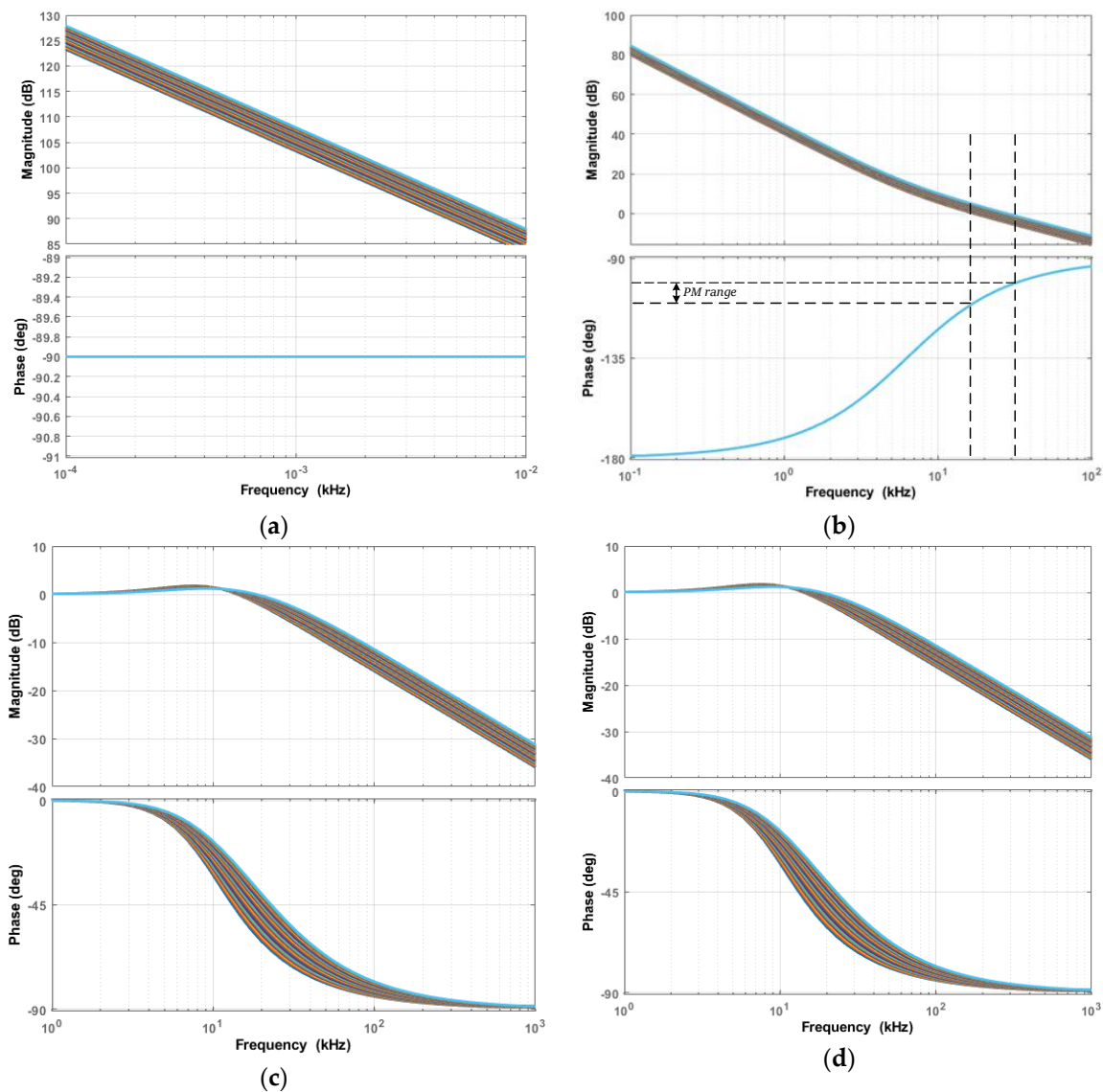


Figure 7. Dual loop UTPR average model block diagram control scheme.

#### 4. Simulation and Experimental Results

Based on the above analysis, the proposed UTPR circuit parameters were designed for multiplier-less dual loop conditions at DCM. The simulation was made with the PSIM tool operating at a switching frequency of  $f_{sw} = 100 \text{ kHz}$ . The input voltage was set to  $V_s = 230 \text{ Vrms}$ . In the design of the UTPR power inductor, the circuit output load was put into two conversion modes: step up and step down. At buck operation, the output load was set to 430 ohms ( $R = 430\Omega$ ) and the output load voltage to 75 volts ( $V_{load} = 75 \text{ V}$ ). At the boost mode, the output load was set to 4000 ohms ( $R = 4 \text{ k}\Omega$ ) and the output load voltage to 400 volts ( $V_o = 400 \text{ V}$ ). By employing (5), the minimal critical inductance is found to be  $L_{critical} = 498 \mu\text{H}$ ; thus, the actual inductance was determined to  $L =$

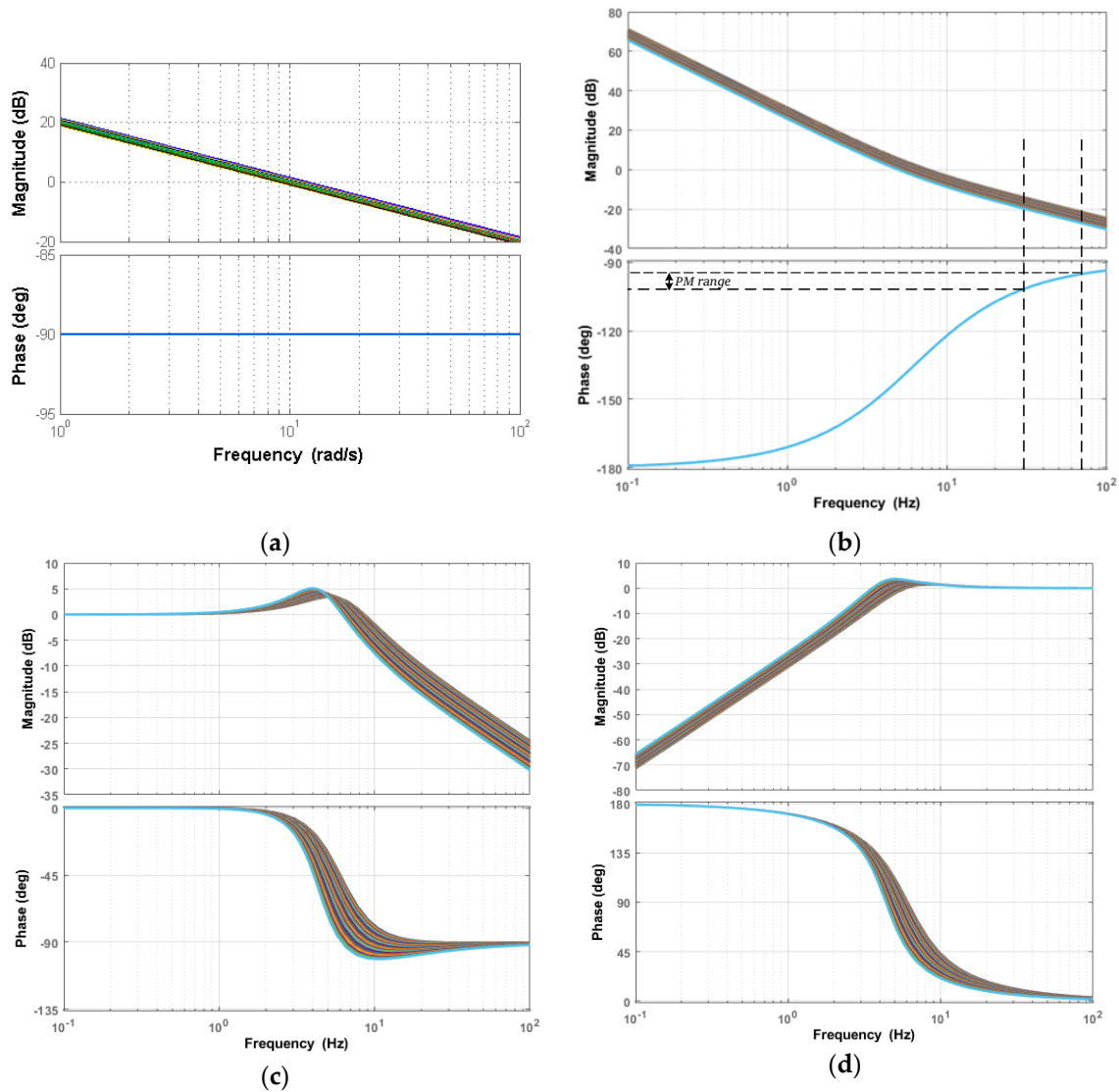
120  $\mu H$ . The output ripple voltage was set to 5%; hence, according to (12), the output capacitors are set to  $C = 470 \mu F$  (each) to satisfy the required output ripple voltage and the holdup demand. Applying (7), the duty ratio is revealed where  $d_{1,buck} = 0.2$  for the buck mode, and  $d_{1,boost} = 0.51$  for the boost mode. The current control loop bandwidth was set to one decade below the switching frequency (10 kHz) and the voltage to one decade below the line frequency (5 Hz). The controllers' coefficients were determined by assuming a nominal input voltage of 230 V, an output capacitor voltage of 275 V, and a load of 2.2 kilo ohm. The integration coefficient was found to be  $k_i=314.5$ . Under the assumption of a damping coefficient in a near-critical point with a value of 0.8, the proportional coefficient value is  $k_p=0.83$ . The voltage loop PI controller integration coefficient is  $k_i=112.6$ , and with a dumping constant of 0.8, the proportional coefficient is  $k_p=0.066$ . The family of all the possible current loop plants is shown in Figure 8a. The current loop gains family results are depicted in Figure 8b, verifying stability at all operating points according to the resulting phase margin (PM) range. Corresponding closed-loop tracking and disturbance rejection capabilities are given in Figures 8c and 8d, respectively, further enforcing the analysis outcomes above.



**Figure 8.** Inductor current control loop (a) Family of current loop plants; (b) Family of current loop gains; (c) Inductor current tracking behavior throughout the operating range; (d) Current loop disturbance rejection capabilities throughout the operating range.

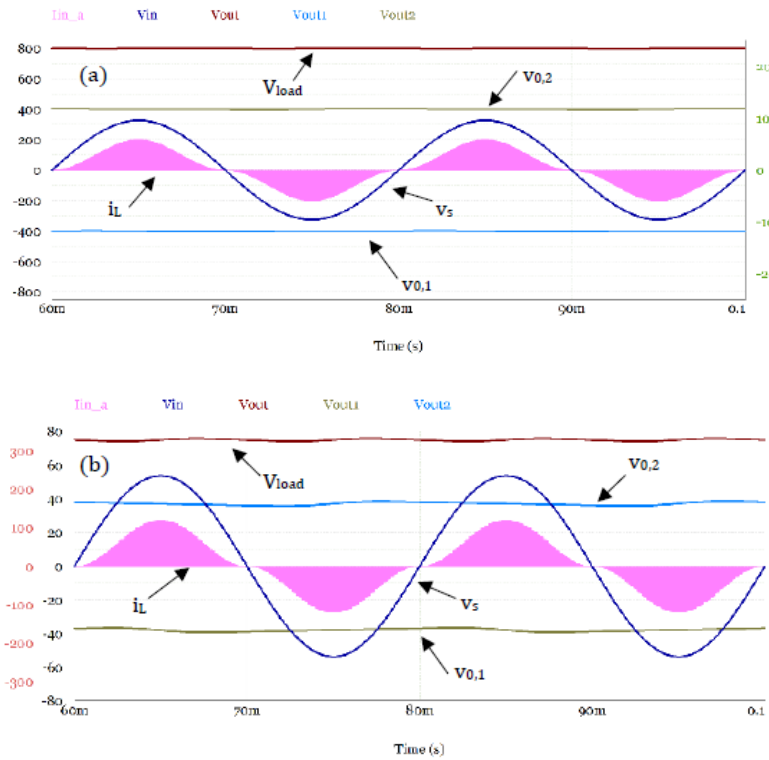
Following the UTPR inner current loop, the outer loop was set to the output voltage. The family of all the possible UTPR output voltage loop plants is shown in Figure 11. The voltage loop gains

family results are illustrated in Figure 9a, verifying stability at all operating points according to the resulting corrected PM range in Figure 9b. Corresponding closed-loop tracking and disturbance rejection capabilities are given in Figures 9c and 9d, respectively, validating the analysis conclusions.



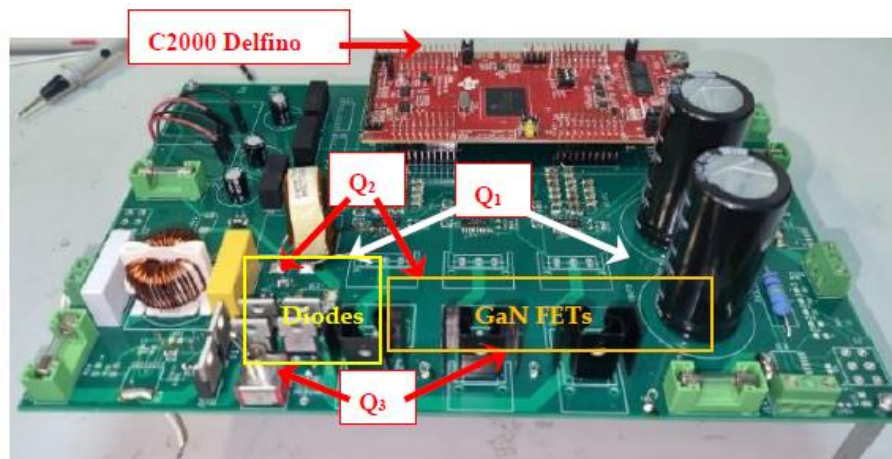
**Figure 9.** Output voltage control loop (a) Family of UTPR output voltage loop plants; (b) Family of UTPR output voltage loop gains; (c) UTPR voltage loop tracking behavior throughout the operating range; (d) UTPR voltage loop disturbance rejection capabilities throughout the operating range.

The DCM operation in a multiplier-less dual loop for buck mode and boost mode presents a self-PFC since the inductor current envelope follows the input voltage sine wave. The output ripple voltage of each output capacitor is marked as  $v_{o,1}$ ,  $v_{o,2}$  and the sum of both capacitors' voltage is equal to load voltage and marked as  $v_{load}$ . The output load voltage ripple frequency is 100 Hz, while the  $v_{o,1}$ ,  $v_{o,2}$  ripple voltage is 50 Hz, as presented in Figure 10a and Figure 10b.



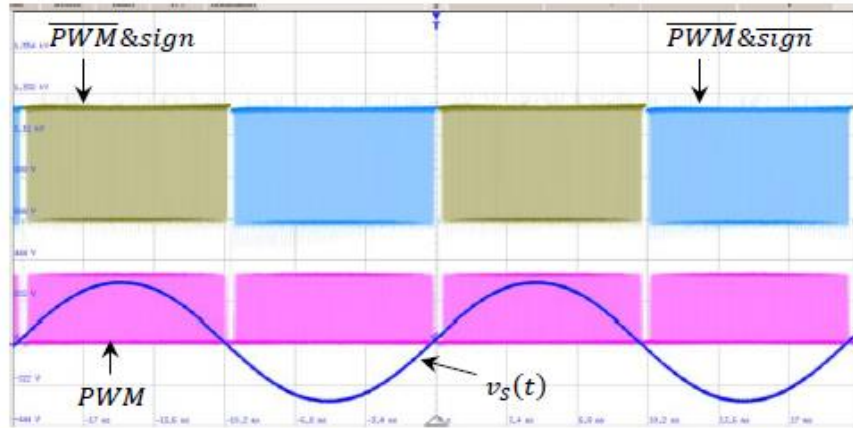
**Figure 10.** Simulation results for the UTPR input current and output voltage operating in DCM: (a) at boost mode and (b) at buck mode.

Following the simulation results, a prototype was designed. Based on the above analysis, the proposed UTPR prototype parameters were designed for operation at DCM with the same values as in the simulation. The switching frequency was set to  $f_{sw} = 100 \text{ kHz}$ , a resistive load of  $R = 0.43 \text{ k}\Omega, 4 \text{ k}\Omega$ . The revealed inductor from (5) is  $L = 120 \text{ }\mu\text{H}$ , and by (14), the output capacitor was set to  $C = 470 \text{ }\mu\text{F}$ . The circuit was fed by the California Instruments 751i AC Power Supply. The Texas-Instrument C2000 Delfino MCU F28379D LaunchPad™ governed the UTPR. The MCU measured the line voltage and synchronized all required logic signals to drive the UTPR switches. The UTPR main SW  $Q_1$  was utilized by the combination of Transphorm 950 V/15 A TP90H180PS GaN FET and the supporting four blocking Schottky diodes of ONSEMI 1.2 kV/10 A, the FFSP10120A in fashion as in Figure 2a. The upper switch  $Q_2$  and lower switch  $Q_3$  were utilized with the same devices in the style shown in Figure 2d. The UTPR experimental board is presented in Figure 11.



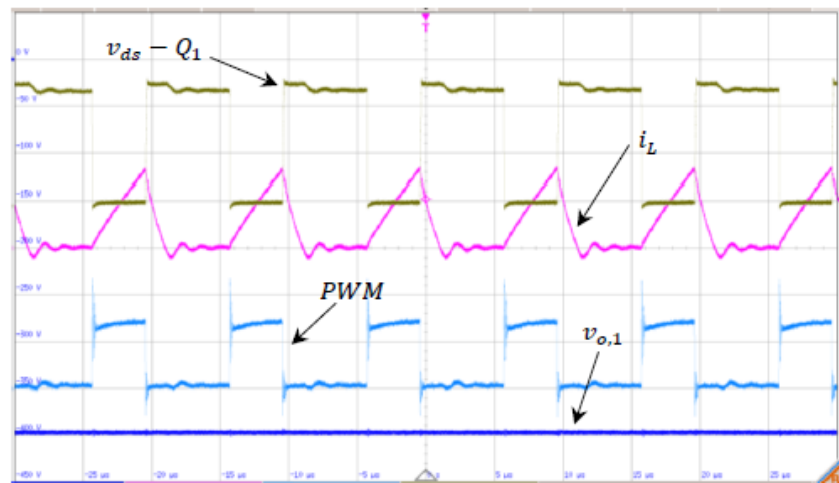
**Figure 11.** Experimental UTPR board.

The UTPR was designed for DCM operation when its control system operates in a multiplier-less dual loop; the reference signal was set according to (8). Measurements were carried out with a 200MHz Rohde & Schwarz RTM3000 oscilloscope equipped with a power analysis tool. The command signals for the switches was set as mentioned above, the main switch ( $Q_1$ ) receives the  $PWM$  signal, the upper switch ( $Q_2$ ) is active during the positive line cycle and, therefore, gets the  $\overline{PWM} \& \text{sign}(v_s(t))$ , and the lower switch ( $Q_3$ ) is active at the negative line sequence and acquire  $\overline{PWM} \& \text{sign}(v_s(t))$ . The command signals for all switches are presented in Figure 12.



**Figure 12.** Experimental signal commands for all switches.

The UTPR principle of operation is similar to all switch mode power supplies where the inductor is charged during the ON time. It delivers the accumulated energy to the output capacitor and the load during the discharge time, as explicit in Figure 13. The specific frame was taken during the positive line sequence where the inductor current is positive, and the output capacitor voltage is negative concerning the line neutral.

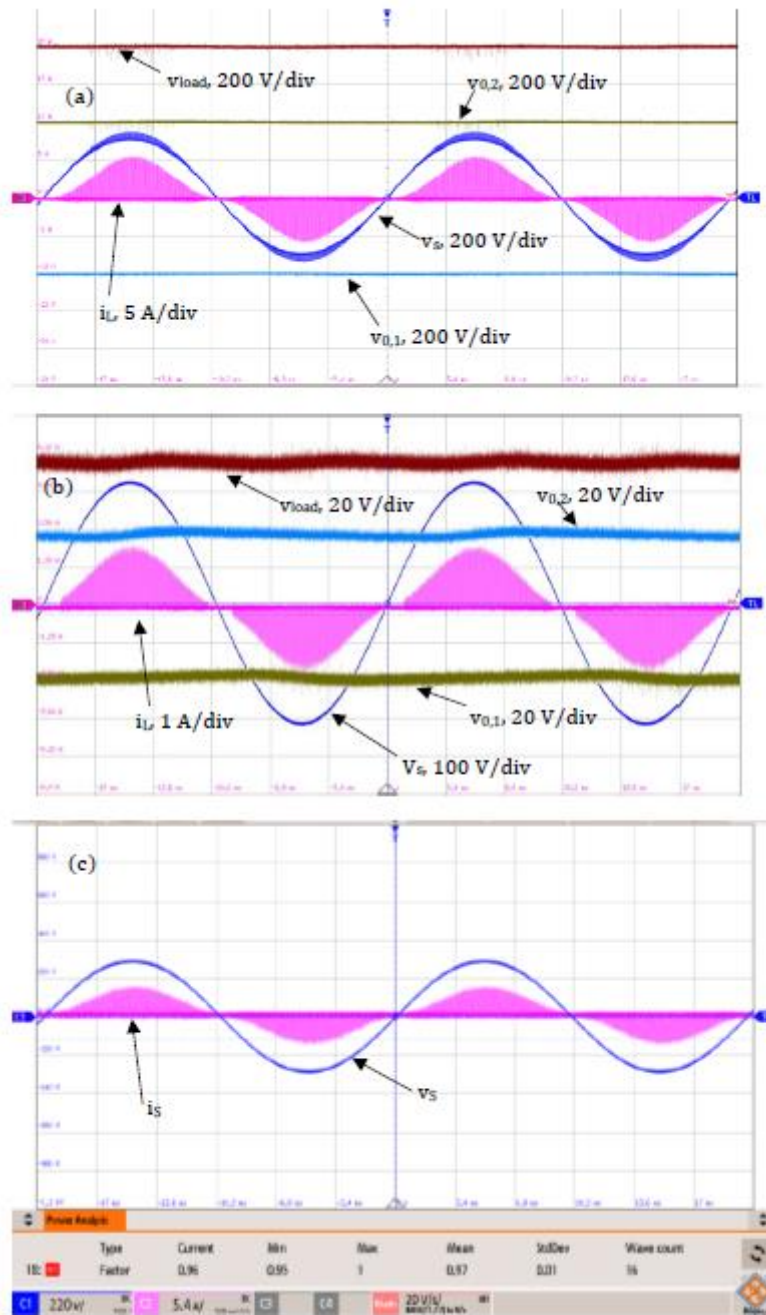


**Figure 13.** Experimental UTPR results of inductor current, main switch ( $Q_1$ ) voltage, PWM signal, and upper capacitor ( $v_{o,1}$ ) voltage.

In the boost mode, experimental results display an input voltage of  $V_s = 230 \text{ Vrms}$ , the output capacitor voltage was  $v_o = 400 \text{ V}$ , and the load voltage was  $v_{load} = 800 \text{ V}$  as shown in Figure 14a. In buck mode, under the same grid supply voltage, the output voltage was  $v_o = 37.5 \text{ V}$ , and the load voltage was  $v_{load} = 75 \text{ V}$ . In both cases, the inductor current envelope allows the input voltage shape, as shown in Figure 14b. The power factor is near unity ( $PF = 0.97$ ), as indicated in Figure 14c.



Although the UTPR runs at a multiplier-less dual loop, the inductor current shape is sinusoidal as an inherent feature of the buck-boost converter.



**Figure 14.** Experimental results for DCM in (a) boost mode; (b) buck mode; (c) and Power Factor.

## 5. Conclusions

This paper presents a new rectifier topology inherited from the buck-boost converter. The UTPR is a single-step universal rectifier; thus, it supports a wide output voltage range while reducing the component count, cost, volume, and weight. The output voltage can apply a two-voltage level for two terminal loads or a voltage level for low harmonic distortion loads. The principle of operation is demonstrated in dual loop mode. It was shown that the UTPR prototype could step up or down while keeping near-unity performance. This unique feature may ease the control computational effort since there is no need for a multiplier in the control circuitry. The UTPR output voltage is suitable for employing a standard load or feeding three-level voltage loads. The proposed topology could



correspond to many applications, especially for commercial low-voltage or high-voltage DC loads, storage applications, EVs, and three-level inverters. Future work on the subject will be implementing the dual loop controller for DCM and CCM at a single-phase rectifier and then into a three-phase interleaved rectifier where the circuit dynamics will be analyzed. A high-value output capacitance is one of the main drawbacks of a three-level single-phase rectifier; when implementing a three-phase rectifier, the output capacitance could be minimized to near zero.

## 6. Patents

The presented work is based on the international application patent cooperation treaty WO2022190097 A1 of 15 September 2022.

**Author Contributions:** Conceptualization, I.A., and D.B.; methodology, I.A., and M.S; software, Y.K.; validation, Y.O., E.D., and I.A.; formal analysis, I.A., and Y.K; investigation, I.A., and A.S; resources, Y.O., E.D.; data curation, A.S.; writing—original draft preparation, I.A.; writing—review and editing, I.A., D.B, M.S; visualization, Y.O.; supervision, I.A.; project administration, A.S.; funding acquisition, I.A.

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