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Tunable Foreground Self-Calibration Scheme for Split SAR ADC

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Abstract: The capacitor-mismatch among diverse defects caused by the manufacturing process variations significantly affects the linearity of capacitor-array used to implement the capacitive digital-to-analog converter (CDAC) in the successive-approximation-register (SAR) analog-to-digital converter (ADC). Accordingly, the linearity of the SAR ADC is limited by that of capacitor-array, resulting in serious yield loss. This paper proposes an efficient foreground self-calibration technique to enhance the linearity of the SAR ADCs by mitigating the capacitor-mismatch based on the split ADC architecture along with variable capacitors. In this work, two ADC channels (i.e., ADC1 and ADC2) for the split ADC architecture include their capacitive DACs (CDACs) whose binary-weighted capacitor-arrays consist of variable capacitors. A charge-sharing SAR ADC is used for each ADC channel. In the normal operation mode, their digital outputs are averaged to be the final ADC output, as in a conventional split ADC. In the calibration mode, every single binary-weighted capacitor for the two ADCs is sequentially calibrated by making parallel or/and antiparallel connection among two or thee capacitors from the two channels. For instance, because the capacitors of the CDACs ideally exhibit the binary-weighted relation as $C_n = 2 \times C_{n-1}$, variable capacitor C_n of ADC1 can be updated to be closest to the sum of C_{n-1} of ADC1 and C_{n-1} of ADC2 for the calibration. For the process, the two capacitor-arrays of the two ADCs can be reconfigured to be connected to each other, so that C_n of ADC1 can be connected with two of C_{n-1} of ADC1 and ADC2 in antiparallel. The two voltages at the top and the bottom plates of the CDAC are compared by a comparator of ADC1, and the comparison results are used to update C_n. This process is iterated, until C_n is in agreement with the sum of two of C_{n-1}. Finally, all the capacitors can be calibrated in this way to have the binary-weighted relation. The simulation results based on the proposed work with a split SAR ADC model verified that the proposed technique can be practically used, by showing that the total-harmonic-distortion and the signal-to-noise-and-distortion ratio were enhanced by 21.8-dB and 6.4-dB, respectively.

Keywords: self-testing; alternative testing; mixed-signal testing; manufacturing test; production test; built-in-self-test (BIST); self-calibration; self-healing; analog to digital converter (ADC)

1. Introduction

The fourth industrial revolution connects more smart devices, making intelligent networks of things which can communicate to each other, i.e., the internet of things. Mobile devices comprising a large proportion of the smart device require high power efficiency of circuit components included in their system [1–3]. Due to the benefit of low power consumption, the successive-approximation-register (SAR) analog-to-digital converter (ADC) among different ADC architectures has been highly attractive for ultra-low power applications such as mobile devices [4], and it can achieve high resolution and accuracy as well [5].

The SAR ADCs consists of a capacitive digital-to-analog converter (CDAC) including binary-weighted capacitors, a comparator, and the SAR logic [5]. The capacitor-mismatch among

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various defects caused by the manufacturing process variations negatively impacts on the linearity of the binary-weighted capacitors in the SAR ADC. Thus, the linearity of the SAR ADC is limited by that of capacitor-array, resulting in serious yield loss [6]. Therefore, the SAR ADC architecture suffers from the capacitor-mismatch issue.

A straightforward solution to mitigate the capacitor-mismatch is to simply increase the dimensions of the binary-weighted capacitors. It may be, however, impractical, because this method can degrade the ADC performances in different aspects, such as decrease in sampling-speed, increase of area overhead, higher power dissipation, and more [7].

There have been attempts to overcome mismatch issues of ADCs as follows. In [8], a calibration-purpose capacitor is added to the capacitor-array of the CDAC, and so it is used to alleviate the capacitor-mismatches. However, it may cause increase in area overhead of the CDAC, and it can also introduce the complexity in the layout of an ADC. For [9], a lookup table is generated to provide the statistical mapping relation between the ADC nominal outputs and actual outputs degraded by different mismatches. Then, gain mismatches among sub-ADCs are calibrated using this mapping relation. This method, however, requires long time to generate the lookup table, and also it demands huge memory space for the statistical mapping process data. In [10], the output signal differences between two identical ADCs (i.e., split ADC) are considered as an error, and then the output weight parameters are digitally updated by a genetic algorithm to reduce errors of an ADC. However, the output difference is not sufficient to represent errors caused by the mismatches, if both ADCs have similar mismatches to be similar outputs [11,12]. *Shuffling* scheme [13] was employed to a CDAC to avoid this issue, where different unit capacitors were randomly set to be used for different bits in each conversion. However, this method causes high complexity in circuity connections, and it may decrease the conversion speed [12]. For [14], capacitor-mismatches of a CDAC in a SAR ADC are calibrated using metal–oxide–semiconductor (MOS) capacitors (MOSCAPs) as a variable capacitor along with a dummy unit-capacitor for their calibration purpose. All the capacitors of the CDAC are replaced with the MOSCAPs, and the capacitance of each capacitor is compared with the capacitance sum of the next-smaller capacitors. However, this comparison process requires the complicated connections among those capacitors and additional calculation process, as the resolution of an ADC increases.

This paper proposes a promising self-calibration technique to significantly improve the performances of SAR ADCs by alleviating the capacitor-mismatches based on the split ADC architecture with variable capacitors. The aim of this work is to achieve the high calibration-accuracy by overcoming the drawback of a conventional split ADC [10].

The paper is organized as follows. A conventional split ADC architecture is briefly reviewed in Section 2. The proposed technique is then explained in Section 3. The experimental results and discussion are presented in Section 4, and conclusions are discussed in Section 5.

2. Review of Split ADC Architecture

This section discusses how a conventional split ADC architecture works, and analyzes their benefits and limitations.

2.1. Configuration

A conventional split ADC is configured as shown in Figure 1 [10]. An ADC input signal v_{in} is applied to two identical ADCs, i.e., *ADC1* and *ADC2* at the same time. Their outputs, x_1 and x_2 are fed to the bit weight functions, f_{w1} and f_{w2} in order to be multiplied by the weights, w_1 and w_2 which are unity initially. In the output process module, the ADC outputs, d_1 and d_2 are averaged to be d_o which is then used as the normal operation output, while the output difference, $d_e = d_2 - d_1$ is applied to the weight updater module, as an error between two ADCs. An adaptive algorithm such as a least-mean-square (LMS) updates w_1 and w_2 based on d_e in the weight updater, as shown in (1).

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$$\begin{aligned} w_1(n+1) &= w_1(n) - \mu\, d_e(n) x_1(n) \\ w_2(n+1) &= w_2(n) - \mu\, d_e(n) x_2(n) \end{aligned} \tag{1}$$

where n indicates the sample index, and μ represents the LMS step size. w_1 and w_2 are then properly multiplied by next outputs, x_1 and x_2 in f_{w1} and f_{w2}. This process is iterated, until d_1 is identical to d_2.

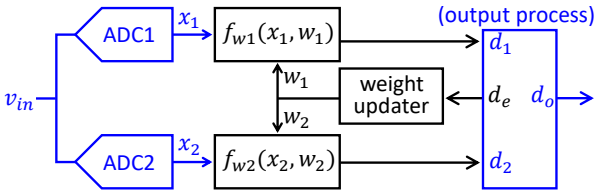

Figure 1. Configuration of conventional split ADC.

2.2. Considerations

There are several benefits of the split ADC architecture as follows. Each ADC channel occupies half the original ADC area, and thus a split ADC does not require larger area. In addition, each channel has a half of capacitance and G_m used for the original ADC, and it may also alleviate the noise at the output by the average process [10].

However, the output difference, d_e is not sufficient to represent the mismatch between two ADC channels, if both channel outputs include similar errors with the same polarity [11,12], i.e., if $|d_1| \approx |d_2|$ and $d_1 \cdot d_2 > 0$, then $d_e \approx 0$. Accordingly, (1) results in (2). The bit weights are, thus, not updated, thereby masking mismatches and degrading calibration accuracy.

$$\begin{aligned} w_1(n+1) &\approx w_1(n) \\ w_2(n+1) &\approx w_2(n) \end{aligned} \tag{2}$$

This issue can be observed from the simulation results in Figure 2 and Table 1; one model has similar mismatches between their two channels, and the other one does not. The model with this issue exhibited highly nonlinear results, compared to those of the other model without the issue.

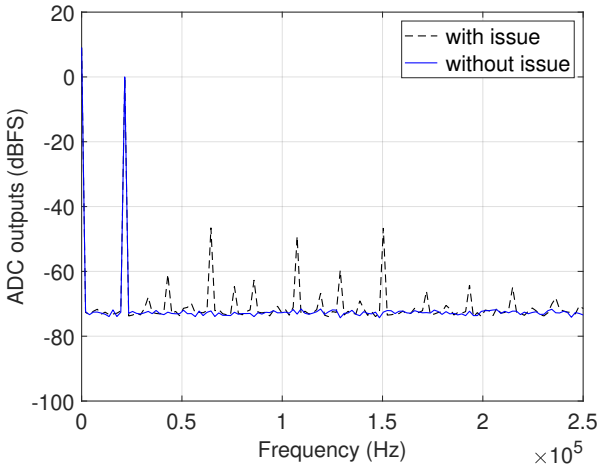

Figure 2. Spectral responses from simulation of conventional split ADCs with and without issue.

Table 1. Simulation results of conventional split ADCs with and without issue.

Performances	with issue	without issue
SNR	44.3 dB	48.2 dB
THD	42.3 dB	62.8 dB
SINAD	43.8 dB	48.5 dB

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3. Proposed Scheme

This work proposes an efficient foreground self-calibration scheme to enhance the performances of the SAR ADC by mitigating the capacitor-mismatches using variable capacitors. As a result, this work overcomes the drawback of a conventional split ADC discussed in Section 2.

3.1. Configuration

The proposed work can be simply configured by employing the split ADC platform, as shown in Figure 3(a) derived from Figure 1. The two ADC channels (i.e., ADC1 and ADC2) and the output average process highlighted in blue in a conventional split ADC shown in Figure 1 are employed for this work, because the proposed work does not require an adaptive algorithm using d_e which is fundamentally required for a conventional split ADC. Thus, the proposed work differently uses the two ADC channels for our calibration purpose. Those two ADC channels provide an efficient platform to allow the proposed calibration unit (i.e., *cal. unit*) to calibrate each capacitor using a few reference capacitors, resulting in much simpler process. Cal unit consists of two processes; the linear search process for the calibration and the voltage generation (by an embedded voltage generator) to apply an input voltage v_{bg} to the voltage-controlled variable capacitor, as shown in Figure 3(c). An 8-bit ADC is used as an example for better understanding, and the proposed work can be simply applied to higher resolution of the ADC.

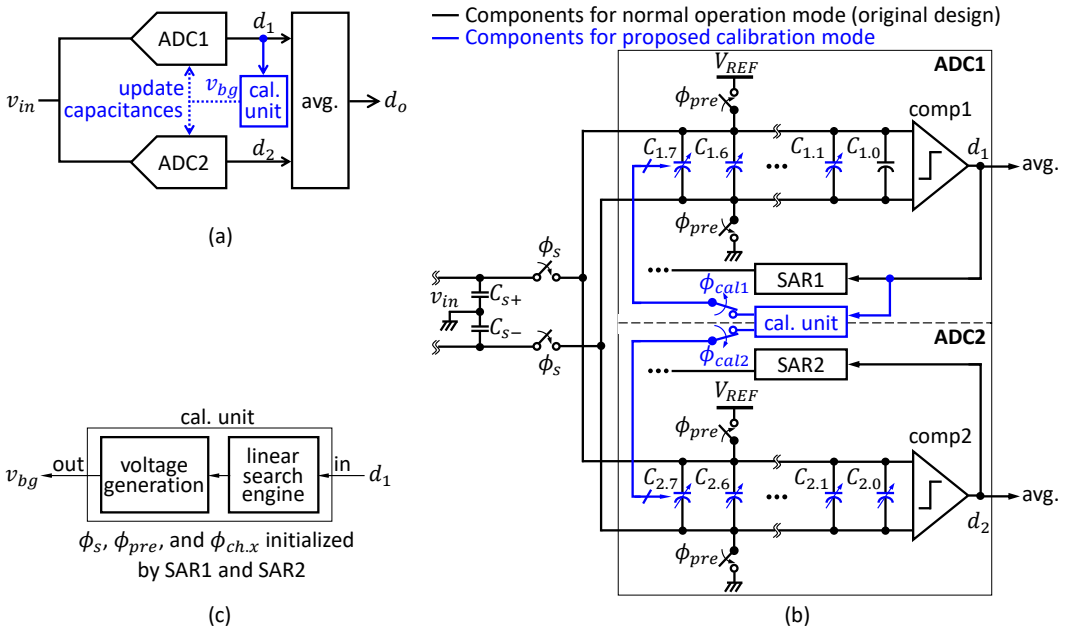

Figure 3. (a) Configuration of proposed work, (b) proposed foreground self-calibration based on split CS-SAR ADC, and (c) *cal. unit* embedded in (b).

The proposed work in Figure 3(a) can be realized as shown in Figure 3(b). A charge-sharing (CS)-SAR ADC [15] with differential inputs is used for each of ADC1 and ADC2, each of which consists of a track/hold stage (omitted in Figure 3(b) for simplicity), a sample stage (C_{s+} and C_{s-}), a CDAC ($C_{ch.x}$), and a comparator (*comp1* or *comp2*).

The convention $C_{ch.x}$ in the CDAC represents either a binary-weighted capacitor or capacitance in contexts, and its subscript *ch* indicates each ADC channel index (i.e., 1 or 2), and another subscript x represents each capacitor index in the CDAC (e.g., $0-7$ for an 8-bit ADC). Thus, ideally $C_{1.7} = C_{2.7} = 2^7 C_u$, $C_{1.6} = C_{2.6} = 2^6 C_u$, ..., $C_{1.0} = C_{2.0} = C_u$, where C_u is a unit capacitor. In addition, ϕ_{pre} is open to make connections between the top and bottom plates of ADC1 and those of ADC2. For each binary-weighted capacitor in a conventional CS-SAR ADC, there are two internal switches, $\phi_{ch.x}$ for each $C_{ch.x}$ as depicted in Figure 4(a) and (b) [15]. As shown in Figure 4(b), those two switches

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allow us to make connection between each $C_{ch.x}$ and their top or bottom plate, resulting in parallel ($S_{para.ch.x}$) or antiparallel ($S_{anti.ch.x}$) connection of $C_{ch.x}$. We call those two switches, $\phi_{ch.x}$ *para-switches* for convenience. In addition, a practical capacitance $C_{ch.x}$ can be modeled as a capacitance combined with an ideal capacitance $\overline{C}_{ch.x}$, and $C_{pt.ch.x}$ and $C_{pb.ch.x}$ which are the parasitic capacitances occurred on the top and bottom plates, respectively [16].

Different types of the capacitor to be used for a CDAC can be considered. While metal-oxide-metal (MOM) capacitors have good linearity, those exhibit low capacitance density because of thick oxide layer. In addition, metal-isolation-metal (MIM) and poly-isolation-poly (PIP) capacitors show good linearity and high capacitance density due to thin oxide layer, however those require additional masks and more fabrication steps, thereby increasing manufacturing cost. On the other hand, MOSCAPs have high density of the capacitance, and those need no additional mask process. For the structure of the MOSCAP, the MOSCAP introduces capacitance between a bulk and a gate of the metal–oxide–semiconductor field-effect-transistor (MOSFET) as shown in Figure 4(c), and the gate and the source (connected with the drain) are two terminals of a variable MOSCAP. Then, increasing the input voltage, v_{bg} between the bulk and the gate almost linearly decreases the capacitance between their two terminals, resulting in a MOSCAP as a variable capacitor. Those capacitors, however, suffer from the nonlinearity; a MOSCAP differently operates in three operation regions divided on the basis for voltage values across the MOSCAP, where its capacitance varies with the voltage value across the MOSCAP in the depletion region, while it is overall constant in the accumulation and inversion regions. As mentioned in Section 1, in [14], all the capacitors of the CDAC are replaced with variable MOSCAPs shown in Figure 4(c) by carefully using the MOSCAPs in the inversion region, and thus a SAR ADC is calibrated based on the binary-weight relation among capacitors along with a dummy unit-capacitor for their calibration purpose. In the proposed work, the variable MOSCAPs employed from [14] are fully charged in the precharge step. Then, because the passive CDAC of the CS SAR ADC is not connected with any power source, and also it has no connection with external circuitry, assuming a comparator has high impedance at its input terminal, the same amount of the net charges in the capacitors are retained until the sampling step is completed. Thus, the MOSCAPs stay in the inversion region during the calibration process. The variable MOSCAP shown in Figure 4(c) is discussed in detail in [14,16]. The aim of this work is to accomplish a highly accurate calibration methodology by overcoming the drawback of a conventional split ADC, using a variable capacitor and its input voltage generator employed from [14] in cal unit. In addition, the variable capacitors used for the cal unit can be a capacitor-array as well as a voltage-controlled capacitor (e.g., variable MOSCAP, varicap, and more). In fact, proposing a new variable capacitor along with its input voltage generator is not trivial, and thus it is out of scope of this work.

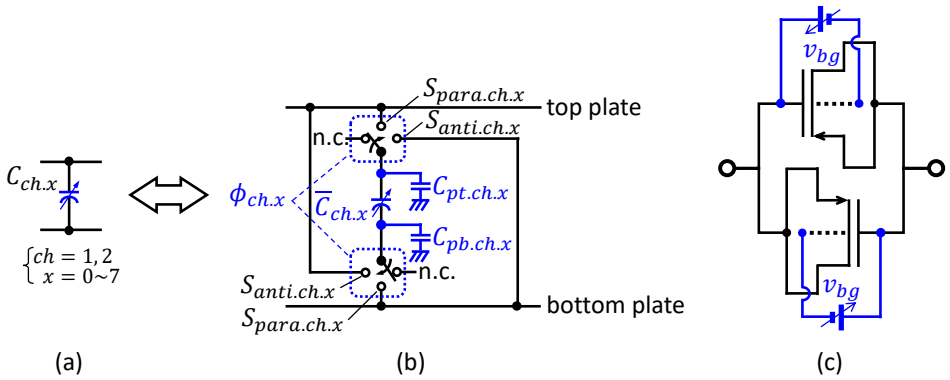

Figure 4. (a) Variable and binary-weighted capacitor symbol used in Figure 3(b) represents (b) a capacitor with *para-switches*, and it can be realized using (c) variable MOSCAP or (d) variable MOSCAPs in antiparallel.

To be summarized, the components for this work are highlighted in blue in Figure 3(b), such as variable capacitors-based arrays of the CDAC, the nodes $S_{top/bot}$, cal unit, and switches $\phi_{cal1/2}$. For

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efficiency, a set of the track/hold stage and the sample stage, which is designed for each of two ADC channels in a conventional split ADC, are merged into a single set which can be shared by the two ADCs for this work, so that ADC1 and ADC2 can use exactly same input stage, as shown in Figure 3(b).

3.2. Calibration process

The procedure for the proposed foreground self-calibration is discussed in detail in this section. The proposed scheme is performed in two sequential steps: (1) precharge and (2) capacitance calibration, and the full process is operated by cal unit.

For the precharge step (i.e., the first step), the split CS-SAR ADC shown in Figure 3(b) is reconfigured into that shown in Figure 5, by performing the followings: ϕ_s is open to disconnect the sampling stage (i.e., C_{s+} and C_{s-}) from the CDAC for both the channels. ϕ_{pre} is closed to provide the charges to all the binary-weighted capacitors. The para-switches of all the capacitors are then connected to their $S_{para.ch.x}$ shown in Figure 4(b), and comp1 and comp2 are disabled. Finally, all the binary-weighted capacitors are fully precharged by V_{REF}.

For the capacitance calibration (i.e., the second step), all the binary-weighted capacitors are sequentially calibrated in order from the least-significant-bit (LSB) capacitor to the most-significant-bit (MSB) capacitor, as listed in Table 2, thereby completing all the capacitors in the binary-weighted relation. For better understanding, the first two sequences in Table 2 are explained using Figures 5–7, and Table 2, in detail as an example, instead of describing the generalized procedure.

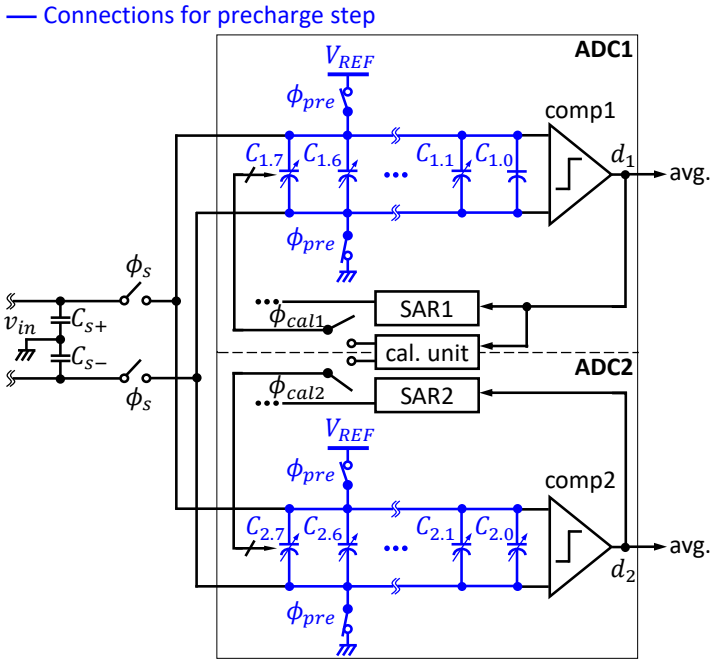

Figure 5. Precharge step.

The first calibration sequence of Table 2 calibrates $C_{2.0}$ using $C_{1.0}$ as a reference capacitor, without any change of $C_{1.0}$ after its fabrication, as shown in Figure 6. Firstly, the LSB capacitors of each ADC channel (i.e., $C_{1.0}$ and $C_{2.0}$) are connected to their top and bottom plates in antiparallel. In order for this, $\phi_{2.0}$ is set on $S_{anti.2.0}$ as shown in Figure 7(a), while $\phi_{1.0}$ is set on $S_{para.1.0}$ as shown in Figure 7(b). On the other hand, all other capacitors are disconnected from the top and bottom plates by setting their para-switches on *n.c.* (i.e., no connection). In addition, comp2 is disabled, and comp1 is enabled assuming that its common-mode voltage is ignored for simplicity. Basically, $C_{2.0}$ of ADC2 is connected to $C_{1.0}$ and comp1 by setting ϕ_{pre} open in both the two ADC channels as highlighted in blue in Figure 6. The values of the switches for the proposed calibration mode and the normal mode are summarized in Table 3 and Figure 8. The only those effective circuits are depicted in Figure 7(c) for better understanding.

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Table 2. Capacitors participating in each calibration sequence.

Calibration sequences (cal. seq.)	Reference capacitor(s)	Capacitor under calibration
1	$C_{1.0}$	$C_{2.0}$
2	$C_{1.0}$ and $C_{2.0}$	$C_{1.1}$
3	$C_{1.1}$	$C_{2.1}$
4	$C_{1.1}$ and $C_{2.1}$	$C_{1.2}$
...	...	...
15	$C_{1.7}$	$C_{2.7}$

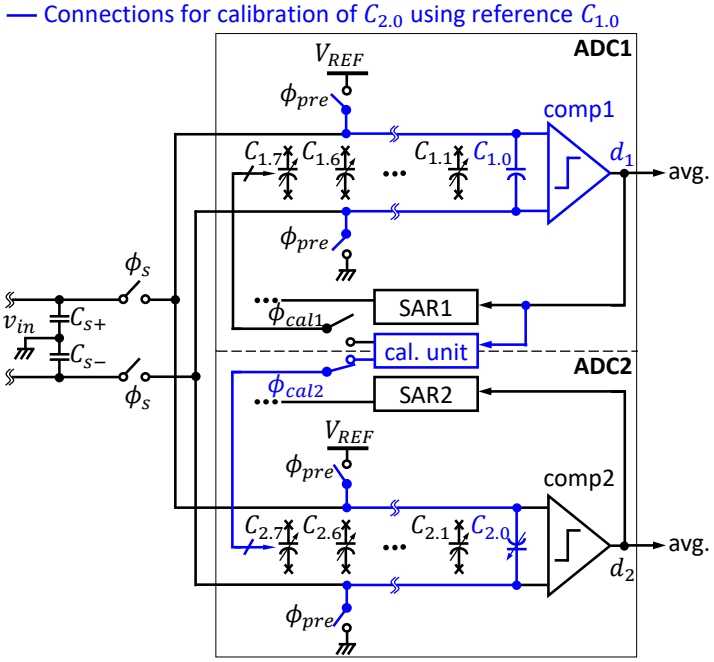

Figure 6. Capacitance calibration step for the first calibration sequence in Table 2.

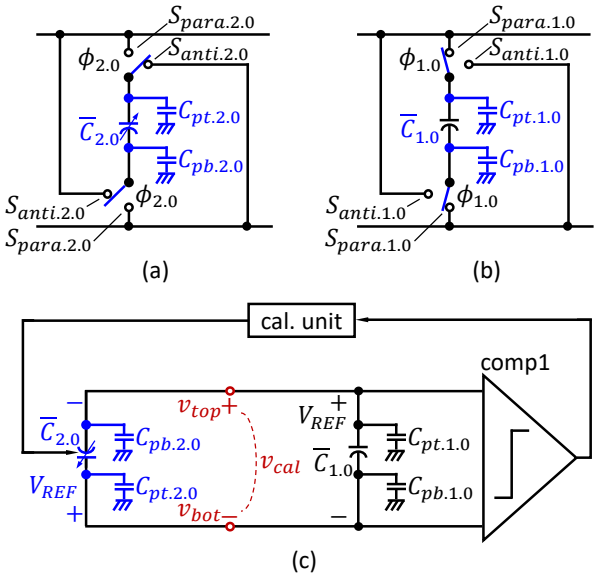

Figure 7. Connections for para-switches of (a) $C_{2.0}$ and (b) $C_{1.0}$ shown in Figure 6 support (c) effective circuitry of Figure 6.

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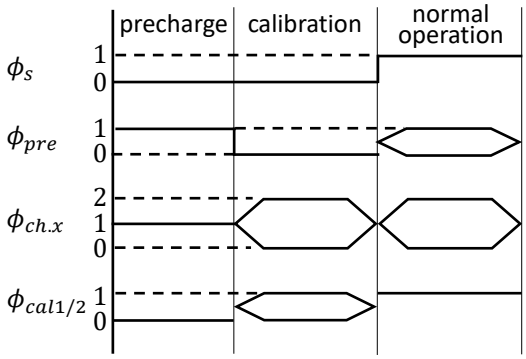

Figure 8. Values of switches for proposed calibration mode and normal mode.

Table 3. Value definitions of switches for proposed calibration mode.

Values	ϕ_s	ϕ_{pre}	$\phi_{ch.x}$	$\phi_{cal1/2}$
0	open	open	open	open
1	closed	closed	$S_{para.ch.x}$	closed
2	n/a	n/a	$S_{anti.ch.x}$	n/a

In Figure 7(c), v_{cal}, which is a voltage between the top and bottom plates, is derived by the charge conservation from (3) to (7). At the moment when $C_{1.0}$ and $C_{2.0}$ are initially (i.e., the time $t = 0$ right after the precharge step) connected in antiparallel, V_{REF} is still dropped across each capacitor. As discussed in Figure 4(b), $C_{pt.1.0}$ and $C_{pb.1.0}$ are the parasitic capacitances for $\overline{C}_{1.0}$, and $C_{pt.2.0}$ and $C_{pb.2.0}$ are the parasitic capacitances for $\overline{C}_{2.0}$, as shown in Figure 7(a), (b), and (c), as modeled in [16]. Then, the overall initial charge $Q_{ini.top}$ on the top plate in Figure 7(c) can be identified as

$$\begin{aligned} Q_{ini.top.1.0} &= \overline{C}_{1.0}(V_{REF} - 0) + C_{pt.1.0}(V_{REF} - 0) \\ Q_{ini.bot.2.0} &= \overline{C}_{2.0}(0 - V_{REF}) + C_{pb.2.0}(0 - 0) \\ Q_{ini.top} &= Q_{ini.top.1.0} + Q_{ini.bot.2.0} \\ &= (\overline{C}_{1.0} + C_{pt.1.0} - \overline{C}_{2.0})V_{REF} \end{aligned} \tag{3}$$

where $Q_{ini.top.1.0}$ and $Q_{ini.bot.2.0}$ are the initial charges on the top plate of $\overline{C}_{1.0}$ and the bottom plate of $\overline{C}_{2.0}$, respectively, which are made in the precharge step. Thus, $Q_{ini.top}$ is the sum of them in antiparallel circuit. Similarly, the overall initial charge $Q_{ini.bot}$ on the bottom plate of the CDAC can be found as

$$\begin{aligned} Q_{ini.bot.1.0} &= \overline{C}_{1.0}(0 - V_{REF}) + C_{pb.1.0}(0 - 0) \\ Q_{ini.top.2.0} &= \overline{C}_{2.0}(V_{REF} - 0) + C_{pt.2.0}(V_{REF} - 0) \\ Q_{ini.bot} &= Q_{ini.bot.1.0} + Q_{ini.top.2.0} \\ &= (\overline{C}_{2.0} + C_{pt.2.0} - \overline{C}_{1.0})V_{REF} \end{aligned} \tag{4}$$

where $Q_{ini.bot.1.0}$ and $Q_{ini.top.2.0}$ are the initial charges on the bottom plate of $\overline{C}_{1.0}$ and the top plate of $\overline{C}_{2.0}$, for each. Similarly, $Q_{ini.bot}$ is the sum of them in antiparallel circuit as well.

On the other hand, if $t > 0$, then the overall final charge $Q_{fin.top}$ and $Q_{fin.bot}$ on the top and bottom plates can be found as

$$\begin{aligned} Q_{fin.top} &= (C_{pt.1.0} + C_{pb.2.0})v_{top} + (\overline{C}_{1.0} + \overline{C}_{2.0})(v_{top} - v_{bot}) \\ Q_{fin.bot} &= (C_{pb.1.0} + C_{pt.2.0})v_{bot} + (\overline{C}_{1.0} + \overline{C}_{2.0})(v_{bot} - v_{top}) \end{aligned} \tag{5}$$

where v_{top} and v_{bot} are the voltages at the top and bottom plates of the CDAC, and also it is defined as $v_{cal} = v_{top} - v_{bot}$, which is the input voltage of comp1.

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Then, the two relations, $Q_{ini.top} = Q_{fin.top}$ and $Q_{ini.bot} = Q_{fin.bot}$ are obtained by the charge conservation, and those can be described using (3), (4), and (5) as follows.

$$\begin{aligned}(\overline{C}_{1.0} + C_{pt.1.0} - \overline{C}_{2.0})V_{REF} &= (C_{pt.1.0} + C_{pb.2.0})v_{top} + (\overline{C}_{1.0} + \overline{C}_{2.0})(v_{top} - v_{bot}) \\ (\overline{C}_{2.0} + C_{pt.2.0} - \overline{C}_{1.0})V_{REF} &= (C_{pb.1.0} + C_{pt.2.0})v_{bot} + (\overline{C}_{1.0} + \overline{C}_{2.0})(v_{bot} - v_{top}).\end{aligned} \tag{6}$$

v_{cal} is finally obtained by solving the simultaneous equations of (6) as

$$v_{cal} = \frac{C_{pt.1.0}C_{pb.1.0} - C_{pt.2.0}C_{pb.2.0} + (C_{pt1.0} + C_{pt.2.0} + C_{pb.1.0} + C_{pb.2.0})\hat{C}_1}{(C_{pt.1.0} + C_{pt.2.0})\check{C}_1 + (C_{pt.1.0} + \hat{C}_1)(C_{pb.1.0} + C_{pt.2.0})} \times v_{top} \tag{7}$$

where $\check{C}_1 = \overline{C}_{1.0} + \overline{C}_{2.0}$ and $\hat{C}_1 = \overline{C}_{1.0} - \overline{C}_{2.0}$. The comparison technique using antiparallel connection among multiple capacitors has been used in a conventional CS-SAR ADC [14,15].

As shown in (7), v_{cal} is a function of $\overline{C}_{2.0}$ as a variable capacitance. Based on the correlation in (7), the proposed calibration algorithm is simply overviewed in Figure 9(a). If $C_{1.0} > C_{2.0}$, then $v_{cal} > 0$, and accordingly comp1 output becomes 1, where this condition is defined as *case1* using a case indicator $dir = 1$. Since then, v_{bg} is decreased to increase $C_{2.0}$, resulting in comp1 $= 0$ at the moment when $C_{1.0} < C_{2.0}$ or $v_{cal} < 0$ which is defined as *case2* represented using $dir = -1$. The linear search for the calibration of $C_{2.0}$ finishes at this transition from the case1 to the case2, which can be considered as the moment when $C_{1.0} \approx C_{2.0}$ or $v_{cal} \approx 0$. In addition, even in the opposite transition from the case2 to the case1, the linear search works similarly. Overall, the calibration process for each capacitor under calibration is finished at the transition between the case1 ($dir = 1$) and the case2 ($dir = -1$), where $dir = 0$ initially.

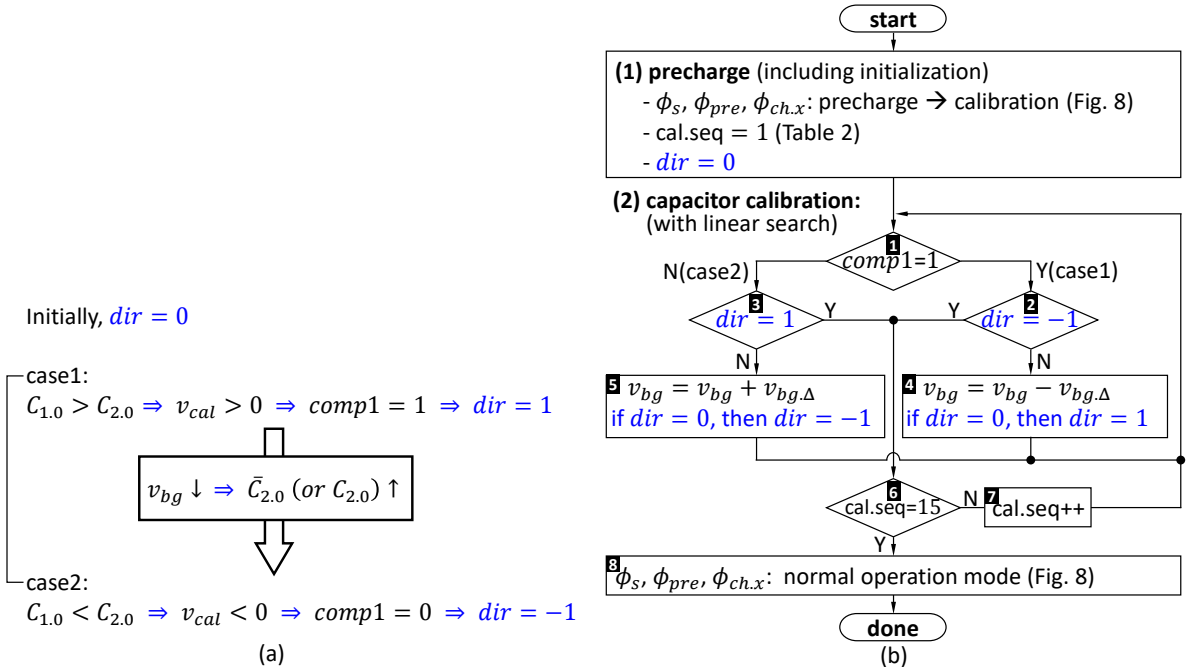

Figure 9. (a) Correlation among different parameters for (b) flow chart of proposed calibration process.

Based on (7) and Figure 9(a), the flow chart for this work is described as shown in Figure 9(b). The process in the flow chart is performed to calibrate capacitances, i.e., the second step of the proposed work. All those procedures are controlled by the linear search engine in cal unit shown in Figure 3(c). Initially, $dir = 0$ right after the precharge step is done. We put numbers from #1 to #8 for each flow of Figure 9(b). In #1, v_{cal} in (7) is measured by comp1, and then if comp1 output $= 1$ or case1 (i.e., $C_{1.0} > C_{2.0}$ and $v_{cal} > 0$), then it is also asked if the current $dir = -1$ in #2 to see if we were in the case2

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previously, or to see if we are in the transition between the cases 1 and 2. Because $dir = 0$ initially, we go to #4, and dir becomes 1 to represent the case1. In addition, v_{bg} is decreased by a step size $v_{bg.\Delta}$ of a MOSCAP, thereby updating $\overline{C}_{2.0}$. Then, we go back to #1 to check if comp1 output $= 1$ after v_{cal} is measured again, because v_{cal} has a correlation with the updated $C_{2.0}$, as shown in (7). If comp1 output $= 0$ in this time, then we go to #3 which is the case2. Because we were previously in the case1 and thus currently $dir = 1$, this moment is the transition from the case1 to the case2 which can be considered as the moment when $C_{1.0} \approx C_{2.0}$ or $v_{cal} \approx 0$, and thus the linear search finishes for the calibration of $C_{2.0}$, as discussed earlier. $\overline{C}_{2.0}$ may be correlated with its parasitic capacitances, $C_{pt2.0}$ and $C_{pb2.0}$ as shown in (7), and thus v_{bg}, which exhibits the correlation in (7), is identified to meet $v_{cal} \approx 0$ for the calibration of $C_{2.0}$. Next, we go to #6 to check if cal.seq $= 15$ (i.e., the last calibration sequence of Table 2). If no, then the second calibration sequence is set in #7 (i.e., cal. seq. $= 2$), which is discussed further below.

There can be a trade-off between $v_{bg.\Delta}$ and the process time of the linear search, as in general linear search method; the higher $v_{bg.\Delta}$ is, the sooner the linear search can be done, and the less accurate the searched value is (or vice versa). In addition, the following relation can be concluded from (7) to meet $v_{cal} = 0$:

$$\overline{C}_{2.0} = \overline{C}_{1.0} + \frac{C_{pt.1.0}C_{pb.1.0} - C_{pt.2.0}C_{pb.2.0}}{C_{pt1.0} + C_{pt.2.0} + C_{pb.1.0} + C_{pb.2.0}}. \tag{8}$$

The second calibration sequence of Table 2 calibrates $C_{1.1}$ using a sum of $C_{1.0}$ and $C_{2.0}$ which has been previously calibrated, and thus can be reused as a reference capacitor, as shown in Figure 10. Similarly, ϕ_{pre} is open. $C_{1.0}$ and $C_{1.1}$ of ADC1 and $C_{2.0}$ of ADC2 are connected in antiparallel to the top and bottom plates, by setting $\phi_{1.1}$ on $S_{anti.1.1}$, and by setting $\phi_{1.0}$ and $\phi_{2.0}$ on $S_{para.1.0}$ and $S_{para.2.0}$, respectively, as shown in Figure 10(a) and (b). $C_{1.0}$ is connected to $S_{para.1.0}$ (omitted for simplicity), as in Figure 7(b). All other capacitors are disconnected from the top and bottom plates, and also comp2 is disabled, while comp1 is enabled. As a result, $C_{1.1}$ is connected to $C_{1.0}$ and $C_{2.0}$ in antiparallel, as depicted in Figure 10(c).

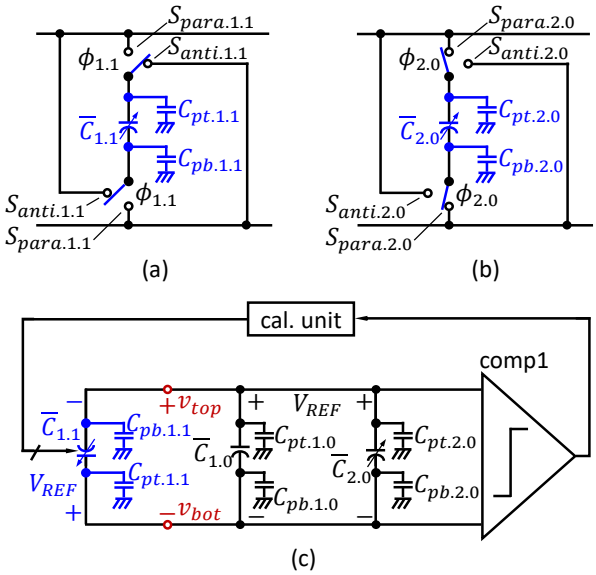

Figure 10. Connections for para-switches of (a) $C_{1.1}$ and (b) $C_{2.0}$ to be (c) calibration mode in antiparallel connection, along with $C_{1.0}$.

v_{cal} in Figure 10(c) is obtained based on the charge conservation as follows. When $C_{1.1}$, $C_{1.0}$, and $C_{2.0}$ are initially connected in antiparallel, V_{REF} is still dropped across each capacitor immediately after the precharge step. As shown in Figure 10(a), (b), and (c), $C_{pt/pb.1.1}$ and $C_{pt/pb.2.0}$ are similarly modeled as the parasitic capacitances on the top and bottom plates of $\overline{C}_{1.1}$ and $\overline{C}_{2.0}$, respectively. Then,

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the overall initial charge $Q_{ini.top}$ and $Q_{ini.bot}$ on the top and bottom plates in antiparallel circuit in Figure 10(c) can be identified as

$$\begin{aligned} Q_{ini.top} &= Q_{ini.bot.1.1} + Q_{ini.top.1.0} + Q_{ini.top.2.0} \\ &= (\overline{C}_{1.0} + C_{pt.1.0} + \overline{C}_{2.0} + C_{pt.2.0} - \overline{C}_{1.1})V_{REF} \\ Q_{ini.bot} &= Q_{ini.top.1.1} + Q_{ini.bot.1.0} + Q_{ini.bot.2.0} \\ &= (\overline{C}_{1.1} + C_{pt.1.1} - (\overline{C}_{1.0} + \overline{C}_{2.0}))V_{REF} \end{aligned} \tag{9}$$

where $Q_{ini.bot.1.1} = -\overline{C}_{1.1}V_{REF}$, $Q_{ini.top.1.0} = (\overline{C}_{1.0} + C_{pt.1.0})V_{REF}$, and $Q_{ini.top.2.0} = (\overline{C}_{2.0} + C_{pt.2.0})V_{REF}$. In addition, $Q_{ini.top.1.1} = (\overline{C}_{1.1} + C_{pt.1.1})V_{REF}$, $Q_{ini.bot.1.0} = -\overline{C}_{1.0}V_{REF}$, and $Q_{ini.bot.2.0} = -\overline{C}_{2.0}V_{REF}$. $Q_{ini.top.1.1}$ and $Q_{ini.bot.1.1}$ are the initial charges on the top and bottom plates of $\overline{C}_{1.1}$, respectively, which are made in the precharge step.

On the other hand, if $t > 0$, then the overall final charge $Q_{fin.top}$ and $Q_{fin.bot}$ on the top and bottom plates can be found as

$$\begin{aligned} Q_{fin.top} &= (C_{pb.1.1} + C_{pt.1.0} + C_{pt.2.0})v_{top} + (\overline{C}_{1.1} + \overline{C}_{1.0} + \overline{C}_{2.0})(v_{top} - v_{bot}) \\ Q_{fin.bot} &= (C_{pt.1.1} + C_{pb.1.0} + C_{pb.2.0})v_{bot} + (\overline{C}_{1.1} + \overline{C}_{1.0} + \overline{C}_{2.0})(v_{bot} - v_{top}). \end{aligned} \tag{10}$$

Then, the two relations, $Q_{ini.top} = Q_{fin.top}$ and $Q_{ini.bot} = Q_{fin.bot}$ are obtained by the charge conservation, and those can be described using (9) and (10) as follows.

$$\begin{aligned} (\hat{C}_2 + C_{pt.1.0} + C_{pt.2.0})V_{REF} &= \check{C}_{pb}v_{top} + \check{C}_2(v_{top} - v_{bot}) \\ (C_{pt.1.1} - \hat{C}_2)V_{REF} &= \check{C}_{pt}v_{bot} + \check{C}_2(v_{bot} - v_{top}) \end{aligned} \tag{11}$$

where $\check{C}_2 = \overline{C}_{1.0} + \overline{C}_{2.0} + \overline{C}_{1.1}$, $\hat{C}_2 = \overline{C}_{1.0} + \overline{C}_{2.0} - \overline{C}_{1.1}$, $\check{C}_{pb} = C_{pb.1.1} + C_{pt.1.0} + C_{pt.2.0}$, and $\check{C}_{pt} = C_{pt.1.1} + C_{pb.1.0} + C_{pb.2.0}$. Finally, v_{cal} is obtained by solving the simultaneous equations of (11) as

$$v_{cal} = \frac{(\hat{C}_2 + C_{pt.1.0} + C_{pt.2.0})\check{C}_{pt} - \check{C}_{pb}(C_{pt.1.1} - \hat{C}_2)v_{top}}{(\hat{C}_2 + C_{pt.1.0} + C_{pt.2.0})(\check{C}_2 + \check{C}_{pt}) + \check{C}_2(C_{pt.1.1} - \hat{C}_2)}. \tag{12}$$

As in the previous example, the linear search engine in cal unit finds $C_{1.1}$ that satisfies $v_{cal} \approx 0$ in (12). The flow chart of Figure 9(b) works for this example as well. $\overline{C}_{1.1}$ may be correlated with its parasitic capacitances as shown in (12), and thus v_{bg} is identified to meet $v_{cal} \approx 0$ for the calibration of $C_{1.1}$ as well. In addition, the following relation can be concluded from (12) to meet $v_{cal} = 0$.

$$\overline{C}_{1.1} = \overline{C}_{1.0} + \overline{C}_{2.0} - \frac{C_{pb.1.1}C_{pt.1.1} - (C_{pt.1.0} + C_{pt.2.0})(C_{pb.1.0} + C_{pb.2.0})}{\check{C}_{pt} + \check{C}_{pb}}. \tag{13}$$

All other calibration sequences in Table 2 can be also similarly processed. It can be observed in Table 2 that one (or two) reference capacitor is used in the odd(or even)-numbered calibration sequence. In summary, the proposed calibration scheme updates all the capacitances to be in the binary-weighted relation using only one or two reference capacitors, based on an actually fabricated LSB capacitor $C_{1.0}$, instead of forcedly updating each capacitance into a specific value predefined by the design specifications.

Several benefits of this work are summarized as follows:

- The proposed work does not require an adaptive algorithm e.g., LMS as in [10], and thus the heavy calculation process is not needed, and a digital hardware logic for calculation, i.e., a calibration unit, can be much simpler.
- This work does not require a dummy unit capacitor, e.g., C_{d0} by employing two-ADC channel configuration. In [14], C_{d0} is required to make the number of capacitors a power of 2, so that C_i

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under calibration can be compared with $C_{d0} + \sum_{j=0}^{i-1} C_j$ by a comparator for the capacitor mismatch calibration. For the proposed work, two unit capacitors are available from the two original ADC channels, and thus those capacitors facilitate the capacitance calculation based on a power of 2 without a dummy unit capacitor, as shown in Table 2.

- Using a small number (i.e., at most two) of the reference capacitors allows this work to make simple connection of capacitors as well as simple calculation in cal unit. For example of [14] with a 16-bit ADC, C_0 is calibrated using one reference comparator, C_{d0}. C_1 is calibrated using 2 reference capacitors, $C_0 + C_{d0}$, and finally calibrating C_{15} requires a sum of 16 reference capacitors, $C_{14} + C_{13} + ... + C_0 + C_{d0}$. Thus, total 136 reference capacitors are required to calibrate all the 16 capacitors of the CDAC. Basically, an N-bit ADC is calibrated using exponentially increased $\frac{N^2+N}{2}$ reference capacitors. On the other hand, the proposed work with a 16-bit ADC uses only 46 reference capacitors to calibrate all the capacitors of the two ADC channels. Thus, an N-bit ADC is calibrated using linearly increased $3N-2$ reference capacitors for this work. As a result, this work uses only 50, 31, 22, 17, and 14% of the reference capacitors required for [14] (i.e., $(3N-2)/\left(\frac{N^2+N}{2}\right) \times 100$), for 4, 8, 12, 16, and 18-bit ADCs, respectively. Therefore, as an ADC has higher resolution, i.e., more capacitors, the proposed calibration scheme significantly reduces the complexity both in the connection of the capacitors and the calculation process in cal unit.

3.3. Nonidealities

3.3.1. Energy

The energy consumption is discussed for the proposed work, in terms of two different phases: the calibration phase and the normal operation phase. The proposed calibration method is assumed to be conducted in the fabrication process, because it is a foreground calibration.

Firstly, the energy E_{pre} for the precharge step of the calibration phase is primarily consumed by charging the MOSCAPs of the CDAC shown in Figure 5, as in a conventional CS-SAR ADC. E_{pre} for ADC1 can be considered as

$$\begin{aligned} E_{pre} &= V_{REF}(Q_{cur} - Q_{prev}) \\ &= V_{REF}\left\{\sum_{i=0}^{7}(\overline{C}_{1.i} + C_{pt.1.i})V_{REF} - \sum_{i=0}^{7}(\overline{C}_{1.i} + C_{pt.1.i}) \cdot 0\right\} \\ &= V_{REF}^2 \sum_{i=0}^{7}(\overline{C}_{1.i} + C_{pt.1.i}) \end{aligned} \tag{14}$$

where Q_{cur} is a sum of the charges on all the MOSCAPs during the precharge step, and Q_{prev} is that in the previous status (i.e., no connection of the MOSCAPs, before the start of the precharge). Thus, E_{pre} of the split ADC can be

$$E_{pre} = V_{REF}^2 \sum_{i=0}^{7}(\overline{C}_{1.i} + C_{pt.1.i} + \overline{C}_{2.i} + C_{pt.2.i}). \tag{15}$$

As discussed in Section 2.2, the total capacitance of the two ADC channels in a split ADC is identical to that of a conventional ADC. Thus, it is concluded from (15) that the energy consumption of this work based on the split ADC is the same as that of a conventional ADC as well. All other circuits such as the comparators and cal unit are inactive in the precharge step.

Then, the energy consumption for the calibration step of the calibration phase is considered. For a conventional CS-SAR ADC, the CDAC passively operates after the precharge step, contrary to the CR-SAR ADC, and also the comparator inputs have infinite impedance thereby no current drained out of the CDAC [16]. Therefore, there is no primary energy consumed by the MOSCAPs for the CDAC of the proposed calibration, even though the charges are moved among different MOSCAPs

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by varying capacitance. For the voltage generator employed from [10], it is implemented mainly using three capacitors (i.e., C_B, C_{up}, and C_{down}), and thus the energy consumption can be calculated as $V_S^2(C_B + C_{up} + C_{down}) \times 15$, where V_S is a reference source voltage for the generator, and the number 15 means the total number of calibration sequence as discussed for Table 2.

Secondly, the energy consumption for the normal operation with the calibrated MOSCAPs can be as follows. The energy for the precharge of the normal operation phase should be identical to that in the discussion for (15). The primary energy for the CDAC in the binary search step of conventional SAR ADC is not consumed by the MOSCAPs with the calibrated capacitance, because the CDAC still behaves passively, as discussed earlier. For the voltage generators, V_S is disconnected from the generator after completing the calibration process, and the charges from v_{bg} for the already calibrated capacitors are held in each of C_B, C_{up}, and C_{down}. Thus, there is no energy consumption by the generator in the normal operation.

3.3.2. Area

Then, the chip area can be discussed as follows. In general, overall chip area of a conventional SAR ADC is limited by the area of the CDAC which consists of binary-weighted capacitors. Capacitors take up most area of a conventional SAR ADC, and thus the chip area is determined by the capacitance density [17,18]. The area of the CDAC is thus used to estimate the chip area of this work, even though our future efforts will incorporate the silicon implementation of this work. This is an example of the area estimations assuming the conservative unit capacitance of $11fF$ and the capacitance density of $11fF/\mu m^2$ [19], based on 130 nm process, although practical unit capacitor has much less value than this. Because each ADC channel of a split ADC has a half of capacitance for that of a conventional ADC, a unit capacitor can be assumed to be $5.5fF$. The total capacitance of ADC1 is $5.5fF \times (2^0 + 2^1 + \cdots + 2^7) = 1402.5fF$, and that of a split ADC would be $2805fF$. Therefore, the total area of the CDAC for this work can be estimated as $2805/11 = 255\mu m^2$.

3.3.3. Noise

In addition, the noise is discussed as below. Firstly, the noise in the proposed calibration mode can be analyzed as follows. For the precharge step, the thermal noise charge caused by the precharge switches in the CDAC is

$$q_{pre} = \sqrt{kTC_{cdac}} \tag{16}$$

where $C_{cdac} = \sum_{i=0}^{7}(\overline{C}_{1.i} + C_{pt.1.i} + \overline{C}_{2.i} + C_{pt.2.i})$. For the capacitance calibration step, the thermal noise charge introduced by the para-switches of all the capacitors participated in corresponding calibration sequence is

$$q_{cal} = \sqrt{kTC_{cal}} \tag{17}$$

where C_{cal} represents a sum of the reference capacitance(s) and the capacitance under calibration described in Table 2, e.g., $C_{cal} = C_{1.0} + C_{2.0} + C_{1.1}$ for the second calibration sequence. Considering the comparator noise, the total capacitance of the CDAC increases during the linear search process for each calibration sequence. From the comparator point of view, v_{cal} decreases, and the signal-to-noise ratio (SNR) is lower assuming a fixed value of noise. Basically, the effect of the comparator noise may change depending on the combination of the capacitors in the CDAC. It is not trivial to model the comparator noise for the proposed calibration, and thus its derivation is out of the scope for this work. However, the simulation results in Section 4.1 addressed the effect of the comparator noise.

Secondly, the noise analysis for the normal operation mode can be discussed as follows. The thermal noise in the precharge step is identical to that of the calibration mode. For the sampling step, the thermal noise charges caused by the para-switches of each capacitor used for each bit-decision cycle are

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$$q_{cdac1} = \sqrt{kTC_{cdac1}}$$
$$q_{cdac2} = \sqrt{kTC_{cdac2}} \quad (18)$$

where q_{cdac1} and q_{cdac2} are the noise charges occurred in the CDACs of ADC1 and ADC2, respectively. C_{cdac1} and C_{cdac2} are the capacitance sum of the capacitors participated during the sampling process for each bit-decision cycle in ADC1 and ADC2, for each. As in the proposed calibration mode, the effect of the comparator noise may change depending on the combination of the capacitors in the CDAC, and thus it was included in the simulation results.

4. Experimental Results and Discussion

The behavioral simulations were performed to validate the performance of the proposed calibration scheme, using MATLAB. Two 8-bit CS-SAR ADCs were modeled to configure a conventional split ADC. For the proposed calibration configuration, the capacitor-array for the CDAC was modeled with a nonlinear MOSCAP, and the proposed calibration unit was built. The MOSCAPs used in the simulation were assumed to have 40% of the average capacitances as their capacitance ranges, and their linear ranges were carefully used for the simulation. Capacitance-mismatches were set from 4% to 8%, and the standard variation of each capacitance was 1% as in typical capacitors. In addition, Gaussian random noises were set in the circuits for practical conditions.

4.1. Results of proposed calibration scheme

The proposed calibration process was performed from the LSB capacitors to the MSB capacitors, and then the critical performances of the ADCs were measured before and after applying this work, as shown in Figures 11 and 12, Tables 4 and 5. The legend, *before calibration* in all the plots and tables in Section 4.1 indicates the results measured from a conventional (single-channel) CS-SAR ADC which was not calibrated. On the other hand, the legend, *after calibration* represents the results obtained based on this work. The identical capacitor-mismatches were applied to the ADCs used to obtain each of those two results indicated by the legends, *before calibration* and *after calibration*. It is noted that the result comparison between a conventional split ADC and this work is discussed in Section 4.2.

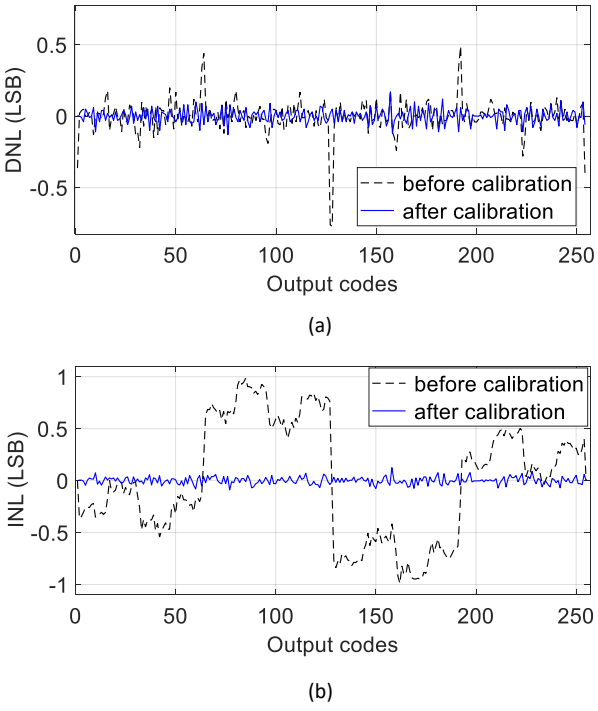

Figure 11. (a) DNL and (b) INL plots measured before and after applying this work.

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Table 4. DNL and INL results acquired before and after applying this work.

	before calibration	after calibration
DNL	0.78	0.17
INL	2.20	0.12

To evaluate the static performance of ADCs calibrated by this work, a conventional histogram-based differential-nonlinearity (DNL) and integral-nonlinearity (INL) method [20] was conducted by applying a ramp signal to both of a single CS SAR ADC (for *before calibration*) and a split ADC with the proposed calibration (for *after calibration*). The outputs of each ADC were then captured to obtain the code widths translated into the histogram results. Their DNL and INL results were acquired as shown in Figure 11, and Table 4 summarizes the results. Both DNL and INL results of *before calibration* were quite poor, compared to those of *after calibration*. In particular, because the mismatches of the MSB and the MSB−1 capacitors heavily affect overall performance of an ADC in general, a couple of high peaks can be observed around the MSB and the MSB−1 codes in the DNL plot, e.g., a center code and more. Accordingly, abrupt changes are observed in those output codes of the INL plot.

Conventional DSP-based test using the coherence sampling [20] was performed to accurately measure the dynamic performances of the ADC calibrated by the proposed scheme. A 21.5-kHz single-tone sinusoidal signal was applied to both a single ADC (for *before calibration*) and a split ADC based on this work (for *after calibration*). The stimulus was set on −1dBFS in order to avoid clipping of their output signal, as in conventional production testing. A total of 2^9 samples was captured by each ADC at 1-MSPS. The spectral responses of each ADC are shown in Figure 12, and the dynamic performance parameters are summarized in Table 5. In addition, the harmonic coefficients up to the 10-th order [21] were used to obtain the total-harmonic-distortion (THD) results. It is clear that SNR, THD, and signal-to-noise-and-distortion ratio (SINAD) were significantly enhanced by the proposed calibration scheme. Thus, this work can be practically used as a foreground self-calibration solution for SAR ADCs.

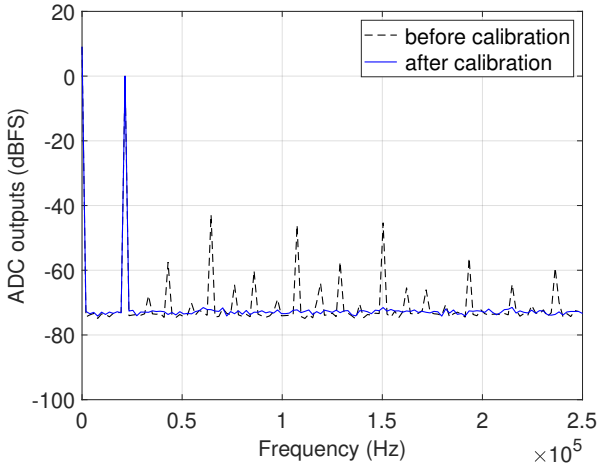

Figure 12. Spectral responses obtained before and after applying this work.

Table 5. Dynamic performances acquired before and after applying this work.

	before calibration	after calibration
SNR	43.5 dB	48.8 dB
THD	41.7 dB	63.5 dB
SINAD	42.5 dB	48.9 dB

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4.2. Comparison with conventional split ADC

As discussed in Section2 previously, the aim of this work is to overcome the issue of a conventional split SAR ADC [10], which exhibits low calibration accuracy, if two ADC channels have similar mismatches to be similar outputs. To validate this performance of this work, an identical set of the capacitor-mismatches from 4 to 8% was applied to the same bit-level of capacitors in the two channels of a split ADC, so that both the ADC channels can exhibit similar errors, e.g., the same 8% of the capacitor-mismatch on both $C_{1.1}$ and $C_{2.1}$. Under this condition, each of a split ADC [10] and this work completed their calibration processes. The results are shown in Table 6. All the performances were significantly improved by this work. In addition, the performances of this work was evaluated, even in the case that both ADC channels showed different errors, and the results are shown in Table 7. It was validated that SNR, THD, and SINAD of a split ADC calibrated by this work were compatible with those of a conventional split ADC [10], if both the ADCs have the different errors.

Table 6. Calibration performance comparison between a conventional split ADC and this work, in case of two channels showing similar errors.

	[10]	this work
SNR	44.3 dB	48.5 dB
THD	42.3 dB	63.1 dB
SINAD	43.8 dB	48.7 dB

Table 7. Calibration performance comparison between a conventional split ADC and this work, in case of two channels showing different errors.

	[10]	this work
SNR	48.4 dB	48.8 dB
THD	62.8 dB	63.5 dB
SINAD	48.5 dB	48.9 dB

4.3. Nonidealities for calibration

The effects of nonideality can be considered to analyze the calibration performance of the proposed work in practical situations. This section evaluates the performance of this work by different levels of capacitor-mismatch, and by the number of the conversions.

4.3.1. Levels of capacitor-mismatch

As discussed previously, the dynamic performances of SAR ADCs are limited by the capacitor-mismatch, and different levels of the mismatch can be introduced by the variations of practical manufacturing process. Because the mismatch on the MSB capacitance seriously affects the CDAC performance, SNR, THD, and SINAD of an ADC calibrated by the proposed work were analyzed, by increasing the mismatches on the MSB capacitors up to 13% in the simulation. As the mismatch increased, each of SNR, THD, and SINAD almost exponentially diminished before applying this work, while those obtained after applying the proposed work were overall consistent, as shown in Figure 13. Because of capacitive variation present in the variable capacitors, the performances by the proposed work exhibited small variations.

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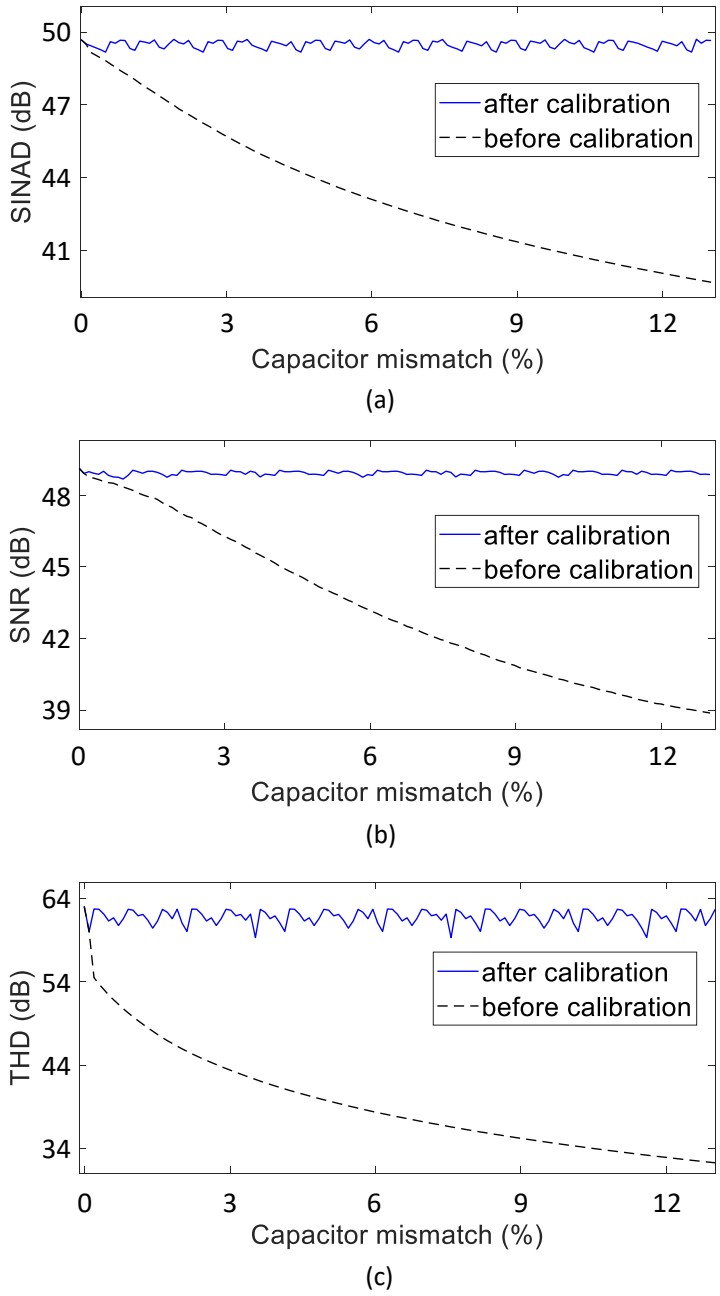

Figure 13. Performances as a function of capacitor-mismatch on MSB capacitor.

4.3.2. Number of conversions

The linear search process is performed to update each capacitor under calibration by monitoring the outputs of comp1 for this work, as discussed in Section 3. Figure 14 shows how SNR and THD of a split ADC were improved, as the capacitors were calibrated from the LSB to the MSB capacitors in the calibration. Overall, as the conversion went on, SNR and THD were enhanced. The total number of conversions was 2364. In particular, because the proposed calibration is processed from the LSB to the MSB capacitor, both of SNR and THD rose steeply from the conversion index 1861 at which the proposed calibration for the MSB-1 capacitor was completed.

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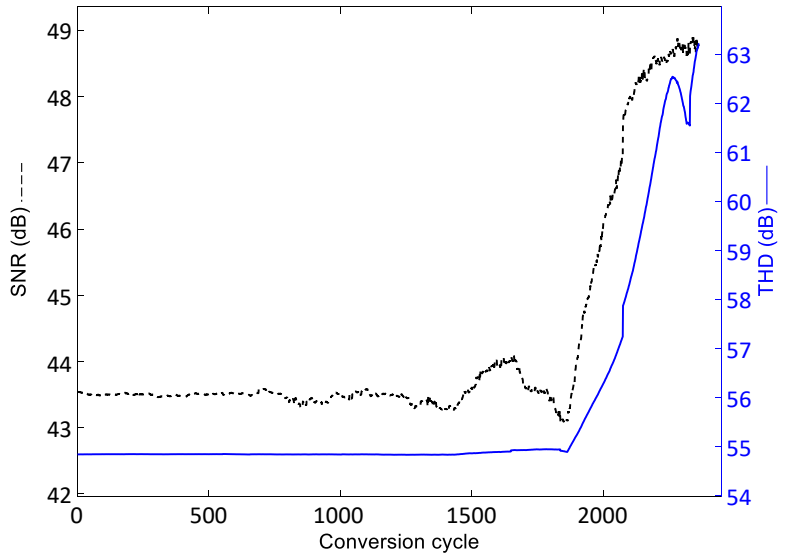

Figure 14. Performances as a function of conversions.

5. Conclusions and future work

This paper proposed a promising foreground self-calibration scheme, that improves the linearity of the SAR ADCs by significantly alleviating the capacitor-mismatches efficiently using the split ADC architecture along with variable capacitors. In this work, two CS-SAR ADC channels of the split ADC have their CDACs whose binary-weighted capacitors are implemented using variable capacitors. In the normal operation mode, their digital outputs are averaged to be the final ADC output. For the calibration mode, every single binary-weighted capacitor of a split ADC is calibrated one at a time. For instance, C_n of ADC1 can be updated to be closest to the sum of C_{n-1} of ADC1 and C_{n-1} of ADC2 by comparing those two capacitances using comp1 based on the reconfiguration. The comparison process can be iterated by updating C_n with the linear search, till C_n is in agreement with the sum of two of C_{n-1}. Finally, all the capacitors can be calibrated in this way to have the binary-weighted relation. The simulation results based on the proposed work with an 8-bit split SAR ADC model verified that the proposed scheme can be practically used, by showing that THD and SINAD were enhanced by 21.8-dB and 6.4-dB, respectively. Therefore, this work efficiently overcomes the limitation on the calibration accuracy of the conventional split SAR ADC, in case that the similar capacitor-mismatches are present in both ADC channels. Our future efforts will incorporate further enhancement of the calibration accuracy by overcoming the comparator offset error of both the ADCs. In addition, the process time will be optimized to be used as a background calibration scheme as well, and this work will be implemented in silicon.

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