A 30% Power Reduction Circuit Design for NAND Flash by Utilizing 1.2V I/O Power Supply to Bitline Path

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***Abstract*—This study proposes a low power circuit design for NAND Flash which is one of the power-hungry devices in datacenters. Power consumption in bit-line (BL) path can be reduced by 60% by utilizing 1.2V I/O power supply instead of 3V power supply, which contributes to reduction in the total power during read operation of 30%. The additional switching circuit only requires silicon area of 0.1mm^2 which is equivalent to 0.1% of a nominal die size of 100mm^2. To prevent degradation in sensing margin, the sensing node is pulled up to an internal supply voltage of 2V as used in the conventional design, which is regulated from 3V power supply, before starting sensing operation. This switching operation requires an additional timing of about 100ns which is equivalent to about 2% of an entire BL delay of 5µs. NAND flash interface does not have to be changed because the proposed design can work with the existing interface. BL path and the additional switches were designed in 65nm CMOS. A reduction in power in BL path of 60% was validated with SPICE simulation. As a result, the proposed design can contribute to power reduction in datacenter without any significant overhead on silicon area, BL delay and system design change.**

Keywords—NAND flash, low power circuit, bit line, datacenter

I. INTRODUCTION

Huge amounts of data such as photos, movies, and personal information are stored in datacenters. The amount of data has been increasing day by day. It is reported in [1] that the disks storing the data such as Hard Disk Drives (HDDs) and Solid-State Drives (SSDs) consume 14% of power consumption in datacenters. SSD is composed of multiple NAND flash memory chips, NAND controller, and DRAM as a data buffer, as shown in Fig. 1. SSDs do not have moving mechanical components like HDDs. Thus, both the read/write latency and power can be significantly reduced with SSDs. As a result, SSDs have been replacing HDDs in datacenters because of faster access and lower power.

Fig. 2 shows the trend of the power supplies for NAND Flash. VDDQ supplied to input and output buffers (I/Os) has been reduced from 3V in ONFI 1.0 (a) to 1.8V in ONFI 2.0 (b) and to 1.2V in ONFI 4.0 (c) [2], in order to increase the I/O bandwidth with scaled CMOS. On the other hand, VDD has not been updated from 3V because it is used for charge pumps to generate write/erase voltages of 20V or higher as well as for digital circuits with 3V CMOS. After ONFI 2.0, VDDQ has been decoupled from VDD, resulting in power reduction in I/O bus. For further power reduction, we propose a circuit design for utilizing VDDQ for BL path, as shown in Fig. 2 (d).

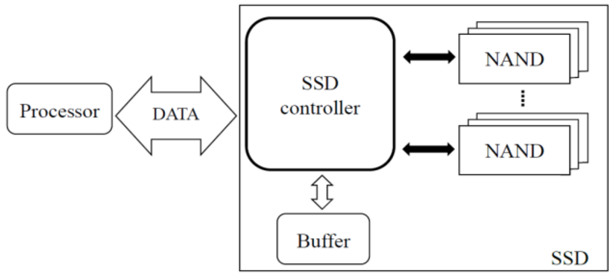

Fig. 1. Overview of SSD configuration.

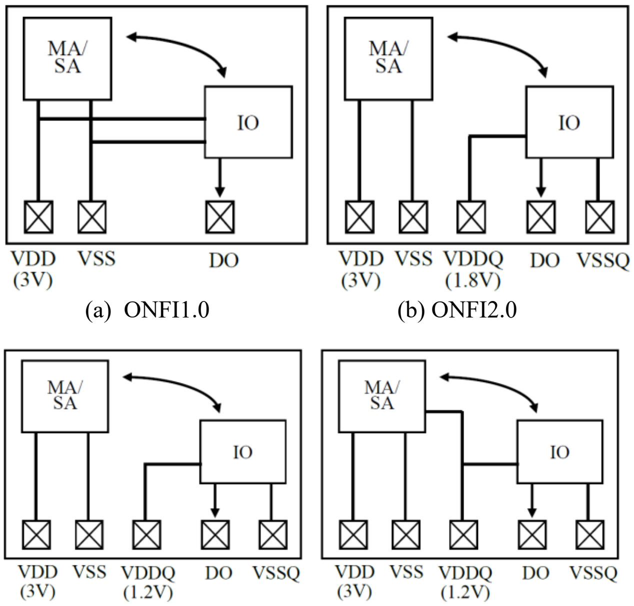

Fig. 2. Trend of power supplies for NAND Flash (MA : memory array, SA : Sense amp.).

This paper is organized as follows. Section II describes the conventional and proposed designs for BL path. Circuit operation is discussed in detail. Effectiveness of the proposed design over the conventional one is shown based on nominal design parameters. Section III discusses potential issues when the proposed circuit is implemented in NAND Flash, i.e., the overhead of the area for additional circuits, the delay time for switching the power supply for BL path from VDD to VDDQ and vice versa, and the noise immunity with VDDQ for BL voltages. Section IV presents the scalability of power on VDDQ and C_{BL}. Section V summarizes the results.

II. Conventional vs. Proposed Circuits

Conventional and proposed BL and I/O paths are illustrated in Fig. 3 (a) and (b), respectively. The operation of the conventional circuit is explained first. The readout flow of NAND flash is divided into the pre-charge and sense periods. In the pre-charge period, BL and the sensing node (SN) are charged from VDD through a voltage regulator. Pass transistors limit BL voltages to about 0.5V. At the same time, word-lines (WLs) are driven so that the current corresponding to the cell data flows in the memory cells.

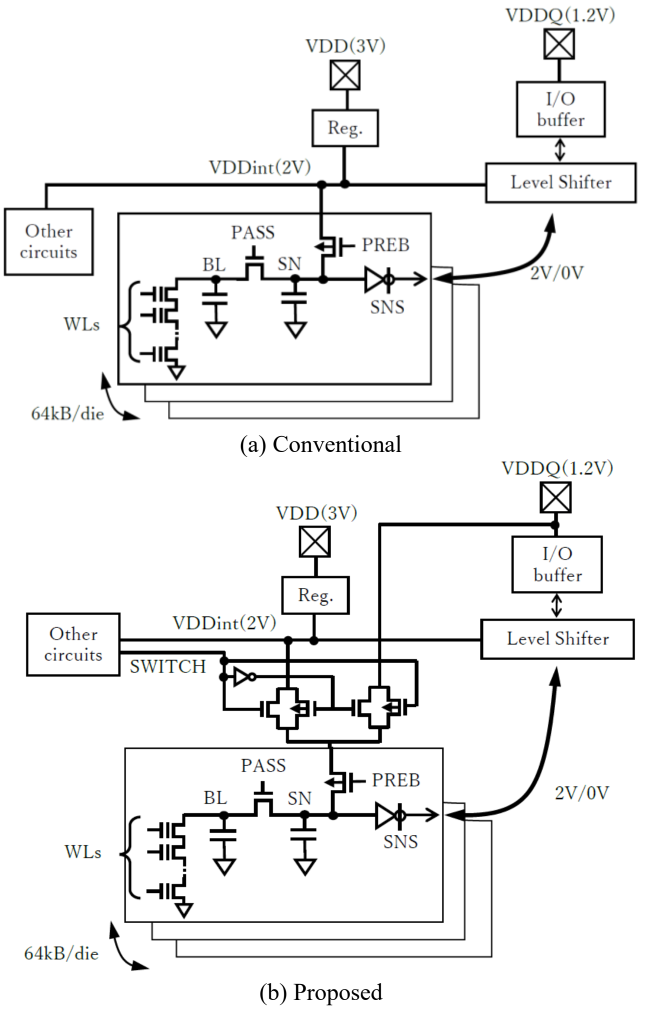

Fig. 3. (a) Conventional and (b) proposed BL and IO paths.

A difference between "0"- and "1"-cell currents causes a slight potential difference in BL, which is amplified from BL voltages to SN voltages with the source follower transistors. The sense period starts with the SN nodes disconnected from VDDint. The pass transistors flow the current as much as the cell current. Thus, the SN nodal voltages for the BLs which are connected with "1" cells decrease much faster that those with "0" cells. Thus, the cell data can be sensed. The signals with a voltage swing of 2V is converted to those with a voltage swing of VDDQ by the level shifters for I/Os. As shown in Fig. 3 (b), the proposed circuit adds the switches between VDDint and VDDQ. In order to reduce the power consumption in the BL path, the charges to BLs in the pre-charge period come from VDDQ rather than VDD.

TABLE I. Design Parameters Used in This Study

Param.	Description	Value	Unit
VDD	Power supply for control circuits	3.0	V
VDDQ	Power supply for I/O circuits	1.2	V
C_{BL}	BL capacitance	3.0	pF
C_{SN}	SN capacitance	0.1	pF
R_{BL}	BL resistance	3.0	MΩ
V_{BL0}	BL charge voltage of data "0"	0.5	V
V_{BL1}	BL charge voltage of data "1"	0.4	V
V_{pass}	Pass gate voltage	1.0	V
I_{cell0}	Memory cell current in data"0"	0	nA
I_{cell1}	Memory cell current in data"1"	100	nA
T_{pre}	Pre-charge time	5.0	µs
T_{ch}	SN boost time	100	ns

SN nodes are pre-charged to VDDQ of 1.2V, which is lower by 0.8V than that of the conventional circuit. Before the sensing operation starts, the pre-charge voltage at SN nodes need to be increased to 2.0V to keep the sensing margin as large as the conventional circuit. VDDBL is disconnected from VDDQ and connected with VDDint. One only needs to add the switches in each die. In addition, it can be implemented regardless of the readout method such as ABL or SBL [3], [4] or the circuits for improving readout accuracy [5], [6]. As a result, the proposed circuit can be used commonly.

In this study, numerical values to estimate the energy per read operation is only for one BL based on the design parameters shown in Table I. The energy is estimated in both the pre-charge and sense periods. In the conventional circuit, BL and SN are charged with VDDint. The energy for charging the BL capacitance and that for supplying the cell current are calculated, independently, with (Capacitance) × (Voltage swing) × (Supply voltage) and with (Cell current) × (Time) × (Supply voltage). As shown in Fig. 4, the total energy is estimated to be 6.0pJ and 2.4pJ with the conventional and proposed circuits. The difference in the total energy only comes from that in the supply voltages.

Let's take a look at the sense period. In the conventional circuit, after the BL pre-charge operation is completed, the supply from VDD stops so that no current flows through the pass transistor and therefore V_{SN} at 2.0V when the data is "0" On the other hand, the current flows from SN to BL when the data is "1". Even though the current flows from SN to BL when the data is "1", there is no energy consumption because VDD is disconnected, as shown in Fig. 5 (a). On the other hand, in the proposed circuit, SN needs to be increased from 1.2V to 2V before the sensing operation starts, in order to have the same sensing margin as the conventional circuit does.

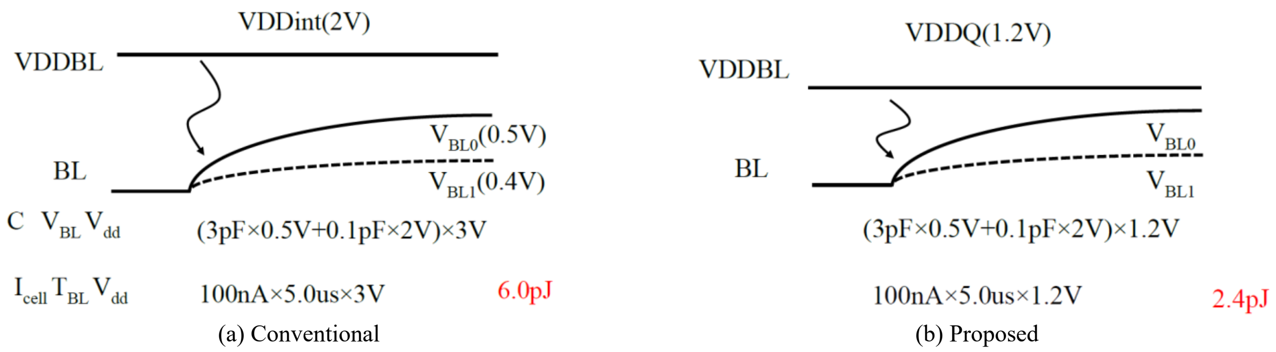

Fig. 4. Pre-charge operation.

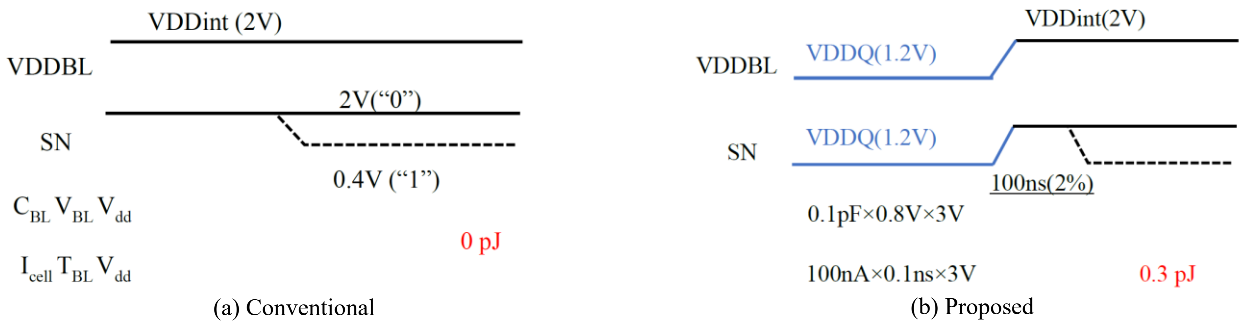

Fig. 5. Sense operation.

The switching time required for increasing the SN voltage to 2.0V is estimated to be as short as 0.1µs. VDD needs to supply the charges to SN as well as the cell current. Therefore, a total energy is estimated to be 0.3pJ, as shown in Fig. 5 (b). As a result, the energy required for a single read cycle is 6.0pJ with the conventional circuit and 2.7pJ with the proposed circuit. This means that the power consumption for BL pass can be reduced by 60% and the power consumption of the chip can be reduced by 30%, assuming that the power consumption for the WL path is as high as that for the BL path. Potential issues in implementing the proposed circuit are the overhead of additional circuit area, the additional delay for switching and the noise immunity. The next section discusses them.

III. Trade-Offs : Area, Delay and Noise Immunity

To validate the effectiveness of the proposed circuit on power reduction, we designed the circuit in 65nm CMOS including the sensing circuits, the I/O circuits and the control circuit, as shown in Fig. 6. Based on this layout design, the actual additional switching circuit is estimated to require silicon area of $0.1mm^2$ in case of 64KB 4 plane operation, which is equivalent to 0.1% of a nominal die size of $100mm^2$. Standard NMOSFETs were used to mimic memory cells. Poly resistors and MIM capacitors were used instead of the parasitic resistance and capacitance of BLs, respectively. The control circuit internally generates all the control signals with an external single clock. An additional control signal switches the timing for the conventional circuit and that for the proposed one. Fig. 7 (a) shows a circuit model of BL path for SPICE simulation. Figs. 7 (b) and (c) show the conventional and proposed control signals, respectively. In the conventional circuit mode, VDDBL stays at 2.0V for entire operation. BL operation starts with PREB low. Depending on the cell current, BL voltage goes up to about 0.5V for "0" and about 0.4V for "1". With PREB high, SN nodes are discharged. The difference in SN voltages is amplified and the digital data is latched with SNS high. In the proposed circuit mode, BL pre-charge starts with PREB low and VDDBL switched to 1.2V VDDQ. BL is charged up with VDDQ, resulting in power reduction. Sensing operation starts with PREB high right after VDDBL is charged up to VDDint of 2V. By skewing the timing difference between the clock edges in VDDBL and SNS, we confirmed that a short time of 100ns was sufficient. It was also validated that the additional switch resistance affected no visible impact on BL pre-charging time because the BL pre-charge current is limited by the pass transistors operating in saturation regions. The SPICE simulation also confirmed a power reduction in BL path of 60% with the proposed circuit. Intentional noises were injected into VDDQ to validate whether the circuit has sufficient noise immunity. A noise amplitude of 0.1V with frequency of 100MHz – 1GHz affected BL voltages with only a few mV in SPICE simulation.

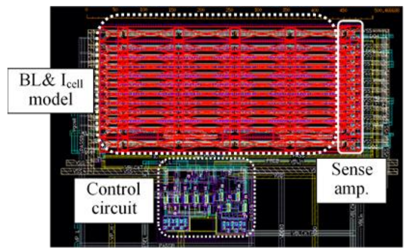

Fig. 6. Layout view of the proposed BL path.

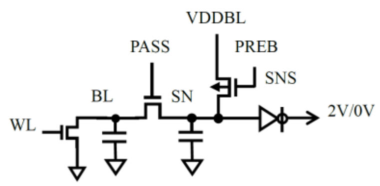

Fig. 7. (a) Circuit model for SPICE simulation

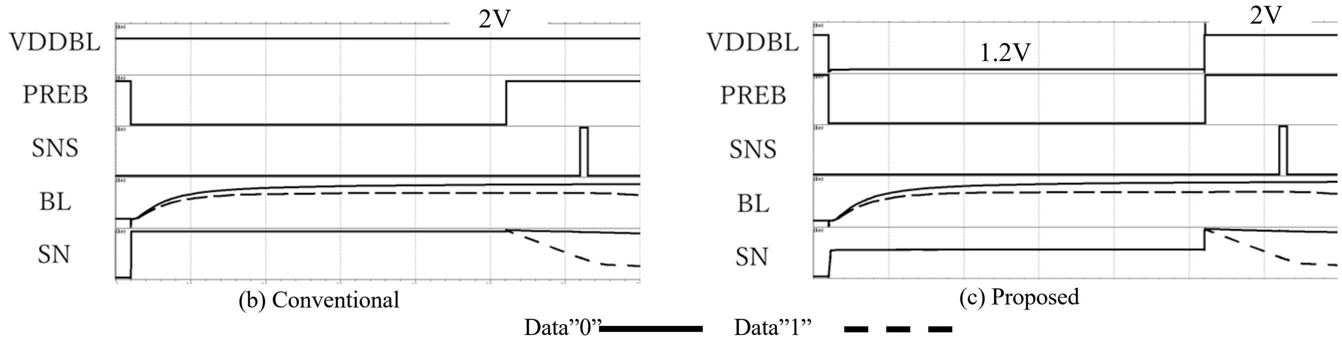

Fig. 7. Signal waveforms of the conventional circuit (b) and of the proposed circuit (c).

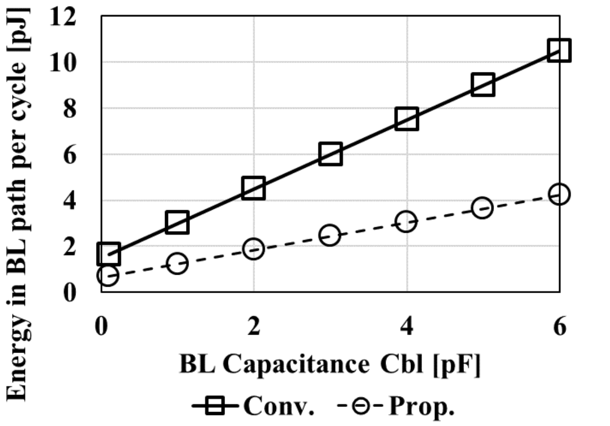

Fig. 8. Comparison of energy between conventional and proposed circuits when C_{BL} is changed

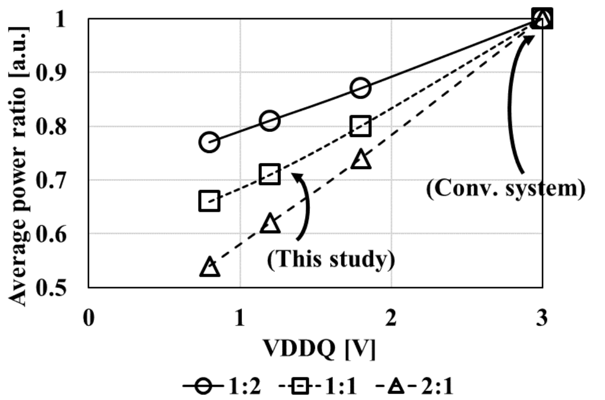

Fig. 9. Average power reduction vs. VDDQ when the proposed design is used. The ratio between BL and WL path energy is assumed to be 1:2, 1:1, or 2:1.

IV. Scalability

BL capacitance was assumed to be 3.0pF in this study. How significant is the BL capacitance on BL path energy? Fig. 8 compares the BL path energy as a function of BL capacitance. It is found that the proposed design can reduce BL path energy by 60% even if the BL capacitance varies from 0.1pF to 6pF. The ratio between BL and WL path energy was assumed to be 1:1 in this study. How significant is the energy per read operation? Fig. 9 shows that the average power can be reduced to be 20% for 1:2 or 40% for 2:1. It is clear that reduction in VDDQ in the future contributes to the average power reduction with the proposed design.

TABLE II. Estimated Feature Comparison

	BL path without Vddq	BL path with Vddq
BL charge voltage	VDD (3V)	VDDQ (1.2V)
S/A voltage in sense period	VDDint (2V)	VDDint (2V)
Power	1	0.7
BL delay time	1	1.02
Chip size	1	1.001

V. Conculusion

Table II summarizes the comparison between the conventional and proposed circuits. In the proposed circuit, the power consumption for BL path is reduced by 60% by utilizing 1.2V power supply for high-speed I/O instead of 3V power supply for peripheral circuits during BL charging. The overall chip power can be reduced by 30%. The overhead of the switching circuit on the BL delay from 2V VDDint to 1.2V VDDQ is 2% of the total read operation time. The additional circuit only requires 0.1% of each chip. The proposed circuit is a general-purpose system that can be implemented in any NAND chips with various sensing methods such as SBL/ABL in any SSDs because of no change in NAND interface.

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