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Article

Modeling of Cross-Coupled AC–DC Charge Pump Operating in Subthreshold Region

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Abstract: This paper proposes a circuit model of Cross-Coupled CMOS AC – DC Charge Pump (XC – CP) operating in subthreshold region. The aim is improving the efficiency to design XC – CPs with variety of specifications, e.g., input and output voltages and AC input frequency. First, it is shown that the output resistance (*Ro*) of XC – CP is much higher than those of CPs with single diodes (SD – CP) and ultra-low-power diodes (ULPD – CP) as charge transfer switches (CTSs). Second, the reason behind the above feature of XC – CP is identified by a simple model that the gate-to-source voltages of CTS MOSFETs are independent of the output voltage of the CP. Third, high but finite *Ro* of XC – CP is explainable with a more accurate model that includes the dependence of the saturation current of MOSFETs operating in subthreshold region on the drain-to-source voltage which is a function of the output voltage of CP. The model was in good agreement with measured and simulated results of XC – , SD – and ULPD – CPs fabricated in 250 nm CMOS.

Keywords: AC–DC; RF–DC; charge pump; rectenna; wireless power transfer; IoT; energy harvesting

1. Introduction

AC – DC charge pumps (CPs) are used to convert AC input power to DC output power for microwave wireless power transmission (MWPT) or RF energy harvesting (RF – EH) [1–11], biomedical application [12–16] and (c) vibration energy harvesting [17–20], as shown in Figure 1 (a) – (c). Figure 1 (d) illustrates a circuit diagram of CP composed of multiple rectifiers and capacitors connected in series between the input and output terminals. The capacitors are driven by differential signals *CLK* and *CLKB*, alternately. A filtering capacitor is connected at the output terminal to generate a DC voltage. The DC voltage is used for the following circuit blocks or ICs such as sensors and RF ICs in IoT edge modules or medical devices. The rectifier used in AC – DC CPs was originally a diode-connected single MOSFET [21–23], as shown in Figure 2(a). When the amplitude of the input AC voltage is low in low power systems, reverse leakage becomes significant concern. To reduce the reverse leakage current, ultra-low-power diodes were proposed and used in low power AC – DC CPs [24–26], as shown in Figure 2(b). To boost the gate voltages of switching MOSFETs for increasing the forward current, cross-coupled CMOS or CMOS latch has been widely used [27–34], as shown in Figure 2(c).

The frequency of AC signals is spread depending on use cases. MWPT utilizes ISM bands such as 920 MHz [1 – 3], 2.4 GHz [4 – 7], 5.8 GHz [8 – 9], and 24 GHz [10 – 11]. To have low tissue attenuation, ultrasound with moderate frequencies of 6.78 MHz and 13.56 MHz is used for biomedical application [12–16]. Fundamental resonant frequency used for vibration energy harvesting is nominally at 1 –100Hz [17 – 20]. Thus, improving the efficiency to design AC – DC CPs is required. A circuit model plays a key role to improve the design efficiency. Models for AC – DC CPs with single diodes have been developed in [25–40]. DC – DC CPs with cross-coupled CMOS operating in triode region was modeled in [41]. However, the output resistance of the CP (*Ro*) was given not specifically but by the traditional method of $N/fC\ coth(Ton/Ron\ C)$, where N is the number of stages, f clock frequency, C stage capacitance, Ton the period that the MOSFET turns on, Ron on-resistance of the MOSFET.

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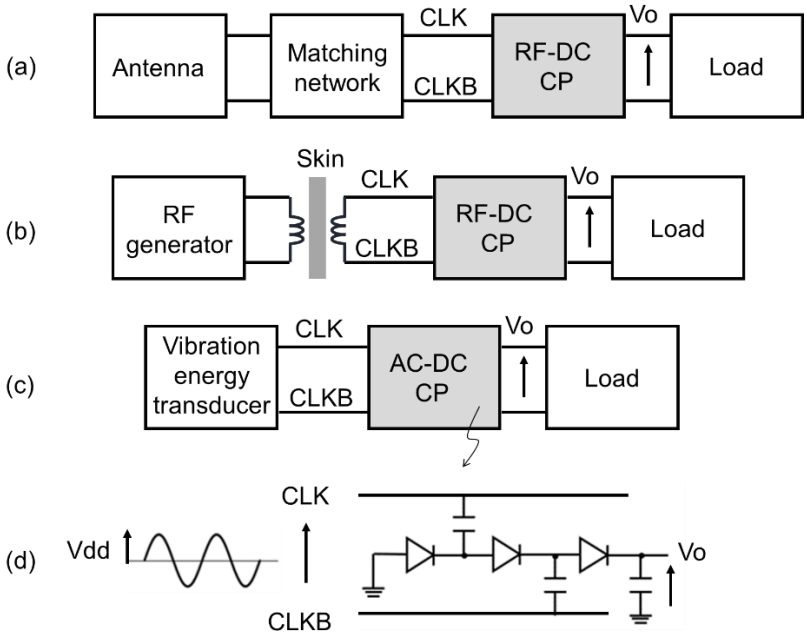

Figure 1. Applications of AC – DC/RF – DC CPs ((a) Microwave wireless power transmission or RF energy harvesting, (b) biomedical application, (c) vibration energy harvesting) and (d) circuit diagram of CP.

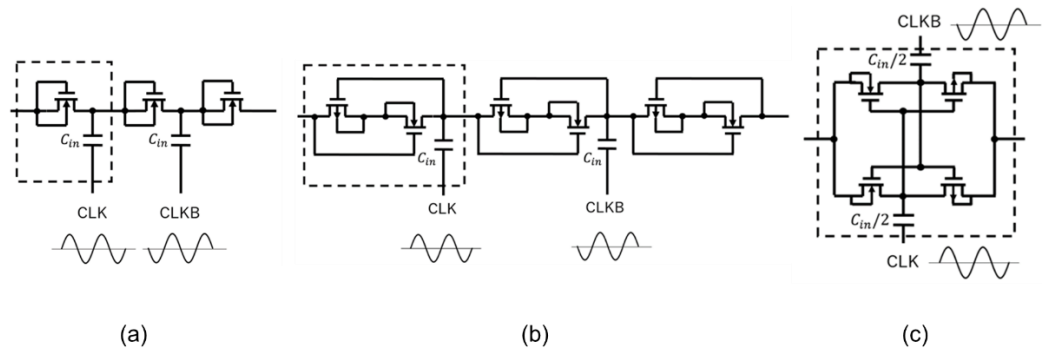

Figure 2. AC – DC CPs with diode-connected MOSFETs (a), ultra-low-power diodes (ULPDs) (b) and cross-coupled CMOS or CMOS latch (c).

To directly take a look at differences in *Ro* among SD – CP, ULPD – CP and XC – CP, SPICE simulation was done using the design parameters in 65nm CMOS as shown in Table 1, resulting in Figure 3. Surprisingly, *Ro* of XC – CP was 3X higher than those of SD – CP and ULPD – CP. As a result, the previous model [39,40] needs to be modified to predict high *Ro* for XC – CP.

Table 1. Design parameters for Figure 3.

Parameter	Symbol	Value
Clock frequency	*f*	1 GHz
Number of stages	*N*	32
Stage capacitance	*C*	100 fF
Clock amplitude	*Vdd*	400mV

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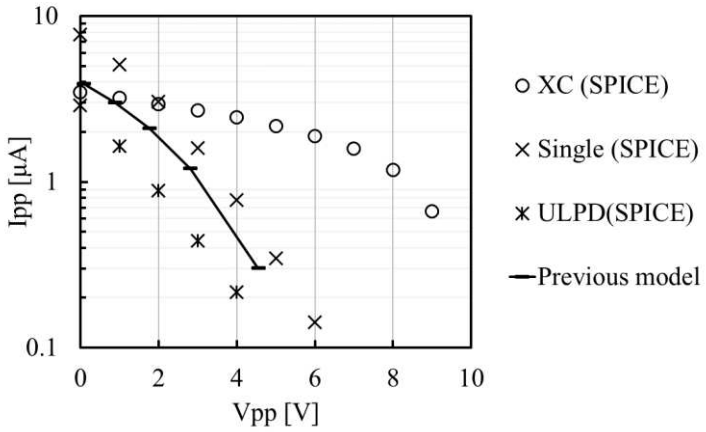

Figure 3. Output voltage *Vpp* – output current *Ipp* under the condition of Table 1.

This paper proposes a circuit model of cross-coupled CMOS AC – DC charge pump (XC – CP) operating in subthreshold region. The aim is improving the efficiency to design XC – CPs with variety of specifications, e.g., input and output voltages and AC input frequency. First, it is shown that the output resistance (R_O) of XC-CP is much higher than those of CPs with single diodes (SD – CP) and ultra-low-power diodes (ULPD – CP) as charge transfer switches (CTSs). Second, the reason behind the above feature of XC-CP is identified by a simple model that the gate-to-source voltages of CTS MOSFETs are independent of the output voltage of the CP. Third, high but finite R_O of XC – CP is explainable with a more accurate model that includes the dependence of the saturation current of MOSFETs operating in subthreshold voltage on the drain-to-source voltage which is a faction of the output voltage of CP. The model was in good agreement with measured and simulated results of XC –, SD – and ULPD – CPs fabricated in 250 nm CMOS.

This paper is composed of the following sections. Section 2 shows the characteristics and schematics of rectifiers composing each stage to be optimized. Section 3 presents fabricated circuits and measurement results. Section 4 summarizes this research.

2. Modeling of cross-coupled CMOS AC – DC charge pump (XC – CP) operating in subthreshold region

This section starts with the review of the previous AC – DC CP model [39], [40] and proposes a new one for XC – CP operating in subthreshold region. Table 1 summarizes the circuit parameters of the XC – CP.

Table 2. Definition of design parameters.

Parameter	Description	Parameter	Description
f	Frequency of input power	I_S	Saturation current of MOSFET operating in subthreshold region
V_{in}	Input AC voltage of XC–CP	C	Stage capacitor (capacitance per stage)
V_{dd}	Amplitude of V_{in}	N	Number of stages
V_{PP}	Output DC voltage of XC–CP	R_O	Output resistance of CP
I_{PP}	Average output current of XC–CP	I_{SC}	Short circuit current of CP
V_T	Effective thermal voltage	V_{OC}	Open circuit voltage defined by $R_O I_{SC}$

(2-1) Previous model of AC – DC CP [39], [40]

Figure 4a illustrates a sub-circuit of XC – CP to define the nodal voltages V_n and V_{n+1}. CLK and CLKB have the voltage amplitude of $V_{dd}/2$. Figure 4b shows the waveform of V_n and V_{n+1}.

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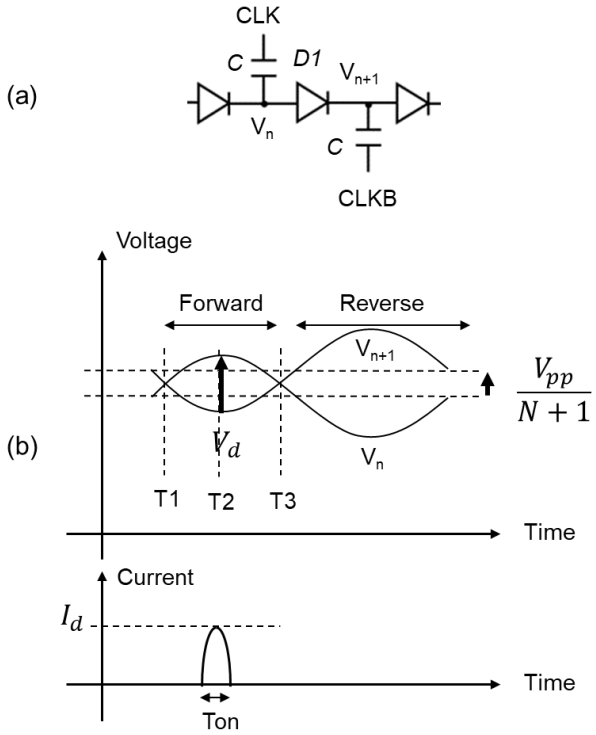

Figure 4. Nodal voltages V_n and V_{n+1} of neighboring stages (a) and their waveform (b).

The charge transfer switch (CTS) or rectifying diode D1 operates forward bias regime between T1 and T3 and reverse bias one after T3. The peak forward voltage appears around the middle of the time period between T1 and T3, namely T2. V_1 and V_2 at T2 can be expressed by $V_{dd}/2 - I_{pp}/fC$ and $V_{dd}/2 + I_{pp}/fC + V_{pp}/(N+1)$, respectively, where $V_{dd}/2$ is the clock amplitude of each of CLK and CLKB when the top plate parasitic capacitance is ignored for simplicity, I_{pp} is the output current, I_{pp}/fC is a voltage shift due to the amount of transferred charges I_{pp}/f in steady state, and $V_{pp}/(N+1)$ is the DC offset between the next neighbor capacitor nodes. As a result, the voltage difference at the peak points of V_n and V_{n+1} at T2 (V_d,) is given by (1).

$$V_d = V_{dd} - \frac{2I_{pp}}{fC} - \frac{V_{pp}}{N+1} \tag{1}$$

When the CTS MOSFET operates under subthreshold region, the drain-to-source current I_d is expressed by (2), where I_S is the saturation current, V_{gs} the gate-to-source voltage, and V_T the effective thermal voltage.

$$I_d = I_s e^{\frac{V_{gs}}{V_T}} \tag{2}$$

With a conduction angle γ defined by Ton / Tc, i.e., (3), the average output current I_{pp} can be expressed by (4).

$$\gamma = cos^{-1}\left(1 - \frac{2I_{pp}}{fCV_{dd}}\right) \tag{3}$$

$$I_{pp} = \frac{\gamma}{\pi} I_d \tag{4}$$

When V_{gs} is equal to V_d as in a single-MOSFET CTS, from (1), (2) and (4), one can result in $V_{pp} - I_{pp}$ relationship (5).

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$$I_{pp} = \frac{2}{\pi}\sqrt{\frac{I_{pp}}{fCV_{dd}}}I_s e^{\frac{V_{dd}-\frac{2I_{pp}}{fC}-\frac{V_{pp}}{N+1}}{V_T}} \tag{5}$$

"Previous model" in Figure 3 is given by (5). One can numerically calculate V_{pp} with a certain value input to I_{pp}.

(2-2) Proposed model of XC – CP

Figure 5 (a) illustrates next neighbor two-stages of XC – CP. Because each stage has two capacitors, the capacitance of each capacitor is designed to be $C/2$ so that the total capacitance per stage is the same as the other CPs. The peak voltage difference V_d between the next neighbor capacitors is the sum of V_{ds} of PMOSFET and NMOSFET, i.e., $2V_{ds}$. Figure 5 (b) shows V_{gs} and V_d at the peak points. When the stage at the right half of Figure 5 (a) is the second stage, V_{2D} and V_{2U} are given by $-V_{dd}/2 + I_{pp}/fC + V_{pp}/(N+1)$ and $V_{dd}/2 - I_{pp}/fC + V_{pp}/(N+1)$, respectively.

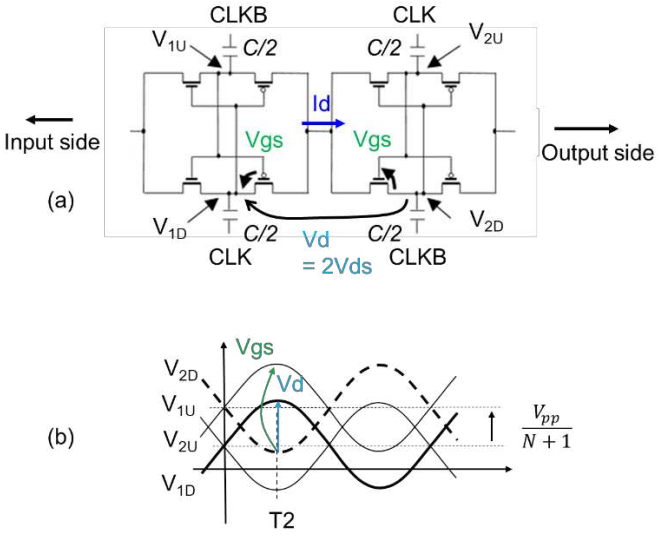

Figure 5. Sub-circuit of XC – CP (a) and waveform of nodal voltages (b).

Thus, $V_{gs} = V_{2U} - V_{2D}$ is given by (6).

$$V_{gs} = V_{dd} - \frac{2I_{pp}}{fC} \tag{6}$$

V_d is given by (1) as well as SD – CP. Assuming NMOSFET has the drain-to-source current as large as PMOSFET does, the peak current from one capacitor to the next is given by (7).

$$I_d = I_s e^{\frac{V_{gs}}{V_T}}\left(1 - e^{-\frac{V_{ds}}{V_T}}\right) \tag{7}$$

Charge transfer occurs in every half cycle, resulting in (8).

$$I_{pp} = \frac{2\gamma}{\pi} I_d \tag{8}$$

From $V_d = 2V_{ds}$ and (6) – (8), a subthreshold XC – CP model is given by (9).

$$I_{pp} = \frac{2\gamma I_s}{\pi} e^{\frac{V_{dd}-\frac{2I_{pp}}{fC}}{V_T}}\left(1 - e^{-\frac{V_{dd}-\frac{2I_{pp}}{fC}-\frac{V_{pp}}{N+1}}{V_T}}\right) \tag{9}$$

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When $V_{ds} \gg V_T$, (9) is reduced to be (10). Because it has no V_{pp} term, it indicates that a subthreshold XC – CP is a current source with an infinite output resistance. This fact is originated by (6) which has no dependency on V_{pp}.

$$I_{pp} = \frac{2\gamma I_s}{\pi} e^{\frac{V_{dd} - \frac{2I_{pp}}{fC}}{V_T}} \tag{10}$$

(2-3) More accurate model with a finite output resistance

Even though (10) can express a large output resistance, it needs modification to have a finite output resistance rather than an infinite one. Figure 6(a) shows $I_{ds} - V_{gs}$ of an NMOSFET in 250 nm CMOS, which suggests that I_s has dependency on V_{ds}, namely drain-induced barrier lowering. Based on the data of Figure 6(a), $I_s - V_{ds}$ was plotted in Figure 6(b). The curve is well fit with $I_S = 18.4\ e^{10.7\ V_{ds}}$ in nA.

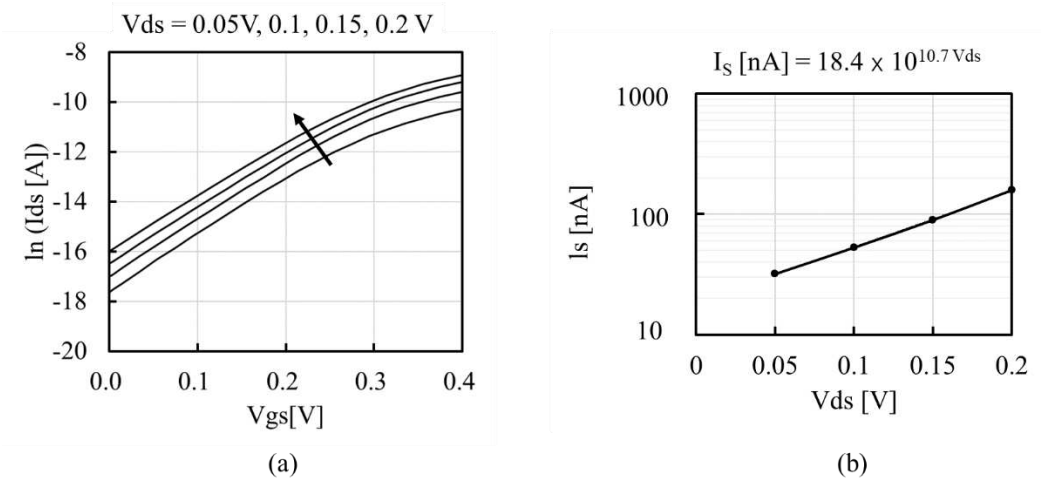

Figure 6. $I_{ds} - V_{gs}$ (a) and an extracted $I_s - V_{ds}$ (b) of an NMOSFET in 250 nm CMOS.

Assuming the $I_s - V_{ds}$ curve can be generally described by (11), (10) and (9) can be revised as (12) and (13), respectively.

$$I_s = I_{s0} e^{\frac{V_{ds}}{\eta V_T}} \tag{11}$$

$$I_{pp} = \frac{2\gamma I_{s0}}{\pi} e^{\frac{(1+\frac{1}{2\eta})(V_{dd} - \frac{2I_{pp}}{fC}) - \frac{V_{pp}}{2\eta(N+1)}}{V_T}} \tag{12}$$

$$I_{pp} = \frac{2\gamma I_{s0}}{\pi} e^{\frac{(1+\frac{1}{2\eta})(V_{dd} - \frac{2I_{pp}}{fC}) - \frac{V_{pp}}{2\eta(N+1)}}{V_T}} \left(1 - e^{-\frac{V_{dd} - \frac{2I_{pp}}{fC} - \frac{V_{pp}}{N+1}}{V_T}}\right) \tag{13}$$

Figure 7 compares $V_{pp} - I_{pp}$ between SPICE and models (10), (12), (13) at Vdd = 200 mV when XC – CP is designed with the parameters in Table 3. The three CPs were fabricated with those design parameters which will be discussed in Section 3. Even though the short circuit current at Vpp = 0V had discrepancies from the SPICE result, the output resistance of Model (13) was in better agreement with SPICE than Model (12).

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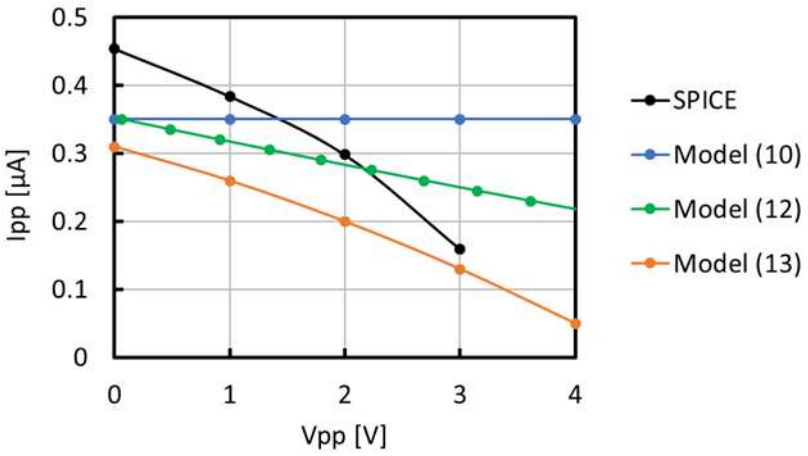


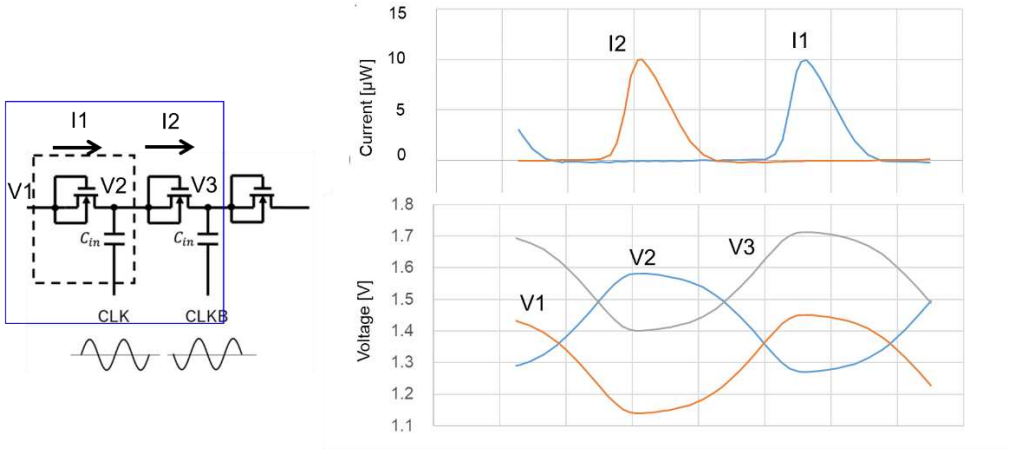
Figure 7. Comparison of V_{pp} – I_{pp} between SPICE and models (10), (12), (13).

Table 3. Design parameters for Figure 7 and used for the fabricated CPs which will be discussed in Section 3.

Parameter	Symbol	Value
Clock frequency	f	1 MHz
Number of stages	N	24
Stage capacitance	C	10 pF
Clock amplitude	Vdd	400mV, 200mV, 50mV

3. Validation of the proposed model

XC – CP, SD – CP and ULPD – CP were designed in 250nm CMOS with the parameters shown in Table 3. Figures 8–10 respectively show simulated waveforms at 12th and 13th stages when *Vdd* is 400 mV and *Vpp* is 3.0V. Note that V3, N- and P-well voltage, of XC – CP in Figure 9, and V2 and V4, N- and P-well voltages, of ULPD – CP in Figure 10, are much more stable than V1 – V3 of SD – CP as shown in Figure 8. I1 and I2 of ULPD – CP become negative in a cycle time, but those are due to AC current to the gate of CTS transistors, not actual leakage current.



(a) (b)

Figure 8. 12th and 13th stages of SD – CP (a) and their waveforms (b).

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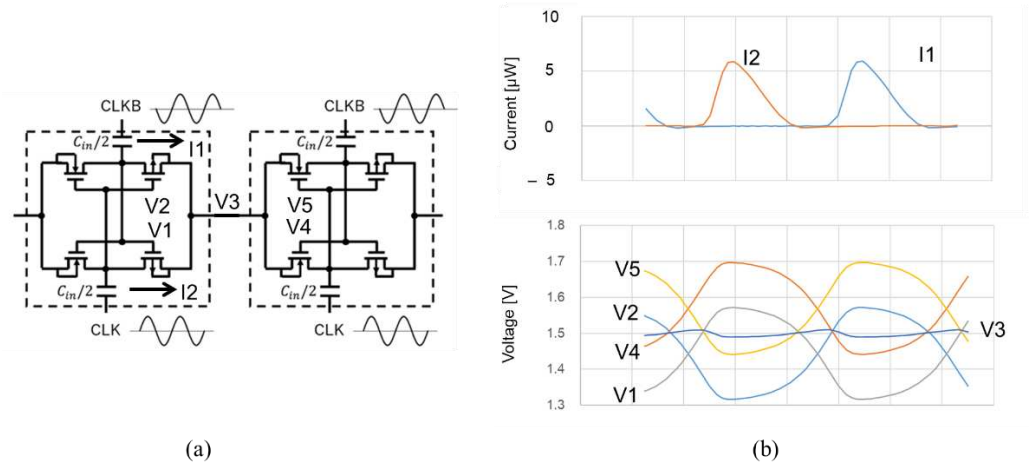
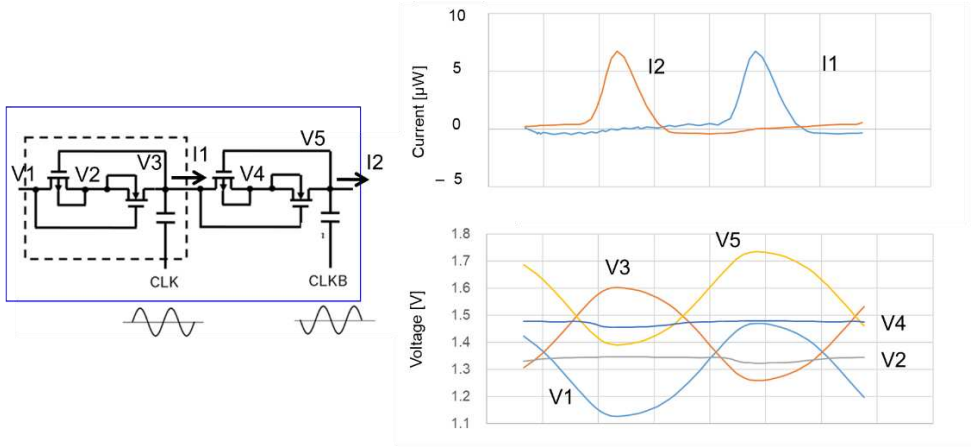


(a) (b)

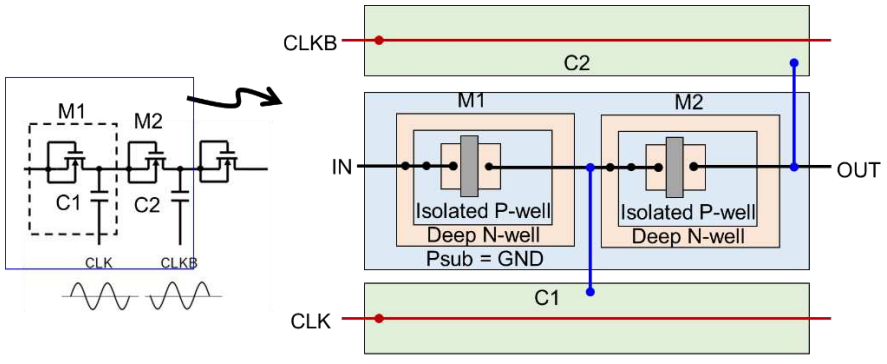
Figure 9. 12th and 13th stages of XC – CP (a) and their waveforms (b).



(a) (b)

Figure 10. 12th and 13th stages of ULPD – CP (a) and their waveforms (b).

XC – CP, SD – CP and ULPD – CP were fabricated in 250nm CMOS to validate the proposed model. Figures 11–13 respectively illustrate layout design for those three CPs.



(a) (b)

Figure 11. Layout unit of SD – CP (a) and its layout design (b).

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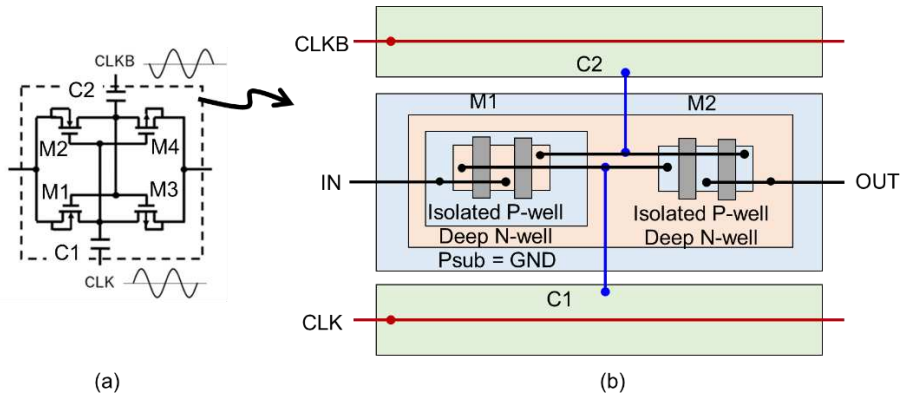

Figure 12. Layout unit of XC – CP (a) and its layout design (b).

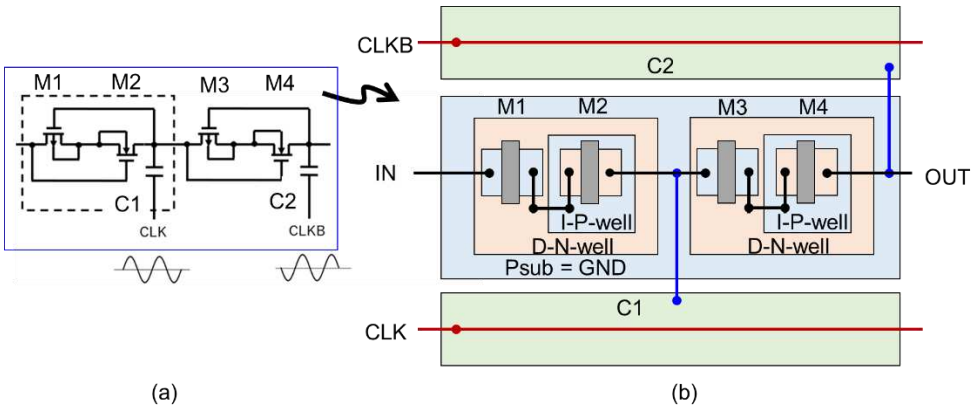

Figure 13. Layout unit of ULPD – CP (a) and its layout design (b).

NMOSFETs were formed in the triple well to isolate their P-well from P-substrate. Deep N-well of the NMOSFET is shared with N-well for PMOSFET to minimize the parasitic capacitance for XC and ULPD CPs. To route wires for CLK and CLKB with minimal length, adjacent two stages are laid out by placing two capacitors at top and bottom of the cell. The CTS is placed in the middle. The cell width is determined by the CTS and the cell height is determined by the two caps and the CTS.

Figure 14 shows die photo. Each CP has 24 stages with a stage capacitor of 10 pF. Because of difference in CTS size of three CPs, XC, ULPD and SD CPs have entire size of 0.48mm^2, 0.49mm^2 and 0.44mm^2, respectively.

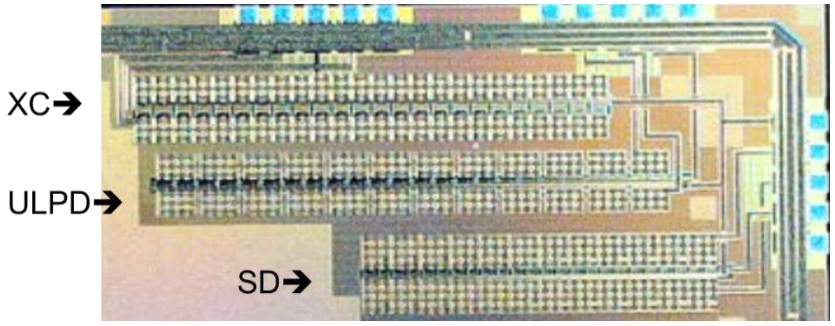

Figure 14. Die photo.

Figure 15 shows measured waveforms of the three CPs with *Vdd* of 200 mV, f of 1 MHz and a load resistance of 10 MΩ. The ripple voltages were below 6mV with a filtering capacitance of 22 pF.

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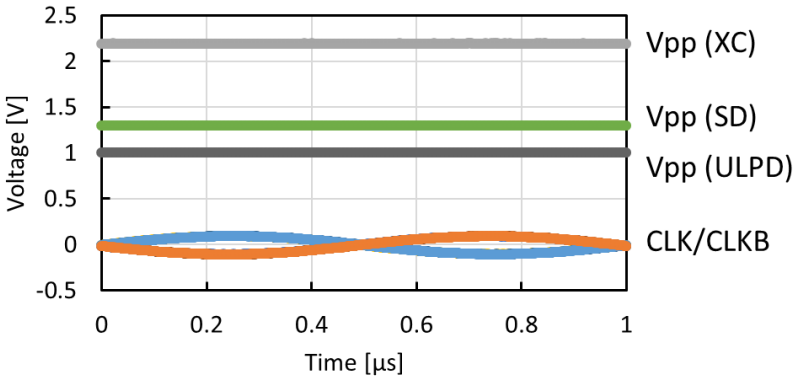

Figure 15. Measured waveform with *Vdd* of 200 mV and f of 1 MHz.

Vpp was measured with various *Vdd* and load resistance. Figures 16 compares *Vpp* – *Ipp* curves between XC, ULPD and SD with SPICE, measurement and model. Hereinafter, the models for XC and SD indicate (13) and (5), respectively.

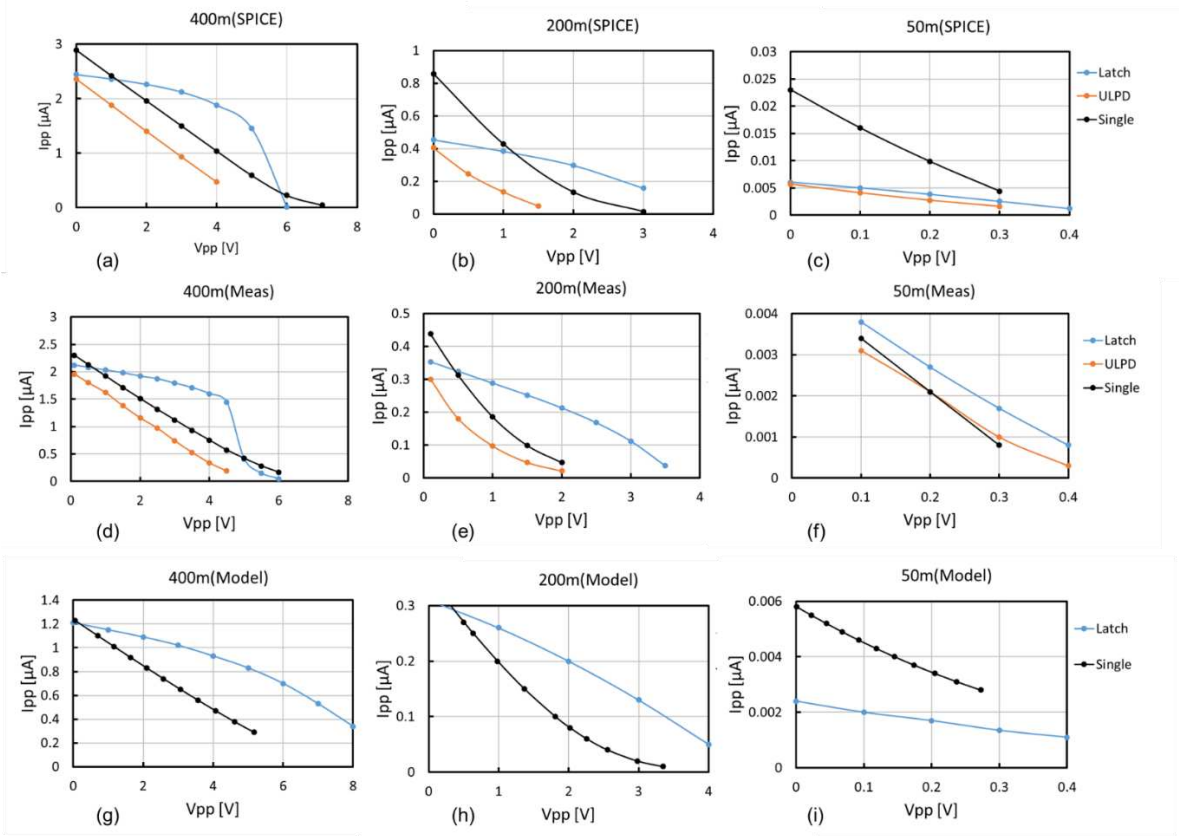

Figure 16. *Vpp* – *Ipp* characteristics: SPICE results with *Vdd* of 400 mV (a), 200 mV (b) and 50 mV (c); measured results with *Vdd* of 400 mV (d), 200 mV (e) and 50 mV (f); models with *Vdd* of 400 mV (g), 200 mV (h) and 50 mV (i).

Figures 16 (a) – (c) show the comparison of *Vpp* – *Ipp* curves given by SPICE simulation between XC, ULPD and SD at *Vdd* of 400 mV (a), 200 mV (b), and 50 mV (c). At *Vdd* of 400 mV or 200 mV, "Latch" or XC – CP had the highest *Ro* in a lower *Vpp* range, but *Ipp* suddenly collapsed at certain *Vpp*. The reason of that behavior has not been identified in this work, which will be determined in the following researches. *Isc* of SC was the highest among the three CPs at *Vdd* of 400 mV, 200 mV and 50 mV. At *Vdd* of 50 mV, *Ipp* of XC is as low as that of ULPD. At such a low *Vdd*, *Vds* of each CTS

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transistor may play a main role. *Vds* of each CTS transistor in XC and ULPD is half of that in SD. When *Vds* goes below V_T, (7) indicates that *Ids* is reduced as *Vds* decreases.

Figures 16 (d) – (f) show the comparison of *Vpp* – *Ipp* curves given by measurement between XC, ULPD and SD at *Vdd* of 400 mV (d), 200 mV (e), and 50 mV (f). *Vpp* – *Ipp* characteristics at *Vdd* of 400mV or 200mV between XC, ULPD and SD were very similar to those of SPICE results. Unlike SPICE results, *Ipp* values of the three CPs were about the same at *Vdd* of 50 mV.

Figures 16 (g) – (i) show the comparison of *Vpp* – *Ipp* curves given by the models between XC and SD at *Vdd* of 400 mV (g), 200 mV (h), and 50 mV (i). *Ipp* of XC was larger than SD when *Vdd* was 400mV or 200mV whereas *Ipp* of XC was smaller than SD when *Vdd* was 50mV. Those trends were similar to SPICE results.

Figures 17 compares *Vpp* – *Ipp* curves between SPICE, measurement and model. Figures 17 (a) – (c) show the comparison of *Vpp* – *Ipp* curves of XC – CP at *Vdd* of 400 mV (a), 200 mV (b), and 50 mV (c). The proposed model (13) was in good agreement with SPICE and measured within a factor of 3 in the swept ranges of *Vpp* and *Vdd*. The model was not succeeded to show sudden collapse at a certain *Vpp* with *Vdd* of 400mV. Figures 17 (d) – (f) show the comparison of *Vpp* – *Ipp* curves of ULPD – CP at *Vdd* of 400 mV (d), 200 mV (e), and 50 mV (f). SPICE and measured results were well matched in terms of the open circuit voltage and within a discrepancy of 20% in terms of *Ro*. Figures 17 (g) – (i) show the comparison of *Vpp* – *Ipp* curves of SD – CP at *Vdd* of 400 mV (g), 200 mV (h), and 50 mV (i). *Ro* had discrepancies from SPICE and measured by a factor of two at *Vdd* of 400mV and was in good agreement with measured at *Vdd* of 200mV and 50mV. The discrepancy in *Ro* between SPICE and measured increases as *Vdd* decreases in comparison with XC and ULPD.

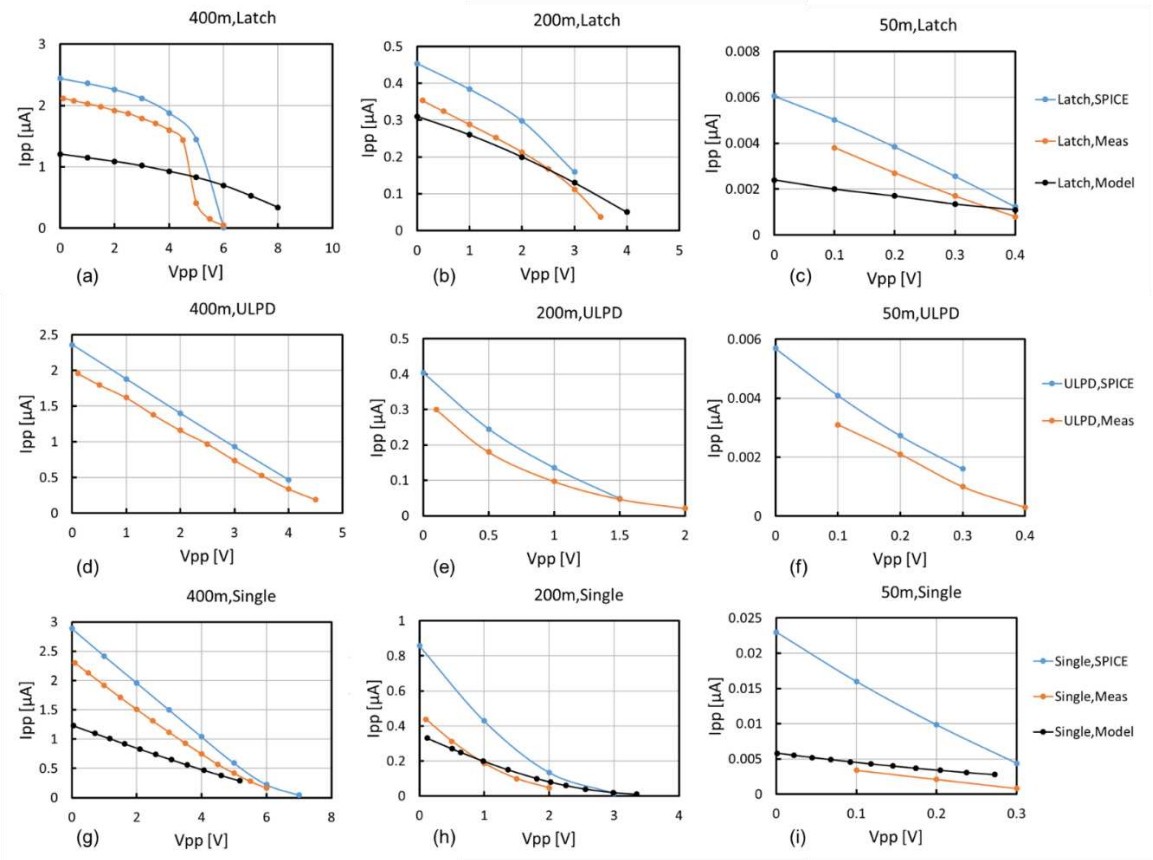

Figure 17. *Vpp* – *Ipp* characteristics: XC – CP (Latch) with *Vdd* of 400 mV (a), 200 mV (b) and 50 mV (c); ULPD – CP with *Vdd* of 400 mV (d), 200 mV (e) and 50 mV (f); SD – CP (Single) with *Vdd* of 400 mV (g), 200 mV (h) and 50 mV (i).

Figures 18 (a) – (c) compare *Ro* (a), *Isc* (b) and *Voc* (c) of XC – CP between SPICE, measured and model (13) at three conditions of (*Vdd*, *Vpp*) = (400 mV, 2.5 V), (200 mV, 1.0 V), and (50 mV, 0.2 V). *Voc*

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of the model was closer to that of SPICE and measured than *Ro* and *Isc* of the model were. This means that the discrepancy in *Ro* of the model from SPICE and measured is as large as that in *Isc*. Figures 18 (d) – (f) compare *Ro* (d), *Isc* (e) and *Voc* (f) of SD − CP between SPICE, measured and model (5) at three conditions of (*Vdd*, *Vpp*) = (400 mV, 2.5 V), (200 mV, 1.0 V), and (50 mV, 0.2 V). Like XC − CP, *Voc* of the model was closer to that of SPICE and measured than *Ro* and *Isc* of the model were.

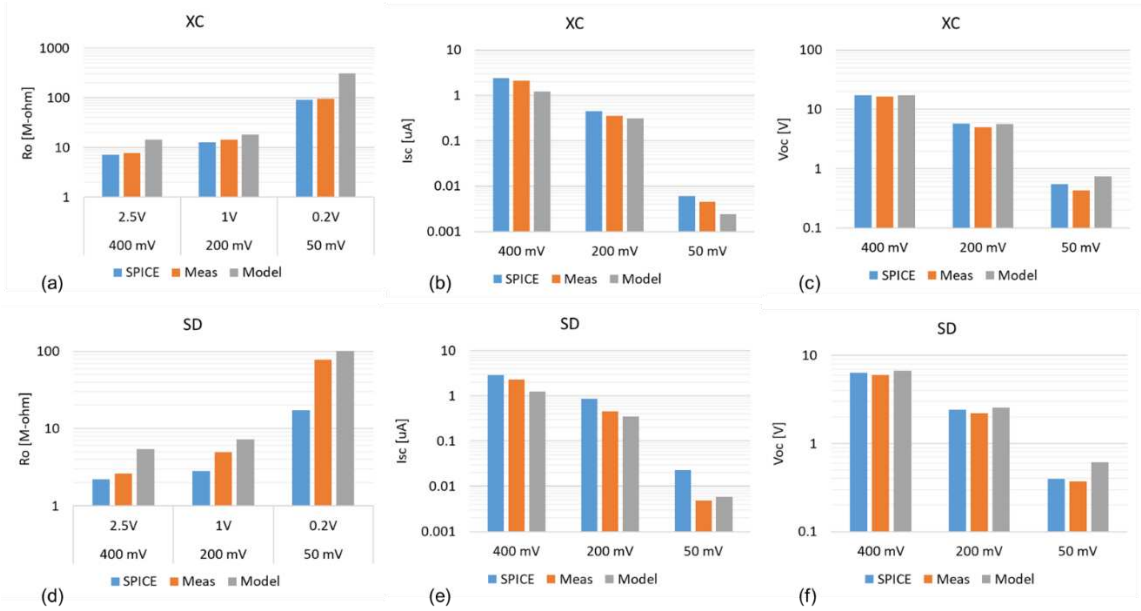

Figure 18. *Ro* (a), *Isc* (b) and *Voc* (c) of XC − CP and *Ro* (d), *Isc* (e) and *Voc* (f) of SD − CP between SPICE, measured and model (13) at three conditions of (*Vdd*, *Vpp*) = (400 mV, 2.5 V), (200 mV, 1.0 V), and (50 mV, 0.2 V).

Figures 19 (a) – (c) compare *Ro* (a), *Isc* (b) and *Voc* (c) of XC − CP normalized by those of SD – CP between SPICE, measured and model at the three conditions of (*Vdd*, *Vpp*) = (400 mV, 2.5 V), (200 mV, 1.0 V), and (50 mV, 0.2 V). From Figure 19 (a), except for the measured result at (*Vdd*, *Vpp*) = (50 mV, 0.2 V), *Ro* of XC – CP was larger than that of SD – CP by a factor of 2.5 or more. When the condition of (*Vdd*, *Vpp*) moved from (400 mV, 2.5 V) to (200 mV, 1.0 V) and from (200 mV, 1.0 V) to (50 mV, 0.2 V), the *Ro* ratio increased with SPICE whereas didn't with measured and model except for the measured result from (200 mV, 1.0 V) to (50 mV, 0.2 V). Figure 19 (b) shows that the *Isc* ratio decreased with SPICE and model whereas didn't with measured. Figure 19 (c) shows that the *Voc* ratios were in good agreement between SPICE, measured and model in those three conditions even though the *Ro* ratio and the *Isc* ratio had different tendency on the operation condition.

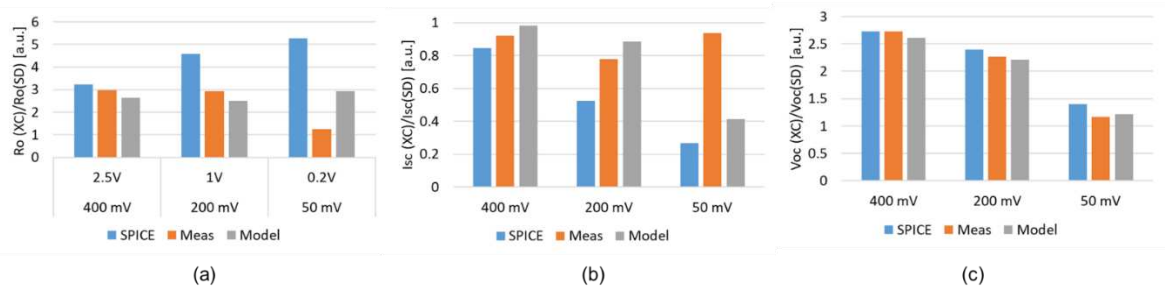

Figure 19. Comparison of *Ro* (a), *Isc* (b) and *Voc* (c) of XC − CP normalized by those of SD – CP between SPICE, measured and model at the three conditions of (*Vdd*, *Vpp*) = (400 mV, 2.5 V), (200 mV, 1.0 V), and (50 mV, 0.2 V).

6. Conclusions

In this paper, a circuit model of AC – DC charge pumps with subthreshold operation cross-coupled CMOS as charge transfer switch (CTS), namely XC – CP, was developed for circuit designers to use the model for determining the initial condition for SPICE simulation. It was observed that XC – CP had much higher output resistance than charge pumps with single NMOSFETs as CTS, namely SD – CP, did. The reason is that the gate-to-source voltage of the MOSFETs in XC – CP doesn't depend on the output voltage unlike SD – CP and charge pumps with ultra-low-power diodes (ULPDs) do. Very high but finite output resistance is resulted from weak but finite dependence of the drain-to-source voltage on the subthreshold current through drain-induced barrier lowering. In both SPICE simulation and measured results, the output current of XC– CP collapses at a certain output voltage. The developed model (13) doesn't predict that behavior. Further research is required to identify what made such behavior. To validate the proposed model, XC -, SD -, ULPD - CPs were fabricated in 250 nm CMOS. The output resistance predicted by the model was in good agreement with SPICE and measured within a factor of two at *Vdd* of 400 mV, 200 mV and 50 mV.

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