Article

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Low-Power Multi-Bit Delta-Sigma Modulator based on Passive and Attenuationless Summation Scheme

Rongshan Wei, Lijie Huang, Gongxing Huang, Renping Wang and Cong Wei *

School of Physics and Information Engineering, Fuzhou University, Fuzhou 350116, China;
weicong0504@163.com

* Correspondence: weicong0504@163.com; Tel.: +8615606095680

Abstract: In the field of delta-sigma modulators, reducing system power consumption without sacrificing accuracy has become a challenge. The summing circuit, as the main part of the cascade-of-integrator-in-feedforward delta-sigma modulator, consumes a significant amount of power in active summing. On the other hand, passive summing circuits have low power consumption but can cause attenuation in the summing results. This article proposes a low-power multi-bit delta-sigma modulator based on passive and attenuationless summation scheme. The summation circuit achieves multiplication of the voltage signal carried on the summation capacitor through bidirectional sampling technique, compensating for the inherent attenuation caused by passive summation, thus eliminating the need for active OTA to achieve perfect summation. A 2-order delta-sigma modulator based on 4-bit 1-order passive noise-shaping (NS) SAR quantizer is designed to verify the scheme. By combining a passive NS SAR as the 4-bit quantizer and the third-stage integrator of the system, and incorporating an energy-efficient cascode floating inverter amplifier (FIA) structure as the core active OTA, these elements have significantly enhanced the energy-efficiency of the modulator. Simulation results show that at a supply voltage of 1.2 V and a bandwidth of 20 kHz, the SNDR reaches 102.62 dB, power consumption is only 148.32 μW, and Schreier figure-of-merit (FoM) of SNDR is 183.92 dB.

Keywords: delta-sigma modulator; low power; passive summation; NS SAR; FIA

1. Introduction

With the rapid development of IoT, sensors powered by batteries are needed, so in addition to high accuracy, low power consumption is also an important requirement for delta-sigma modulators (DSM) [1–7]. Therefore, how to balance between high accuracy and low power consumption has become the focus of exploration in the field of delta-sigma modulators.

With the popularity of the full feedforward delta-sigma topology [8–11], the summation circuit has become an important component of multi-bit DSM. Conventional summation circuits use active operational transconductance amplifiers (OTAs) as the core to sum up the signals at each node of the circuit, consuming a large amount of active power [12–15]. In order to reduce this part of power consumption, passive summation schemes have been widely adopted. However, passive summation circuits directly parallel capacitors carrying the voltage signals of each branch [1,16–20], which reduces power consumption but also causes attenuation of the summation result. This makes the design requirements for multi-bit quantizers more stringent, which is not desirable.

This paper proposes a low-power multi-bit DSM based on passive and attenuationless summation. This circuit aims to achieve coefficient multiplication of the summation through bidirectional sampling technology compared to conventional passive summation schemes, thereby compensating the attenuation caused by summation and achieving attenuationless summation in a passive manner. This saves active power and greatly relaxes the design requirements for multi-bit quantizers.

Due to the recent popularity of the noise-shaping (NS) SAR ADC structure, which improves on the SAR structure by sampling and integrating the residual voltage generated by SAR, and achieving noise-shaping characteristics similar to the DSM structure in a passive manner [21–25], the NS SAR

structure can not only be used as a quantizer for coarse quantization of DSM, but also replace the active integrator in DSM in a passive manner, with high energy-efficiency. Therefore, in order to improve energy-efficiency, the DSM proposed in this paper integrates a 1-order NS SAR based on 4-bit SAR quantizater, allowing the NS SAR to act as a third-stage integrator and quantizer in a passive manner.

The first and second stage integrators in the DSM must use active OTA as the core module. In order to further improve energy-efficiency, the floating inverter amplifier (FIA) architecture with self-extinguishing characteristics is used by DSM [17,26–30]. Since the essence of FIA is to work in the form of inverters, which have great energy-efficiency advantages, FIA optimizes the power supply method of inverters on this basis, transforming the constant power supply mode into a floating capacitor power supply mode. Due to the limited power of capacitors, FIA has a natural self-extinguishing characteristic, which greatly saves the power consumption of the circuit. This characteristic also makes FIA particularly suitable for the half-cycle DSM structure.

This paper is organized as follows: Section 2 introduces the basic principles of conventional passive summation. The proposed passive and attenuationless summation scheme is analyzed in detail in Section 3. Section 4 presents a passive summation case study based on a second-order 4-bit DSM. The simulation results are shown in Section 5 and the conclusion is drawn in Section 6.

2. Conventional passive Summation

Conventional discrete-time DSM passive summation circuits are generally based on the principle of charge redistribution. To simplify, take the example of using passive summation to add two voltages V_{ip1} and V_{ip2}.The working principle is shown in Figure 1.
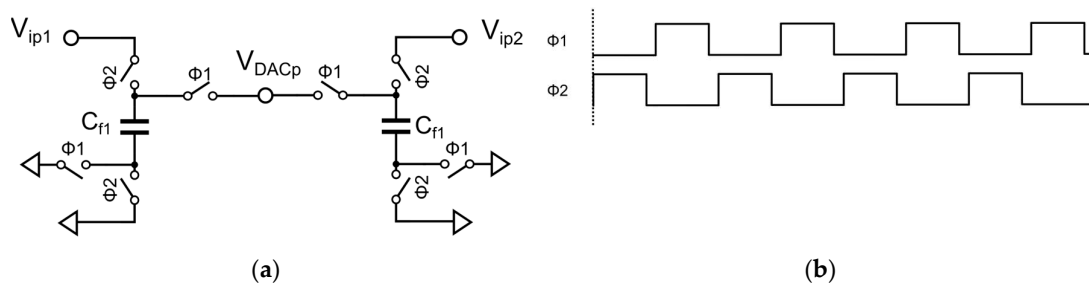

Figure 1. Conventional passive summation circuit diagram and timing: (a) circuit; (b) timing.

During $\Phi 2$, V_{ip1} and V_{ip2} respectively charge capacitors C_{f1} and C_{f2}. At this time, the voltage signals carried by capacitors C_{f1} and C_{f2} are V_{ip1} and V_{ip2}, respectively. During $\Phi 1$, these two voltage signals are transmitted to V_{DACp} for summation. Due to the parallel connection of C_{f1} and C_{f2}, the voltage at the final summation node V_{DACp} will be attenuated to:

$$V_{DACp} = \frac{C_{f1}}{C_{f1} + C_{f2}} V_{ip1} + \frac{C_{f2}}{C_{f1} + C_{f2}} V_{ip2} \tag{1}$$

Based on the above analysis, passive summation will cause the final summation voltage to attenuate to a coefficient less than 1, which is undesirable. The attenuation of the summation coefficient will increase the design requirements of the multi-bit quantizer.

3. Proposed passive and attenuationless summation scheme

In conventional passive summation, for example, if $C_{f1} = C_{f2}$, only 0.5 V_{ip1} and 0.5 V_{ip2} are transmitted to the signal summation node V_{DACp}, causing attenuation. To compensate for this attenuation, a simple and effective method is to increase the multiplication factor of the voltage signal carried by the capacitor. As we know, high-precision delta-sigma ADCs are often implemented in differential form, which allows the use of V_{in1} (V_{in2}) signals that are opposite in phase to V_{ip1} (V_{ip2}) for bidirectional sampling, thus achieving doubling for the summation coefficient.

Figure 2 shows the improved bidirectional sampling passive summation scheme proposed in this paper. The timing is the same as Figure 1(b), and the only difference from Figure 1 is that the bottom plates of C_{f1} and C_{f2} are connected to V_{in1} and V_{in2}, respectively. Through bidirectional sampling of V_{ip1} and V_{in1}, during $\Phi2$, the voltage carried by C_{f1} is $V_{ip1}-V_{in1}$. Since V_{ip1} and V_{in1} are a pair of differential voltages, there is a relationship $V_{ip1}-V_{in1}=2V_{ip1}$, which is equivalent to the voltage signal carried by C_{f1} being $2V_{ip1}$. The same applies to C_{f2}. Therefore, the voltage signals carried by C_{f1} and C_{f2} are doubled through bidirectional sampling technology. During $\Phi1$, these two voltage signals are transmitted to V_{DACp} for summation, and the voltage at the final summation node V_{DACp} is:

$$V_{DACp} = \frac{2C_{f1}}{C_{f1}+C_{f2}}V_{ip1} + \frac{2C_{f2}}{C_{f1}+C_{f2}}V_{ip2} \qquad (2)$$

If $C_{f1}=C_{f2}$, then exactly 1 times the voltage signals of V_{ip1} and V_{ip2} are transmitted at the summation node. Thus, the voltage signals carried by C_{f1} and C_{f2} were successfully multiplied by a factor of 2 through bidirectional sampling, compensating for the attenuation caused by direct parallel connection of the summation capacitors. If a larger multiplication factor is required, a more aggressive expansion scheme can be used, such as increasing the multiplication factor by serially connecting capacitors.
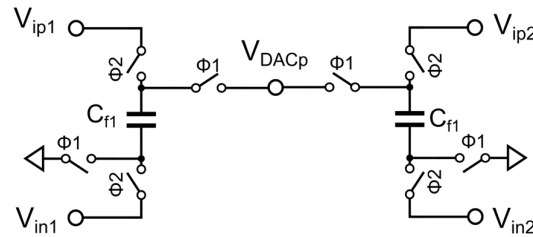

Figure 2. Bidirectional sampling passive summation circuit diagram.

Figure 3 shows the bidirectional sampling and capacitive series passive summation scheme proposed in this paper, which can achieve higher coefficient multiplication. The timing is the same as Figure 1(b). Similar to Figure 2, during $\Phi2$, the sampling is completed, and the voltage signals carried by C_{f1} and C_{f2} are equivalent to $2V_{ip1}$ and $2V_{ip2}$, respectively. During $\Phi1$, since two C_{f1} capacitors are connected in series, the carried voltages are superimposed, and the series circuit composed of two C_{f1} capacitors carries an equivalent voltage signal of $4V_{ip1}$. The same applies to C_{f2}, so that the voltage signals carried by the summation capacitor are quadrupled through bidirectional sampling and capacitive series connection. These quadrupled voltage signals are transmitted to the summation node V_{DACp} for summation, and the voltage at the final summation node V_{DACp} is:

$$V_{DACp} = \frac{4C_{f1}}{C_{f1}+C_{f2}}V_{ip1} + \frac{4C_{f2}}{C_{f1}+C_{f2}}V_{ip2} \qquad (3)$$

Similarly, if $C_{f1}=C_{f2}$, then at the signal summation node V_{DACp}, twice the voltage signals of V_{ip1} and V_{ip2} are transmitted, providing the possibility to compensate for higher attenuation and increasing the applicability and flexibility of the passive and attenuationless summation scheme.
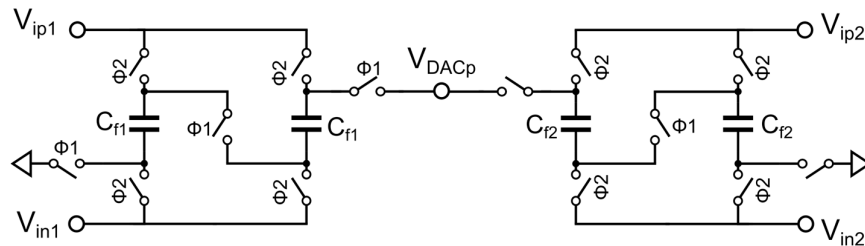

Figure 3. Bidirectional sampling and capacitor series connection passive summation circuit diagram.

It is worth noting that this method can only series connect a maximum of two capacitors, otherwise the parasitic capacitance of the switch will greatly affect the final summation result, and the maximum coefficient multiplication is limited to 4 and can only be an integer multiple. In conventional passive summation, the attenuation increases as the number of summation paths increases, making this scheme less attractive. However, fortunately, in DSMs, the number of summation paths does not exceed 4, and the sum of the summation coefficients (attenuation) is also smaller than this value. Using dynamic-range scaling technology to design summation coefficients as digital numbers such as 0.25、0.5、1 and 2 can help the summation capacitor arrays achieve better matching. In addition, we can parallel additional capacitors to ground at the summation node to control the attenuation value, making it easy to round off the attenuation to an integer.

For DSMs with a summation coefficient sum ≤ 2, it can use bidirectional summation alone to compensate for the attenuation. With a coefficient sum ≤ 4, it need to use the bidirectional sampling and capacitive series connection scheme with greater coefficient multiplication. With a coefficient sum > 4, we can first try to reduce the coefficient sum by loop coefficient scaling or reducing the summation path. If we cannot reduce the summation coefficients, although we cannot compensate for attenuation perfectly, we can try to suppress this attenuation as much as possible.

4. Design example based on passive and attenuationless summation scheme

4.1. System architecture topology

To verify the reliability of the passive and attenuationless summation scheme, we designed a 2-order DSM based on energy-efficient 4-bit 1-order passive NS-SAR quantizer. It can implement a 3-order noise-shaping loop filter. This case is significant because the third-stage is implemented in a passive manner, reducing the number of summation paths and making the proposed scheme even more attractive.

Figure 4 shows the system block diagram of a low-power multi-bit DSM based on passive and attenuationless summation. In this DSM, an NS SAR ADC is integrated to serve as the quantizer of the modulator. The NS SAR achieves shaping effects by sampling and integrating the residual voltage of the SAR, thereby replacing the active OTA and reducing the quantization noise, leading to improved energy-efficiency of the modulator. The NS SAR is designed as a 1-order loop based on 4-bit 1-order passive NS SAR quantizer. The signal and noise transfer functions can be described as follows:

$$\text{STF}_{\text{NS}} = \frac{1 + \dfrac{(1-d)Z^{-1}}{1-(1-d)Z^{-1}}}{1 + \dfrac{(1-d)Z^{-1}}{1-(1-d)Z^{-1}}} = 1 \tag{4}$$

$$\text{NTF}_{\text{NS}} = \frac{1}{1 + \dfrac{(1-d)Z^{-1}}{1-(1-d)Z^{-1}}} = 1 - (1-d)Z^{-1} \tag{5}$$
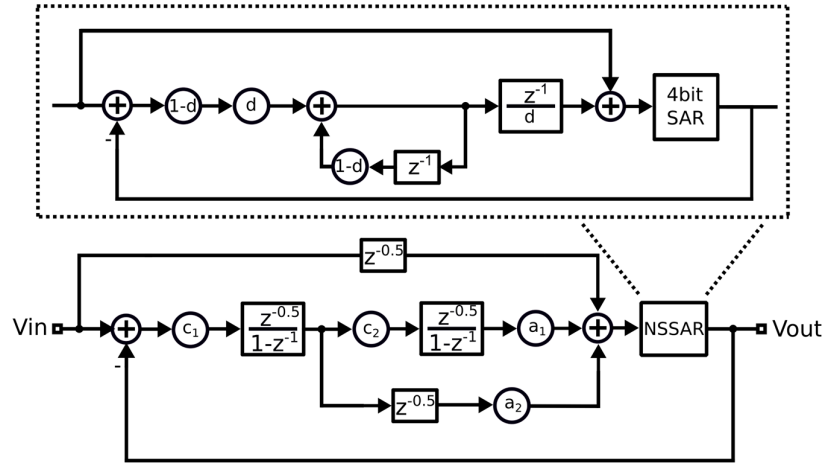
Figure 4. System block diagram.

As can be seen, the signal transfer function of the NS SAR system is strictly equal to 1, and it achieves 1-order shaping effects on the quantization noise introduced by the SAR. The system cascades the NS SAR with a 2-order CIFF modulator structure to implement the third integrator passively. The signal transfer diagram of the entire DSM after cascading can be equivalently represented as Figure 5.
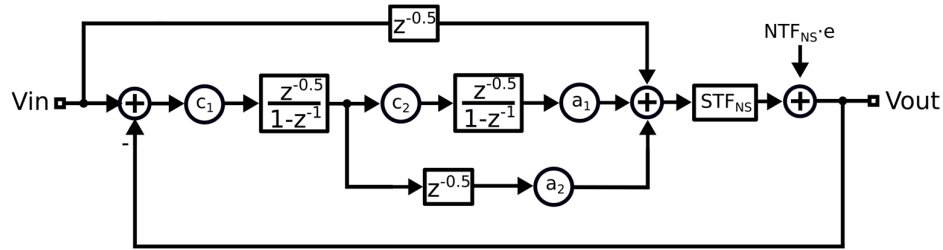

Figure 5. Equivalent system diagram.

As a result, the overall signal and noise transfer function of the system becomes:

$$
\begin{aligned}
STF &= \frac{STF_{NS}(Z^{-1} + c_1 a_2 \dfrac{Z^{-1}}{1-Z^{-1}} + c_1 c_2 a_1 \dfrac{Z^{-1}}{(1-Z^{-1})^2})}{1 + STF_{NS}(c_1 a_2 \dfrac{Z^{-1}}{1-Z^{-1}} + c_1 c_2 a_1 \dfrac{Z^{-1}}{(1-Z^{-1})^2})} \\[2mm]
&= \frac{Z^{-1} + c_1 a_2 \dfrac{Z^{-1}}{1-Z^{-1}} + c_1 c_2 a_1 \dfrac{Z^{-1}}{(1-Z^{-1})^2}}{1 + c_1 a_2 \dfrac{Z^{-1}}{1-Z^{-1}} + c_1 c_2 a_1 \dfrac{Z^{-1}}{(1-Z^{-1})^2}}
\end{aligned}
\tag{6}
$$

$$
\begin{aligned}
NTF &= \frac{NTF_{NS}}{1 + STF_{NS}(c_1 a_2 \dfrac{Z^{-1}}{1-Z^{-1}} + c_1 c_2 a_1 \dfrac{Z^{-1}}{(1-Z^{-1})^2})} \\[2mm]
&= \frac{\left[1 - (1-d)Z^{-1}\right](1-Z^{-1})^2}{1 + (c_1 a_2 + c_1 c_2 a_1 - 2)Z^{-1} + (1 - c_1 a_2)Z^{-2}}
\end{aligned}
\tag{7}
$$

Due to the low input signal frequency of the DSM, Z^{-1} is approximately equal to 1 for the input signal. Therefore, the signal transfer function of the system is 1. From equation

(7), in this system, by cascading the NS SAR with a 2-order CIFF modulator structure, we obtain a 3-order shaping modulator system. The coefficients of the system are set as follows: $d = 0.15$, $c_1 = 2$, $c_2 = 2$, $a_1 = 0.25$, $a_2 = 0.25$.

Additionally, since there are always three summing paths in this system and the sum of the summing coefficients is $1.5 < 2$, we can use bidirectional summation technique to compensate for the attenuation.

4.2. Circuit implementation

4.2.1. Cascode FIA in the integrator

As is well known, the OTA in the integrator is a core structure of the DSM and also the main source of power consumption in DSM. As shown in Figure 6, the FIA is used in the two-stage integrator of the DSM designed in this project, utilizing its natural self-extinguishing effect to further improve the energy efficiency of the DSM. During $\Phi1$, in the sampling cycle, the integrator does not work, and the power supply charges the floating power supply FIA. During $\Phi2$, in the integration cycle, the FIA works. Unlike conventional fixed power supply, the FIA uses a fully floating capacitor Cres to provide the power voltage and current required by this inverter. The voltage and current provided by Cres gradually decrease over time. When the voltage difference of Cres is less than twice the threshold voltage of the transistor, the FIA stops working. This self-extinguishing effect is naturally suitable for half-cycle DSM structures and can further improve the energy efficiency of the entire DSM. The equivalent gm provided by FIA to the system during the integration cycle is estimated as [17]:

$$g_{m\_avg} = \frac{8C_{res}}{Ts} \frac{\Delta V_D}{V_T}$$

(8)

Where T_S is the period of $\Phi1$ and $\Phi2$, ΔV_D is the voltage drop during the charging and discharging of the floating capacitor C_{res}, and V_T is the thermal voltage. It is worth noting that ΔV_D itself is also proportional to V_T, so this FIA structure has strong PVT tolerance. Furthermore, since the power consumption of FIA depends only on ΔV_D and the clock frequency, this means that using FIA as the core operational amplifier of DSM allows for the flexible adjustment of the clock frequency to control performance and power consumption.
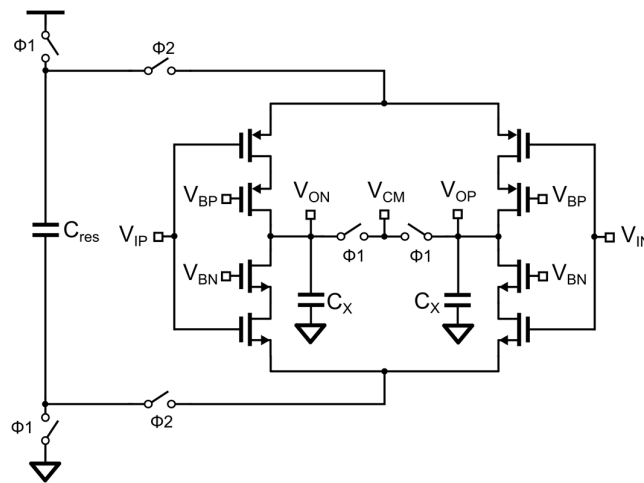

Figure 6. Cascode FIA.

Since the capacitor is fully floating, the FIA is also insensitive to common-mode inputs and automatically modulates the power supply voltage based on real-time common-mode inputs. The FIA does not require dedicated common-mode feedback and only needs
to use a small capacitor C_x to sample the voltage of V_{cm} during $\Phi1$ for simple common-mode feedback.

In order to overcome the disadvantage of low gain in simple FIA, we also applied a cascode FIA structure based on the cascade transistor, which increases the gain of the OTA to the square of the transistor's intrinsic gain. The drawback is that this will result in a decrease in output swing. However, for DSMs that can adjust the output swing using scaling techniques, this is not a disadvantage.

4.2.2. Noise-Shaping SAR ADC used as a quantizer

As shown in Figure 7, the 1-order passive NS SAR quantizer enhances the noise-shaping capability of the loop filter while improving the system's energy efficiency. The specific principle is that during $\Phi 2$, V_{ip} and V_{in} charge the capacitor C_{sum}, and the charge of C_{DAC} is cleared. Here, the capacitance value of C_{sum} is set to be equal to the total summing capacitance in the DSM and is set to be equal to C_{DAC}. During $\Phi s1$, C_{ns} is cleared. During Φ_SAR, NS SAR works, sharing the charge on C_{sum} with C_{DAC} and inputting it into the SAR quantization comparator with the integration voltage $V_{int} = V_{intp}-V_{intn}/d$ from the previous period in a ratio of 1:1/d. The Φc signal is generated asynchronously, automatically generating the next Φc when NS SAR starts working or when the previous comparison bit is compared. After C_{DAC} is also switched by SAR Logic, the value of V_P-V_n is the residual voltage V_{res} generated by the comparison. Vres represents the error generated by SAR quantization. NS SAR relies on sampling and integrating V_{res} to complete noise-shaping. It is worth noting that although the signal is attenuated by half due to the shared charge of C_{sum} and C_{DAC}, the final comparison result is not affected because C_{DAC} is half of the sum of $C_{DAC} + C_{sum}$. During Φ_{ns}, the residual charge on C_{DAC} and C_{sum} continues to be shared with C_{ns}. Since C_{ns} is set to be $dC_{DAC}/(1-d)$, the voltage on C_{ns} is $(1-d)V_{res}$. During $\Phi 2$, the charge on C_{ns} is shared with the charge on C_{int} in the previous period, and the integrated voltage V_{int} on C_{int} is $a(1-d)V_{res}+(1-d)V_{int}\cdot Z^{-1}$. Its equivalent model is shown in Figure 8.
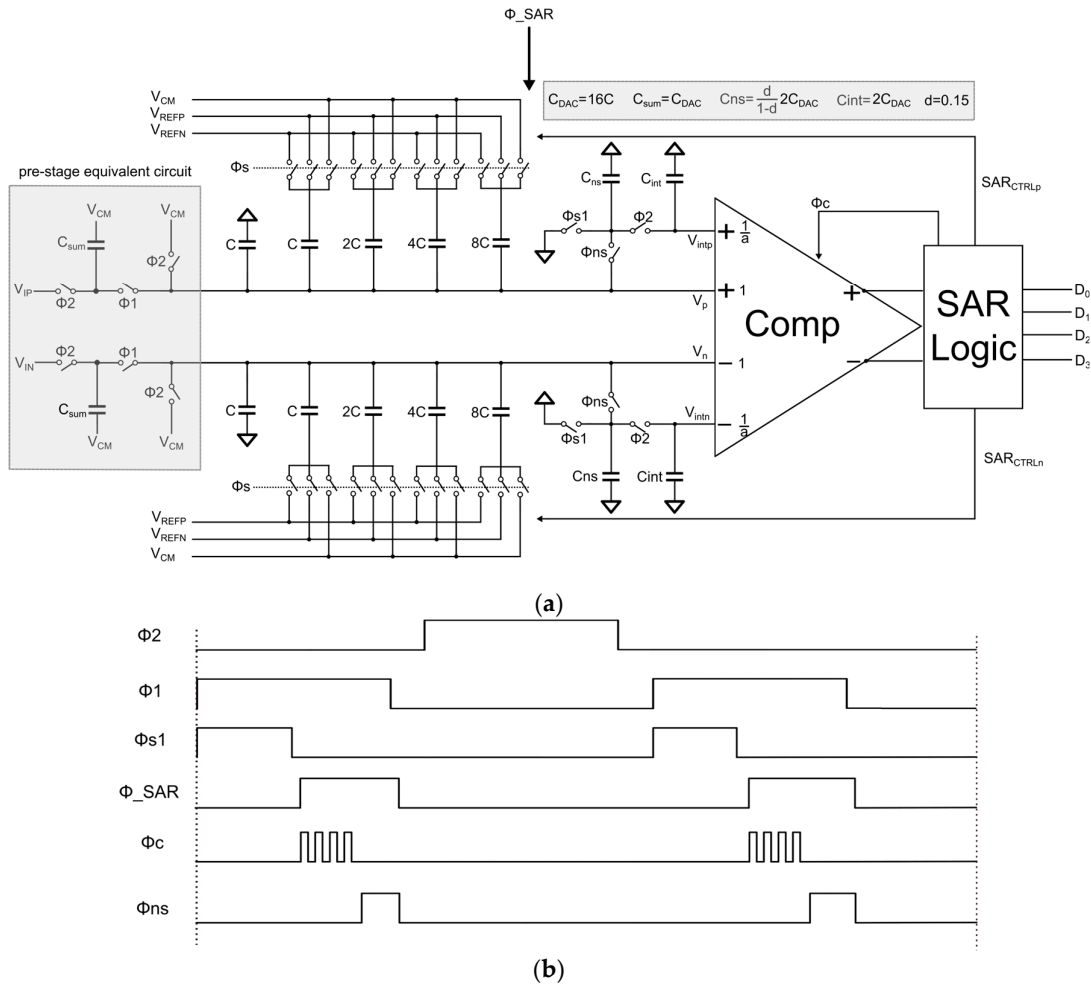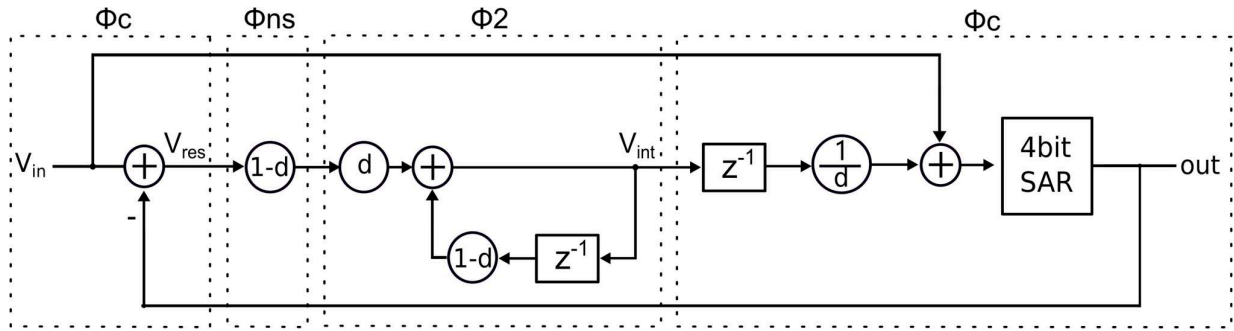

(a)

(b)

Figure 7. Circuit structure and timing of Noise-Shaping SAR ADC: (a) circuit; (b) timing.

Figure 8. Equivalent model of NSSAR.

4.2.3. Overall circuit of the DSM

Figure 9 shows the circuit and timing diagram of the low-power multi-bit DSM based on passive and attenuationless summation. The circuit consists of two integrators, passive summation circuits, a 1-order loop shaping based on 4-bit NS SAR quantizer, DWA module, and feedback DAC arrays. In order to meet the performance requirements of DSM to achieve 100dB at a power supply voltage of 1.2V and OSR=62.5, according to the thermal noise limit=4kT/(OSR·C_S), C_{S1}=14p, C_{S2}=2p are set. It should be noted that the summation circuit completes the passive and attenuationless summation through bidirectional sampling. The signals to be summed by the summation circuit are V_{ip}-V_{in}, V_{o1p}-V_{o1n}, and V_{o2p}-V_{o2n}, and the required summation coefficients are 1 : 0.25 : 0.25. During $\Phi 2d$, the input signal and OTA1 charge the positive terminals C_{f1} and C_{f2} through bidirectional sampling technology, causing the voltage carried by C_{f1} and C_{f2} to be equivalent to 2 times V_{ip} and V_{o1p}, achieving a coefficient doubling. Additionally, the voltage of C_{f3} is cleared. During $\Phi 1d$, the voltage of the positive terminals C_{f1} and C_{f2} is pushed to the summing node V_{DACp} for summation. At the same time, OTA2 charges C_{f3}. The same applies to the negative terminal V_{DACn}. The final summing node V_{DACp}-V_{DACn} is:

$$V_{DACp} - V_{DACn} = \frac{2C_{f1}(V_{ip}-V_{in}) + 2C_{f2}(V_{o1p}-V_{o1n}) + C_{f3}(V_{o2p}-V_{o2n})}{C_{f1}+C_{f2}+C_{f3}+C_p} \tag{9}$$

Where C_P is the estimated parasitic capacitance. If C_{f1} : C_{f2} : C_{f3} : C_P = 4 : 1 : 2 : 1, then the final V_{DACp}-V_{DACn} is:

$$V_{DACp} - V_{DACn} = 1(V_{ip} - V_{in}) + 0.25(V_{o1p} - V_{o1n}) + 0.25(V_{o2p} - V_{o2n}) \tag{10}$$

Therefore, by using bidirectional sampling technology to achieve coefficient doubling for the voltage signals carried by C_{f1} and C_{f2}, a passive and attenuationless summation method is achieved.
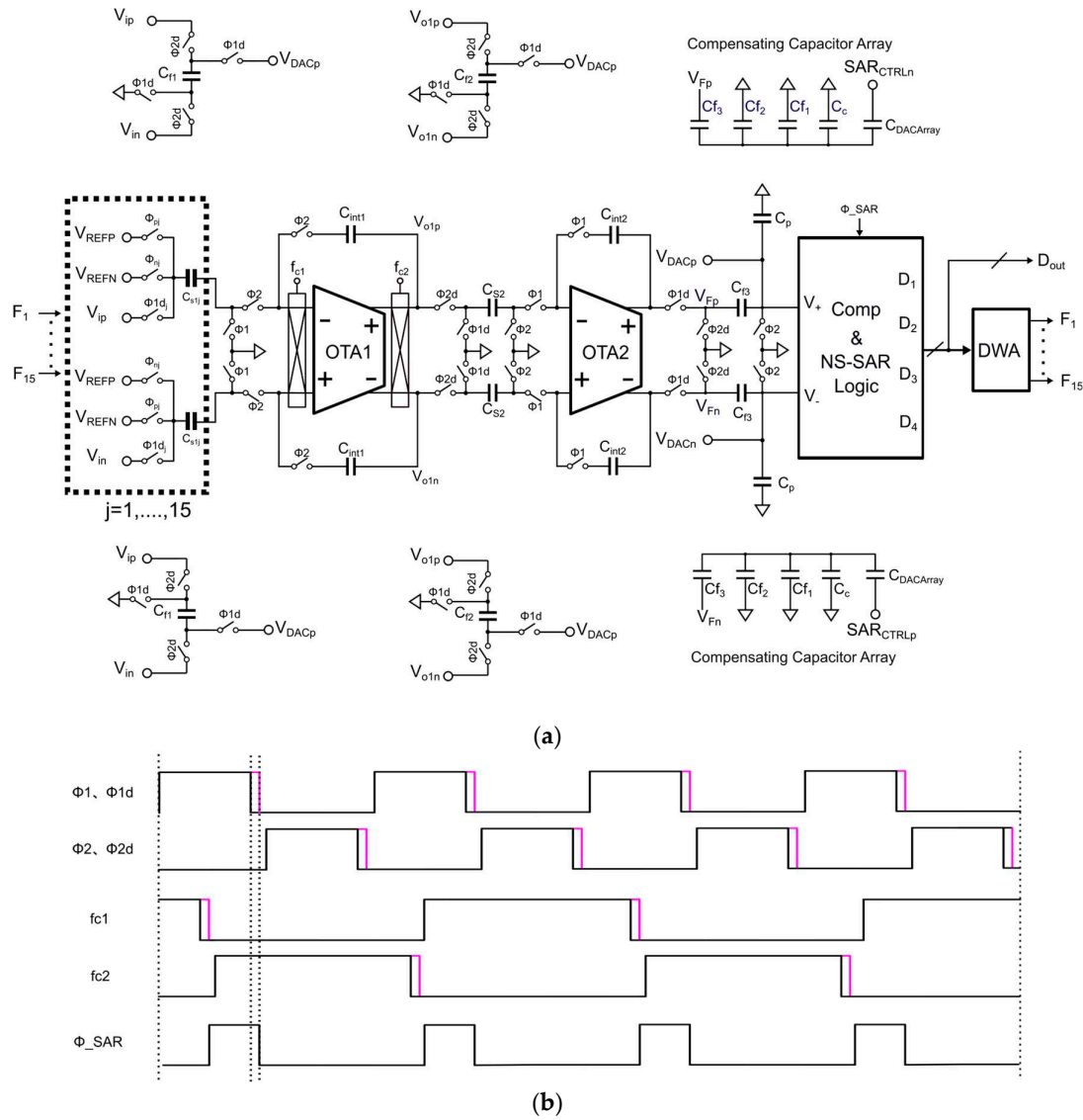
Figure 9. DSM circuit and timing:**(a)** circuit; **(b)** timing.

It should be noted that during summation, the left plate of the C_{f2} capacitor is connected to the output of the second-stage op-amp. The C_{DAC} capacitor switching inside NS SAR will increase the driving pressure on the op-amp, which is catastrophic for FIA. Therefore, we can use a differential positive and negative feedback switching of the C_{DAC} to replicate a capacitor array with the same environment for V_{Fp} and V_{Fn} nodes, but with opposite C_{DAC} switching feedback, to compensate for the two nodes, thereby eliminating the driving pressure on OTA2. This feedback mechanism only generates very small power during comparison and can be ignored relative to the entire system.

5. The simulation results

This DSM based on passive and attenuationless summation was designed using the 180nm CMOS process. The DSM runs at 2.5 MHz with a 1.2 V supply. Under an input signal of 2.9 kHz, the 4-bit code stream output by the modulator was analyzed as shown in Figure 10. In a bandwidth of 20 kHz, the simulated SNR, SNDR and SFDR are 103.08 dB, 102.62 dB and 117.73 dB. The total power consumption is 148.32 μW, with analog power consumption at 78 μW and digital power consumption at 70.32 μW.
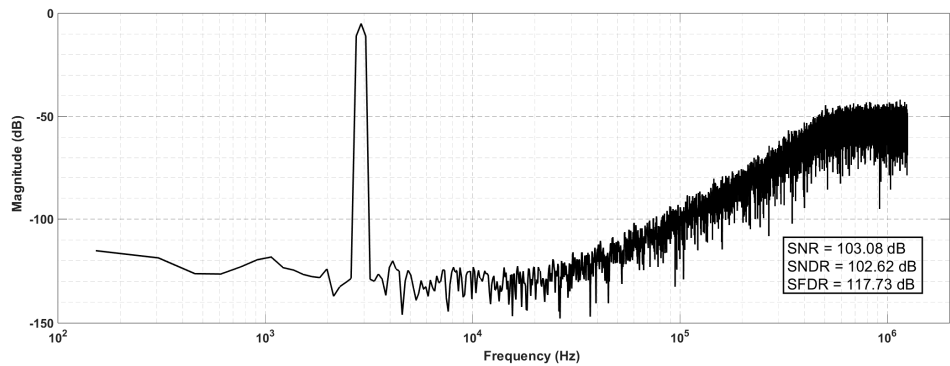
Figure 10. Simulation Output spectrum.

Table 1. Performance comparison.

Parameter	This work	JSSC [31]	JSSC [32]	TCAS-II [33]
Technology	**180nm**	65nm	65nm	65nm
Year		2020	2019	2021
Supply(V)	**1.2**	0.8	1	1
BW (kHz)	**20**	24	25	19.5
SNDR (dB)	**102.62**	89.6	94.6	88.5
Power (μW)	**148.32**	60	175	43.5
FoMs (dB)	**183.92**	175.6	176.2	175

$FoMs = SNDR + 10 * (\frac{BW}{Power})$. *simulation results for verify.

6. The simulation results

This paper proposes a low-power multi-bit DSM based on passive and attenuationless summation. By using bidirectional sampling and capacitor series connection, the voltage signals carried by the summation circuit are multiplied, successfully compensating for the attenuation caused by the parallel connection of the summation capacitors and greatly relaxing the design requirements of the subsequent multi-bit quantizer. Moreover, this scheme does not introduce additional active overhead. By combining the use of FIA and NS SAR, the validation case of a 3rd-order DSM with a 4-bit quantizer in the 180nm CMOS process demonstrates excellent performance in simulation results. The design case used provides a new approach to reduce passive summation paths, making the proposed passive and attenuationless summation scheme highly advantageous in multi-bit DSMs design.

Author Contributions: Rongshan Wei: Conceptualization, Methodology, Software.   Lijie Huang: Data curation, Writing- Original draft preparation. Gongxing Huang: Conceptualization, Methodology. Renping Wang: Visualization, Investigation.   Cong Wei: Methodology, Reviewing.

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