Low-power Multi-bit Delta-Sigma Modulator based on Passive and Attenuationless Summation Scheme

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Article

Low-Power Multi-Bit Delta-Sigma Modulator Based on Passive and Attenuationless Summation Scheme

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Abstract: In the field of delta-sigma modulators, reducing system power consumption without sacrificing accuracy has become a challenge. The summing circuit, as the main part of the delta-sigma modulator, consumes a significant amount of power in active summing, although it can achieve perfect summation. On the other hand, passive summing circuits have low power consumption but can cause attenuation in the summing results. The objective of this article is to explore how to achieve perfect summation in a passive manner. This article proposes a low-power multi-bit delta-sigma modulator based on passive and attenuationless summation scheme. The summation circuit achieves multiplication of the voltage signal carried on the summation capacitor through bidirectional sampling technique, compensating for the inherent attenuation caused by passive summation, thus eliminating the need for active OTA to achieve perfect summation. A pseudo 3-order delta-sigma modulator based on 4-bit quantizer is designed to verify the scheme. Simulation results show that at a supply voltage of 1.2V and a bandwidth of 20kHz, the SNDR reaches 102.62dB, power consumption is only 148.32μW, and Schreier FoM of SNDR is 183.92dB.

Keywords: delta-sigma modulator; low power; passive summation

1. Introduction

With the rapid development of IoT, sensors powered by batteries are needed, so in addition to high accuracy, low power consumption is also an important requirement for delta-sigma modulators (DSM) [1–7]. Therefore, how to balance between high accuracy and low power consumption has become the focus of exploration in the field of delta-sigma modulators.

With the popularity of the full feedforward delta-sigma topology [8–11], the summation circuit has become an important component of multi-bit DSM. Conventional summation circuits use active operational transconductance amplifiers (OTAs) as the core to sum up the signals at each node of the circuit, consuming a large amount of active power [12–15]. In order to reduce this part of power consumption, passive summation schemes have been widely adopted. However, passive summation circuits directly parallel capacitors carrying the voltage signals of each branch [1,16–20], which reduces power consumption but also causes attenuation of the summation result. This makes the design requirements for multi-bit quantizers more stringent, which is not desirable.

This paper proposes a low-power multi-bit DSM based on passive and attenuationless summation. This circuit aims to achieve coefficient multiplication of the summation through bidirectional sampling technology on the basis of conventional passive summation schemes, thereby compensating the attenuation caused by summation and achieving attenuationless summation in a passive manner. This saves active power and greatly relaxes the design requirements for multi-bit quantizers.

This paper is organized as follows: Section 2 introduces the basic principles of conventional passive summation. The proposed passive and attenuationless summation scheme is analyzed in detail in Section 3. Section 4 presents a passive summation case study based on a 3-order DSM. The simulation results are shown in Section 5 and the conclusion is drawn in Section 6.

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2. Conventional passive Summation

Conventional discrete-time DSM passive summation circuits are generally based on the principle of charge redistribution. To simplify, take the example of using passive summation to add two voltages V_{ip1} and V_{ip2}.The working principle is shown in Figure 1.

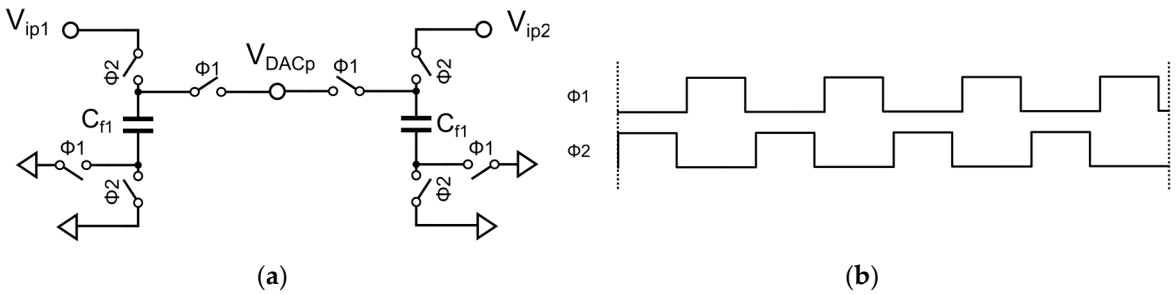

Figure 1. Conventional passive summation circuit diagram and timing: **(a)** circuit; **(b)** timing.

During Φ2, V_{ip1} and V_{ip2} respectively charge capacitors C_{f1} and C_{f2}. At this time, the voltage signals carried by capacitors C_{f1} and C_{f2} are V_{ip1} and V_{ip2}, respectively. During Φ1, these two voltage signals are transmitted to V_{DACp} for summation. Due to the parallel connection of C_{f1} and C_{f2}, the voltage at the final summation node V_{DACp} will be attenuated to:

$$V_{DACp} = \frac{C_{f1}}{C_{f1}+C_{f2}} V_{ip1} + \frac{C_{f2}}{C_{f1}+C_{f2}} V_{ip2} \quad (1)$$

Based on the above analysis, passive summation will cause the final summation voltage to attenuate to a coefficient less than 1, which is undesirable. The attenuation of the summation coefficient will increase the design requirements of the multi-bit quantizer.

3. Proposed passive and attenuationless summation scheme

In conventional passive summation, if C_{f1}=C_{f2} for example, only $0.5V_{ip1}$ and $0.5V_{ip2}$ are transmitted to the signal summation node V_{DACp}, causing attenuation. To compensate for this attenuation, a simple and effective method is to increase the multiplication factor of the voltage signal carried by the capacitor. As we know, high-precision delta-sigma ADCs are often implemented in differential form, which allows the use of V_{in1} (V_{in2}) signals that are opposite in phase to V_{ip1} (V_{ip2}) for bidirectional sampling, thus achieving doubling for the summation coefficient.

Figure 2 shows the improved bidirectional sampling passive summation scheme proposed in this paper. The timing is the same as Figure 1(b), and the only difference from Figure 1 is that the bottom plates of C_{f1} and C_{f2} are connected to V_{in1} and V_{in2}, respectively. Through bidirectional sampling of V_{ip1} and V_{in1}, during Φ2, the voltage carried by C_{f1} is V_{ip1}-V_{in1}. Since V_{ip1} and V_{in1} are a pair of differential voltages, there is a relationship V_{ip1}-V_{in1}=$2V_{ip1}$, which is equivalent to the voltage signal carried by C_{f1} being $2V_{ip1}$. The same applies to C_{f2}. Therefore, the voltage signals carried by C_{f1} and C_{f2} are doubled through bidirectional sampling technology. During Φ1, these two voltage signals are transmitted to V_{DACp} for summation, and the voltage at the final summation node V_{DACp} is:

$$V_{DACp} = \frac{2C_{f1}}{C_{f1}+C_{f2}} V_{ip1} + \frac{2C_{f2}}{C_{f1}+C_{f2}} V_{ip2} \quad (2)$$

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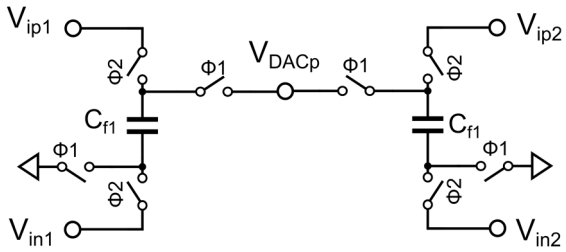

Figure 2. Bidirectional sampling passive summation circuit diagram.

If C_{f1}=C_{f2}, then exactly 1 times the voltage signals of V_{ip1} and V_{ip2} are transmitted at the summation node. Thus, the voltage signals carried by C_{f1} and C_{f2} were successfully multiplied by a factor of 2 through bidirectional sampling, compensating for the attenuation caused by direct parallel connection of the summation capacitors. If a larger multiplication factor is required, a more aggressive expansion scheme can be used, such as increasing the multiplication factor by serially connecting capacitors.

Figure 3 shows the bidirectional sampling and capacitive series passive summation scheme proposed in this paper, which can achieve higher coefficient multiplication. The timing is the same as Figure 1(b). Similar to Figure 2, during Φ2, the sampling is completed, and the voltage signals carried by C_{f1} and C_{f2} are equivalent to $2V_{ip1}$ and $2V_{ip2}$, respectively. During Φ1, since two C_{f1} capacitors are connected in series, the carried voltages are superimposed, and the series circuit composed of two C_{f1} capacitors carries an equivalent voltage signal of $4V_{ip1}$. The same applies to C_{f2}, so that the voltage signals carried by the summation capacitor are quadrupled through bidirectional sampling and capacitive series connection. These quadrupled voltage signals are transmitted to the summation node V_{DACp} for summation, and the voltage at the final summation node V_{DACp} is:

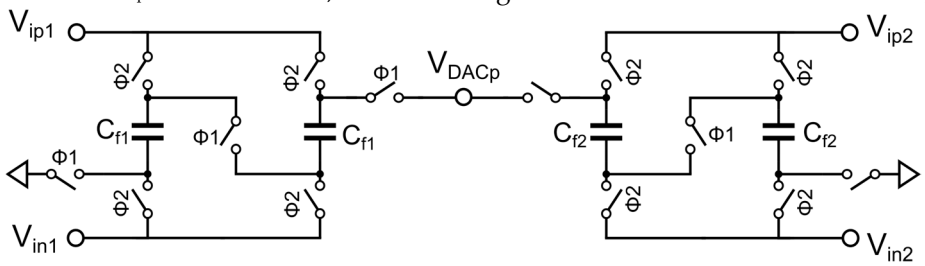

Figure 3. Bidirectional sampling and capacitor series connection passive summation circuit diagram.

$$V_{DACp} = \frac{4C_{f1}}{C_{f1}+C_{f2}} V_{ip1} + \frac{4C_{f2}}{C_{f1}+C_{f2}} V_{ip2} \tag{3}$$

Similarly, if C_{f1}=C_{f2}, then at the signal summation node V_{DACp}, twice the voltage signals of V_{ip1} and V_{ip2} are transmitted, providing the possibility to compensate for higher attenuation and increasing the applicability and flexibility of the passive and attenuationless summation scheme.

It is worth noting that this method can only series connect up to two capacitors, otherwise the parasitic capacitance of the switch will greatly affect the final summation result, and the maximum coefficient multiplication is limited to 4 and can only be an integer multiple. In conventional passive summation, the attenuation increases as the number of summation paths increases, making this scheme less attractive. However, fortunately, in DSMs, the number of summation paths does not exceed 4, and the sum of the summation coefficients (attenuation) is also smaller than this value. Using dynamic-range scaling technology to design summation coefficients as digital numbers such as 0.25、0.5、1 and 2 can help the summation capacitor arrays achieve better matching. In addition, we can parallel additional capacitors to ground at the summation node to control the attenuation value, making it easy to round off the attenuation to an integer.

For DSMs with a summation coefficient sum ≤ 2, it can use bidirectional summation alone to compensate for the attenuation. With a coefficient sum ≤ 4, it need to use the bidirectional sampling and capacitive series connection scheme with greater coefficient multiplication. With a coefficient

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sum > 4, we can first try to reduce the coefficient sum by loop coefficient scaling or reducing the summation path. If we cannot reduce the summation coefficients, although we cannot compensate for attenuation perfectly, we can try to suppress this attenuation as much as possible.

4. Design example based on passive and attenuationless summation scheme

To verify the reliability of the passive and attenuationless summation scheme, we designed a 3-order DSM based on 4-bit quantizer. This case is significant because the third order is implemented in a passive manner, reducing the number of summation paths and making the proposed scheme even more attractive.

Figure 4 shows the system block diagram of a low-power multi-bit DSM based on passive and attenuationless summation. The system cascades a 1-order loop based on 4-bit NSSAR quantizer [21–25] with a 2-order CIFF modulator structure to achieve the 3-order loop in a passive manner, further reducing the total power consumption of the system. The noise transfer function of the entire system is designed as follows:

$$NTF = \frac{(1-Z^{-1})^2(1-0.85Z^{-1})}{1-0.5Z^{-1}+0.5Z^{-2}} \quad (4)$$

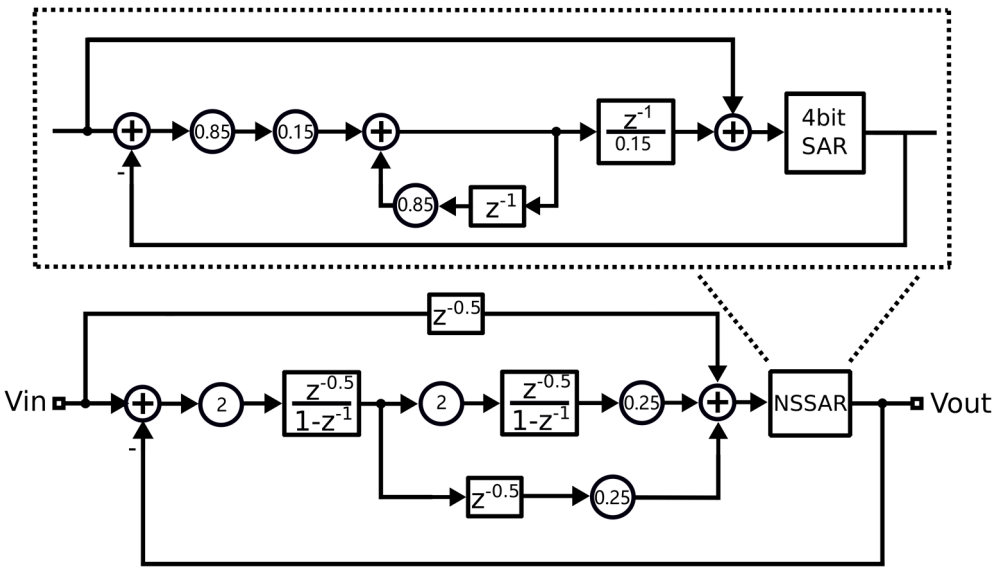

Figure 4. System block diagram.

In this system, there are three summation paths and the sum of the summation coefficients is 1.5 < 2, so we can use bidirectional summation alone to compensate for the attenuation.

Figure 5 shows the circuit and timing diagram of the low-power multi-bit DSM based on passive and attenuationless summation. The circuit consists of two integrators, passive summation circuits, 4-bit NSSAR quantizer, DWA module, and feedback DAC arrays. The OTA in the integrator is chosen as the FIA structure [17,26–30], further improving the energy efficiency advantage of this DSM. It should be noted that the summation circuit completes the passive and attenuationless summation through bidirectional sampling. The signals to be summed by the summation circuit are V_{ip}-V_{in}, V_{o1p}-V_{o1n}, and V_{o2p}-V_{o2n}, and the required summation coefficients are 1:0.25:0.25. During Φ2d, the input signal and OTA1 charge the positive terminals C_{f1} and C_{f2} through bidirectional sampling technology, causing the voltage carried by C_{f1} and C_{f2} to be equivalent to 2 times V_{ip} and V_{o1p}, achieving a coefficient doubling. Additionally, the voltage of C_{f3} is cleared. During Φ1d, the voltage of the positive terminals C_{f1} and C_{f2} is pushed to the summing node V_{DACp} for summation. At the same time, OTA2 charges C_{f3}. The same applies to the negative terminal V_{DACn}. The final summing node V_{DACp}-V_{DACn} is:

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$$V_{DACp}-V_{DACn}=\frac{2C_{f1}(V_{ip}-V_{in})+2C_{f2}(V_{o1p}-V_{o1n})+C_{f3}(V_{o2p}-V_{o2n})}{C_{f1}+C_{f2}+C_{f3}+C_p} \quad (5)$$

Where C_p is the estimated parasitic capacitance. If C_{f1}:C_{f2}:C_{f3}:C_p=4:1:2:1, then the final V_{DACp}-V_{DACn} is:

$$V_{DACp}-V_{DACn}=1(V_{ip}-V_{in})+0.25(V_{o1p}-V_{o1n})+0.25(V_{o2p}-V_{o2n}) \quad (6)$$

Therefore, by using bidirectional sampling technology to achieve coefficient doubling for the voltage signals carried by C_{f1} and C_{f2}, a passive and attenuationless summation method is achieved.

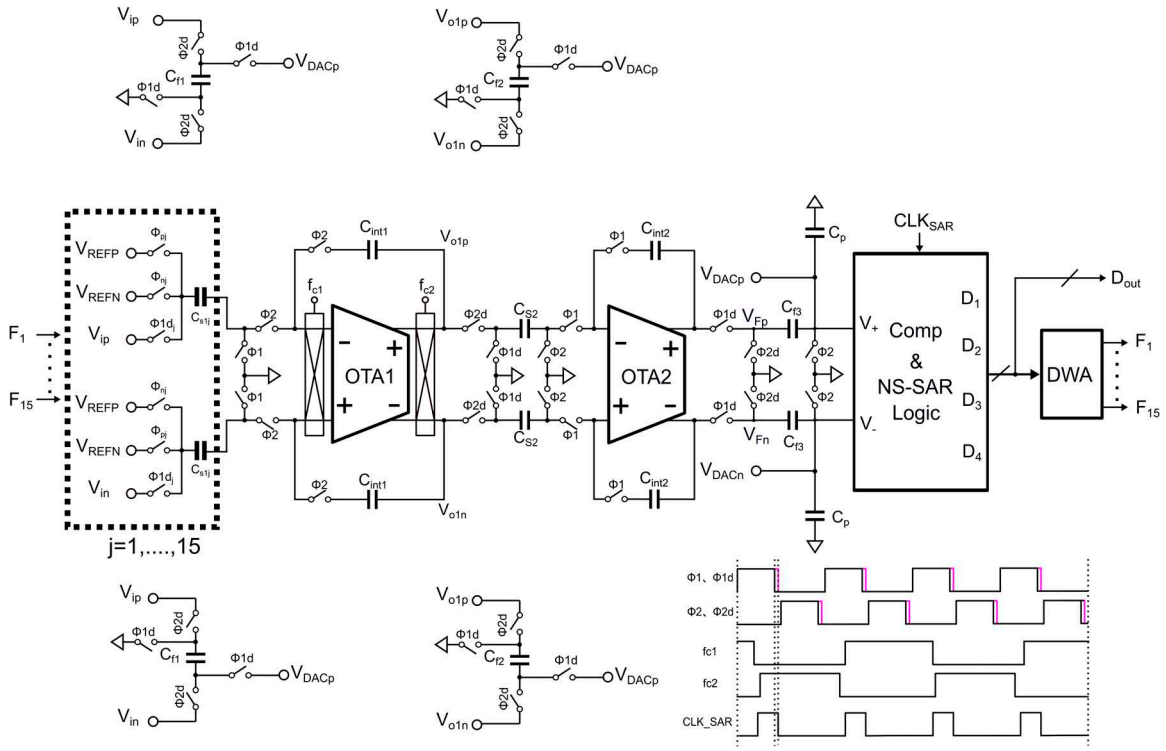

Figure 5. DSM circuit and timing.

5. The simulation results

This DSM based on passive and attenuationless summation was designed using the 180nm CMOS process. The DSM runs at 2.5 MHz with a 1.2V supply. Under an input signal of 2.9 kHz, the 4-bit code stream output by the modulator was analyzed as shown in Figure 6. In a bandwidth of 20 kHz, the simulated SNR, SNDR and SFDR are 103.08 dB, 102.62 dB and 117.73 dB. The total power consumption is 148.32 μW, with analog power consumption at 78 μW and digital power consumption at 70.32 μW.

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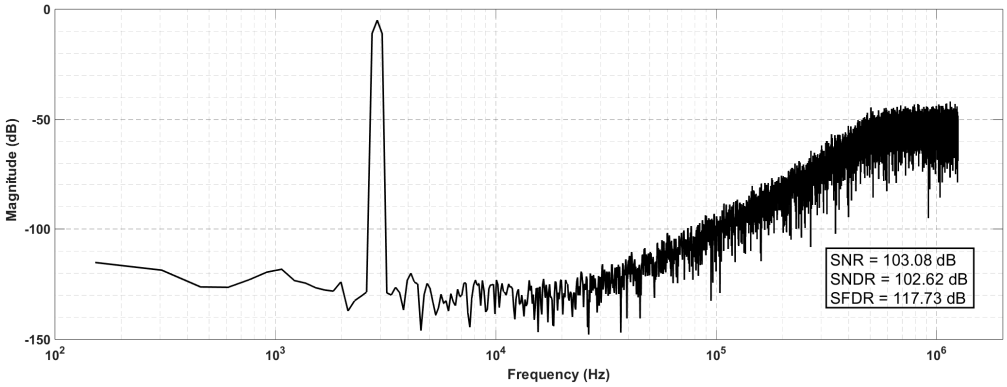

Figure 6. Output signal spectrum diagram.

Table 1. Performance parameters of the design case.

	This work
Technology	**180nm CMOS**
summation type	**passive**
Supply(V)	**1.2**
Fs(kHz)	**2500**
OSR	**62.5**
BW(kHz)	**20**
SNDR(dB)	**102.62**
Power(μW)	**148.32**
FoMs(dB)	**183.92**

$$\text{FoMs} = \text{SNDR} + 10 * (\frac{\text{BW}}{\text{Power}})$$

*simulation results for verify.

6. The simulation results

This paper proposes a low-power multi-bit DSM based on passive and attenuationless summation. By using bidirectional sampling and capacitor series connection, the voltage signals carried by the summation circuit are multiplied, successfully compensating for the attenuation caused by the parallel connection of the summation capacitors and greatly relaxing the design requirements of the subsequent multi-bit quantizer. Moreover, this scheme does not introduce additional active overhead. The validation case of a 3-order DSM based on 4-bit quantizer in the 180nm CMOS process demonstrates good performance in simulation results. The design case used provides a new approach to reduce passive summation paths, making the proposed passive and attenuationless summation scheme highly advantageous in multi-bit DSMs design.

Author Contributions: Rongshan Wei: Conceptualization, Methodology, Software. Lijie Huang: Data curation, Writing- Original draft preparation. Gongxing Huang: Conceptualization, Methodology. Renping Wang: Visualization, Investigation. Cong Wei: Methodology, Reviewing.

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Conflicts of Interest: The authors declare no conflict of interest.

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