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Article

A Comparative Study of n- and p- Channel FeFETs with Ferroelectric HZO Gate Dielectric

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Abstract: This study investigates the electrical characteristics observed in n- channel and p-channel ferroelectric field effect transistor (FeFET) devices fabricated through a similar process flow with 10 nm of ferroelectric hafnium zirconium oxide (HZO) as the gate dielectric. The n-FeFETs demonstrate a faster complete polarization switching compared to the p-channel counterparts. Detailed and systematic investigations using TCAD simulations reveal the role of fixed charges and interface traps at the HZO-interfacial layer (HZO/IL) interface in modulating the subthreshold characteristics of the devices. A characteristic crossover point observed in the transfer characteristics of n-channel devices is attributed with the temporary switching between ferroelectric-based operation to charge-based operation, caused by the pinning effect due to the presence of different traps. This experimental study helps understand the role of charge trapping effects in switching characteristics of n- and p-channel ferroelectric FETs.

Keywords: ferroelectric; FeFETs; HZO; polarization; charge trapping

1. Introduction

Ferroelectric field effect transistors (FeFETs), particularly hafnium oxide (HfO2) based FeFETs, have captured the interest of semiconductor technology as the dominant candidates for future memory applications. FeFETs have all the design components of a traditional MOSFET with a sandwiched ferroelectric material layer as the gate dielectric. The two polarization states of the dielectric determine two separate threshold voltages giving rise to a memory window (MW) between two non-volatile memory states. The discovery of ferroelectricity in hafnium oxide based dielectrics which are CMOS compatible, has attracted enormous interests in integrating FeFETs in emerging non volatile memory, in-memory computing, and neuromorphic computing applications [1-3]. This is in conjunction with rapid developments in artificial intelligence (AI) technology, which has put forward the requirements for high-speed, energy efficient, and non-volatile memories [4-6]. In this regard, the research community has observed a shift from the existing von Neumann computer architectures, driven by developments in FeFET technology [7-9]. FeFETs have demonstrated scalability, low power operation due to their CMOS compatibility, and faster non-destructible read/write operation capabilities.

The ferroelectricity observed in ferroelectric materials is primarily due to their non-centrosymmetric structure [1]. A large number of ferroelectric materials have been reported in the literature, however the most popular ones are PZT, PVDF, and HZO [1]. In such materials the polarization direction is controlled by the displacement of the atoms, their degree of variation in crystalline phase and material compositions [10-19].

Among the various dopants in hafnium oxide (HfO2) such as Al, Sr, La, Gd, Si, and Zr that enable ferroelectricity, Zr doped HfO2 films have been observed to demonstrate stable ferroelectric behavior over a wide range of temperatures, compositions, and require a lower processing

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temperature [20-24]. The principle of a FeFET is the change in threshold voltage resulting from the polarization states of the gate dielectric that induce charges at the gate/channel region. Figure 1 depicts the effects of up and down polarization in n-FeFET and p-FeFET and comparing with charge trapping effects which are opposite to the polarization effects [25].

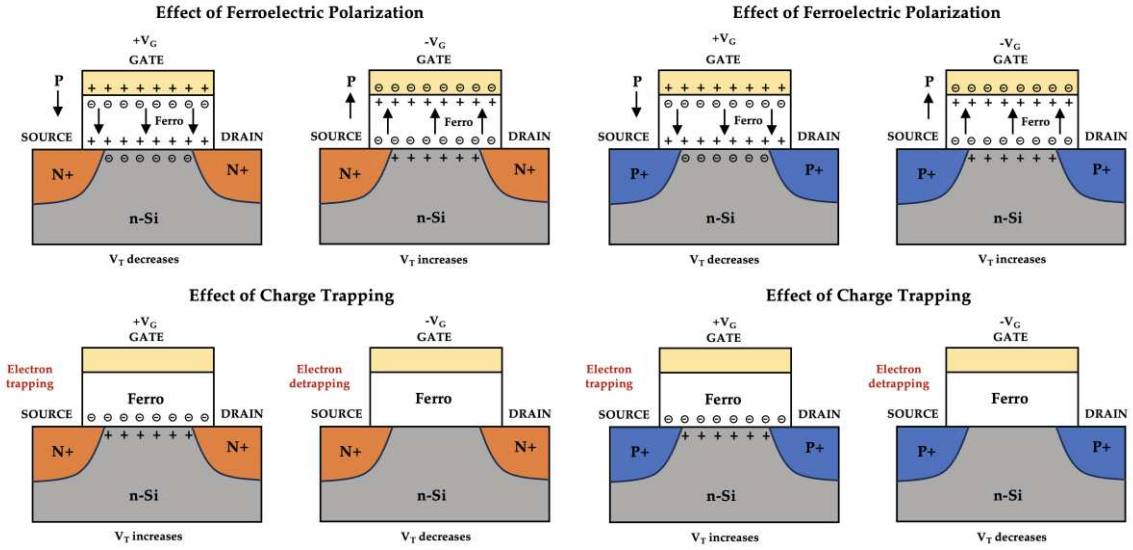

Figure 1. Effect of polarization switching and charge trapping on the threshold voltage shift in MOSFETs.

Hafnium oxide based FeFETs, however, may encounter undesirable charge trapping during the program and erase cycles required for polarization switching [1,20,26]. This is due to the defect density in HfO_2, which limits the span of the memory window post program cycles [1,20,26]. Therefore, the devices demonstrate a slower read operation which leads to a departure from the theoretical values of the memory window (MW) [1,27]. This calls for an early assessment of the different kinds of traps that form in the dielectric stack of the fabricated structure and is the focus of this study.

2. Materials and Methods

2.1. Experimental

The FeFETs were fabricated in a student run fab [28] at Rochester Institute of Technology (RIT) on 1-10 Ω-cm base resistivity silicon wafers with 10 nm ALD deposited hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$) as the gate dielectric and 15 nm of sputtered TiN as the gate electrode, followed by an anneal at 600° C to achieve the ferroelectric phase. The process flow consisted of 5 mask levels designed in-house using Mentor Graphics Pyxis, fabricated by a Heidelberg DWL 66+ direct laser writer, and using the ASML PAS5500 i-line stepper for lithography. The devices consisted of LOCOS (local oxidation of silicon) isolated FETs with ion implanted source and drain regions implanted by the Varian 350D ion implanter. For the n-channel devices, a P31 implant species were used, and for the p-channel devices a B11 implant species were used. The process flow and the device schematics are shown in Figure 2.

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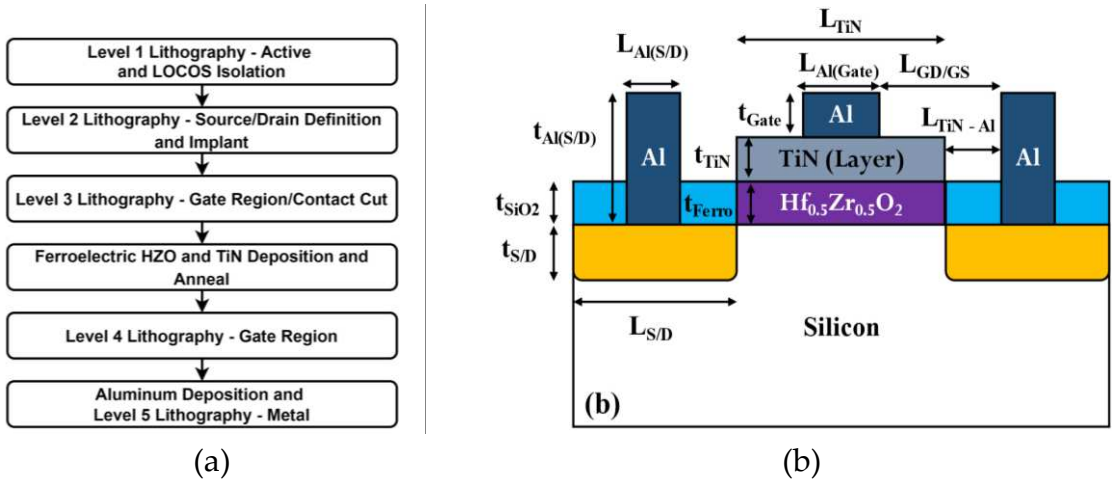

Figure 2. (a) Process flow for the fabrication of FeFETs, and **(b)** Schematic diagram of a fabricated FeFET.

A scanning electron micrograph image of a fabricated device (with designed 15 µm channel length and 15 µm channel width) and a high-resolution TEM image of the gate dielectric are shown in Figure 3. A close observation of the TEM image reveals the crystalline nature of the deposited ferroelectric HZO ($Hf_{0.5}Zr_{0.5}O_2$) thin film on the silicon substrate. Further, at the HZO/Si interface, a thin interfacial layer (IL) of SiO_x (~ 1.63 nm) is observed.

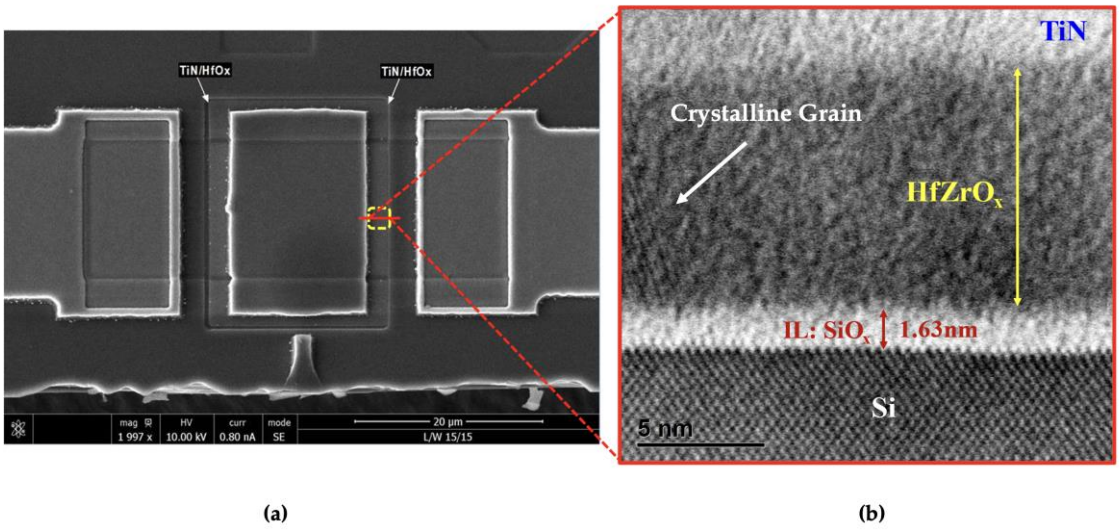

Figure 3. (a) SEM image of a FeFET (top view), and **(b)** Cross-sectional TEM image of the gate stack.

2.2. Polarization Characterization of HZO

The HZO layer employed in this work was characterized for its polarization behavior by fabricating MFM capacitors. The fabricated test structure helps in the assessment and characterization of the deposited thin film ferroelectric layers. The layer stack of the MFM capacitor consists of a bottom electrode deposited by sputtering and standard liftoff procedures to realize a 100 nm TiN layer. This is followed by the conformal atomic layer deposition (ALD) of the 10 nm $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric layer. The top electrode, TiN is then deposited by sputtering.

The polarization-electric field (P-E) hysteresis loop of the test structure were recorded with a Keithley 4200 parameter analyzer, illustrated in Figure 4. As observed, the test structure demonstrates good polarization switching behavior with a remanent polarization ($2P_R$) of 34 µC/cm^2 and a coercive field (E_C) of 1 MV/cm. Also presented is the calibration of a metal-ferroelectric-metal

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(MFM) capacitor through Silvaco's Victory TCAD simulator, which will be used as a primer for realizing the fabricated FeFETs through TCAD for further analysis [29].

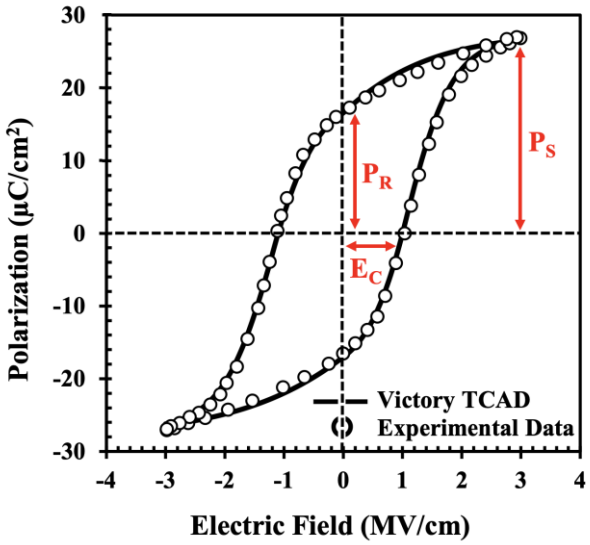

Figure 4. P-E hysteresis loop.

3.1. Experimental Results

3.1.1. DC Characterization

To investigate the DC characteristics, Keithley's 4200-SCS parametric analyzer was used. The transfer characteristics (I_D vs V_{GS}) for the n- and p-FeFETs are shown in Figure 5. The memory window (MW) specified at the drain current of 1 nA/μm, is observed to be 1 V for the n-FeFET and 1.4 V for the p-FeFET. The DC characteristics of the n- and p-FeFETs demonstrate asymmetric subthreshold characteristics. The p-channel devices exhibit steeper subthreshold characteristics compared to their n-channel counterparts. In addition, the n-FeFETs demonstrate a higher contribution of the gate-induced-drain-leakage (GIDL) current component, suggesting the role of stronger band bending at the accumulation region which is responsible for the setup of high electric fields. This consequently results in the tunneling of the valence band (VB) electrons to the conduction band (CB) while generating holes in the VB, otherwise known as band-to-band tunneling (BTBT). Another distinguishing feature of the n-FeFETs is the characteristic crossover point observed during the downward sweep in the transfer characteristics.

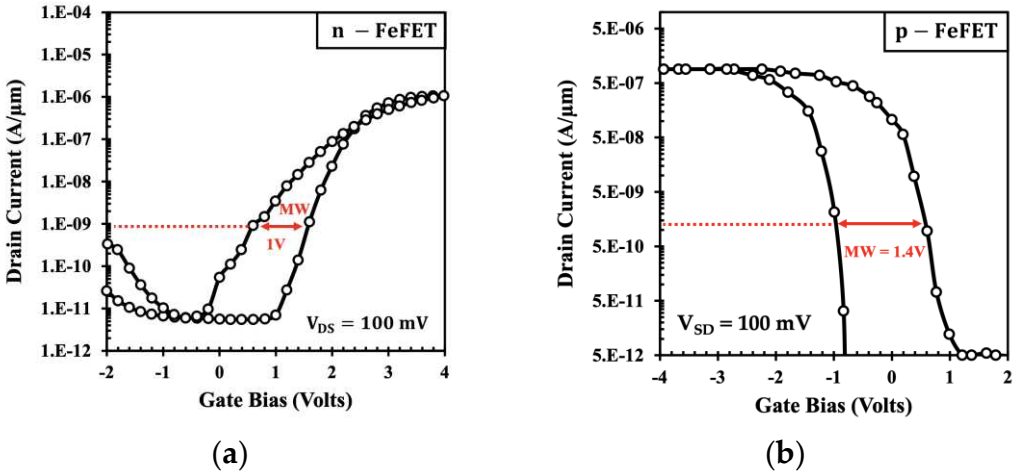

Figure 5. Transfer characteristics of **(a)** n-channel FeFETs, and **(b)** p-channel FeFETs depicting asymmetric behavior.

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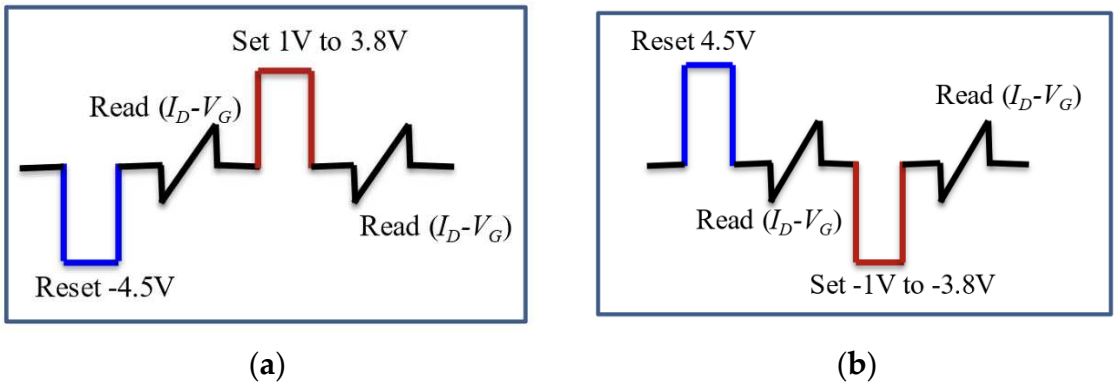
3.1.2. Pulse Characterization

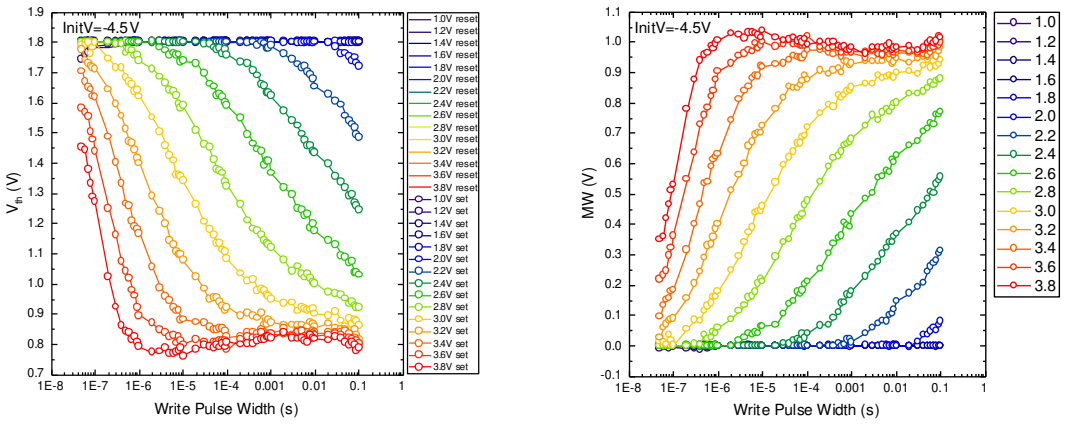
The fabricated n- and p-channel FeFET devices were characterized through a series of read and write pulse cycles using a FormFactor Cascade Microtech Summit 11000/12000 probe station & Keithley 4200-SCS parametric analyzer. The pulse setups for the n- and p-channel devices are shown in Figure 6. For the n-channel devices, the height of the reset pulse is set to -4.5 V with a pulse duration of 1 µs, while the set pulse height is varied from 1 V to 3.8 V and the pulse duration is gradually tuned from 50 ns to 0.1 s. The p-channel devices are also subjected to similar pulsing conditions with reversed polarities.



(**a**) (**b**)

Figure 6. Read and write operations performed at the gate electrode of **(a)** n-FeFET, and **(b)** p-FeFET.

The shift in the threshold voltage (V_{TH}) and the resulting MW for the n- and p-channel devices as a function of pulse width is shown in Figure 7. The switching of the polarization dipoles of a particular ferroelectric layer is a function of both the applied bias and the time duration during which the pulse is applied to the ferroelectric gate stack. As observed from Figure 7(a) and Figure 7(c), the V_{TH} of both devices can be tuned gradually by varying both the pulse height and the pulse duration. As the pulse height decreases, a longer pulse is required for observing the necessary switching of the polarization dipoles. For the n-channel FeFETs, a maximum MW of 1 V, is achieved with a pulse height of 3.8 V and pulse duration of 1 µs, as seen in Figure 7(b). This point corresponds to the complete switching of the polarization dipoles within the ferroelectric layer. Intermediate pulse height/widths can be utilized for partial polarization in multi-level logic devices. For the p-channel devices, however, the pulse characteristics in Figure 7(c) and Figure 7(d) demonstrate a global maxima in the MW at a pulse duration of 10 µs and a pulse height of -3.8 V. Further, on increasing the pulse width, a characteristic roll-off in the MW is observed as a function of write pulse width.



(**a**) (**b**)

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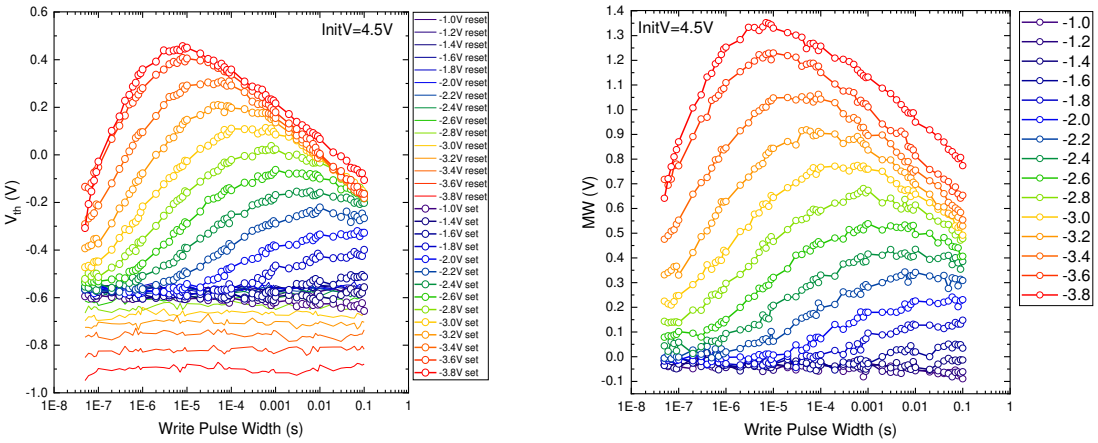

(**c**) (**d**)

Figure 7. Partial polarization switching by varying the pulse width: **(a)** Gradual tuning of V_{TH}, and **(b)** MW for n-channel, **(c)** Gradual tuning of V_{TH}, and **(d)** MW for p-channel by increasing the width of the program pulse.

The switching behavior investigated using different program/erase pulse heights and widths shows a faster complete polarization switching in n-FeFETs (3.8 V, 1 µs) than in p-FeFETs (-3.8 V, 10 µs).

3.2. Simulation Methodology

The polarization parameters extracted from the test structure's P-E hysteresis loops are fed to the simulation deck to realize ferroelectricity in the HZO. The calibrated simulation deck acts as a primer for realizing FeFET devices for the assessment of the trapping parameters. Table 1 provides the geometrical parameters of the fabricated devices used in simulations.

Table 1. Device geometrical parameters depicted in Figure 2(b).

Symbols	Description	Value
$N_{D/S}$	Source/Drain Doping	2 x 10^{19} cm^{-3}
N_{Subs}	Substrate Doping	2 x 10^{15} cm^{-3}
$t_{S/D}$	Junction depth of Source/Drain	0.8 µm
$L_{S/D}$	Lateral Extensions of Source/Drain	13 µm
t_{SiO2}	Thickness of Silicon Dioxide	100 nm
t_{Ferro}	Thickness of Ferro Layer	10 nm
t_{TiN}	Thickness of TiN Layer	12 nm
t_{Gate}	Thickness of Al Gate Contact	750 nm
$t_{Al(S/D)}$	Thickness of Al Source/Drain Contact	750 nm
$L_{Al(S/D)}$	Length of Al Source/Drain Contact	9 µm

Silvaco's Victory Device simulator is used to identify the different kinds of traps that evolved during the fabrication process [26]. A detailed simulation methodology is presented to capture the switching of the polarization dipoles during the upward and downward sweeps.

3.2.1. Calibration of the Fabricated Devices

In modeling the fabricated devices, p-channel devices are considered first due to their steeper subthreshold characteristics and a parallel memory window. The off-state current is tuned by considering donor type bulk traps in the silicon substrate. The bulk trap density is set as 1x10^{16} cm^3 and the trap level is 0.63 eV. The capture cross section for electrons and holes are set to 10^{-13} cm^2 and 10^{-14} cm^2 respectively in accordance with experimental reports [1,20,30]. Further, the literature survey suggests the role of fixed charges and charge trapping at the HZO/SiO_2 interfacial layer (IL) interface

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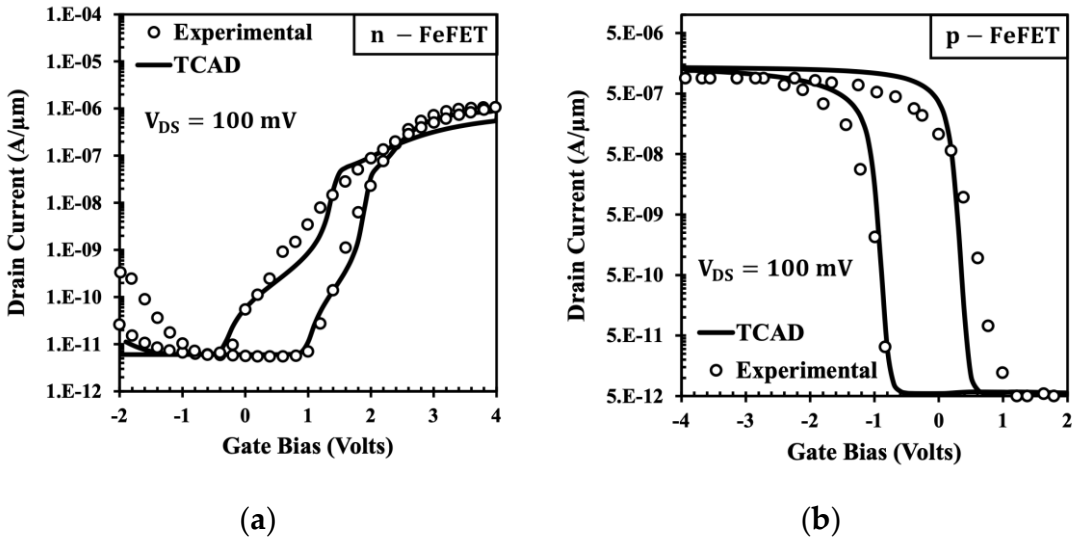
in modulating the subthreshold characteristics and thus limiting the memory window of the fabricated devices [1,20,30]. Accordingly, acceptor type interface traps were tuned at the HZO/IL interface to obtain a best fit to the experimental data. In this regard, an interface trap density of $1.8x10^{13}$ cm^2, trap energy level of 0.20 eV and capture cross sections of 10^{-13} cm^2 and 10^{-14} cm^2 for electrons and holes respectively were defined at the HZO/IL interface [31]. In addition to these, Fermi and SRH models were invoked to capture carrier statistics and the interaction of carriers with traps that evolved during the fabrication process. The Priesach Ferroelectric model was also invoked to model the doping dependent mobility, CVT model [32] and to capture the ferroelectric polarization. The calibrated simulation deck for the p-channel device was then used as the basis for realizing n-channel FeFETs. The off-state current was tuned again by considering the donor type bulk traps in the silicon substrate. The trapping conditions defined in the substrate were similar to that of p-channel devices in order to mimic similar bulk conditions, except that the OFF–state current was tuned by changing the energy of the trap level to 0.43 eV. The interface trap density at the HZO/IL interface was similar to the p-channel case, except that the trap levels were tuned to 0.26 eV to capture the slow subthreshold characteristics observed in Figure 5(a) for n-FeFETs. In addition to this, to capture the GIDL effect observed in n-FeFETs, as seen in Figure 5(a), Kane's BTBT model was invoked, and its coefficients were tuned to achieve the best fit to the GIDL current [27]. The calibrated simulation decks for the n- and p-channel devices are shown in Figure 8.

It is observed that the subthreshold characteristics of n-FeFETs are more affected due to charge trapping at the HZO/SiO_2(IL) interface suggesting that electrons are more easily trapped than holes. The presence of IL further participates in a tunneling current, due to charge trapping at the HZO/SiO_2 (IL). This results in a charge transfer directly between the HZO and Si channel and is responsible for modulating the subthreshold characteristics of the n-FeFETs.



(a) (b)

Figure 8. Calibration of simulation deck in Silvaco's Victory TCAD for **(a)** n-channel, and **(b)** p-channel FeFETs.

The characteristic crossover point observed in the n-channel devices during the downward sweep was also captured in the TCAD simulations, as shown in Figure 8(a). A closer insight into this reveals that there is a temporary switching of the ferroelectric based operation to the charged based operation, which arises due to the presence of the fixed charges and charge trapping at the HZO/IL interface and HZO bulk layer.

The devices are further investigated by recording the contour plots of electron/hole concentrations and conduction current densities after forward and reverse sweeps at 1 nA/μm. These are depicted in Figure 9(a) for n-FeFETs and in Figure 9(b) for p-FeFETs. For the n-channel device, as observed from Figure 9(a), the shift in electron concentration and conduction current density is not significant after the respective program/erase cycles. In contrast, for the p-channel device, a

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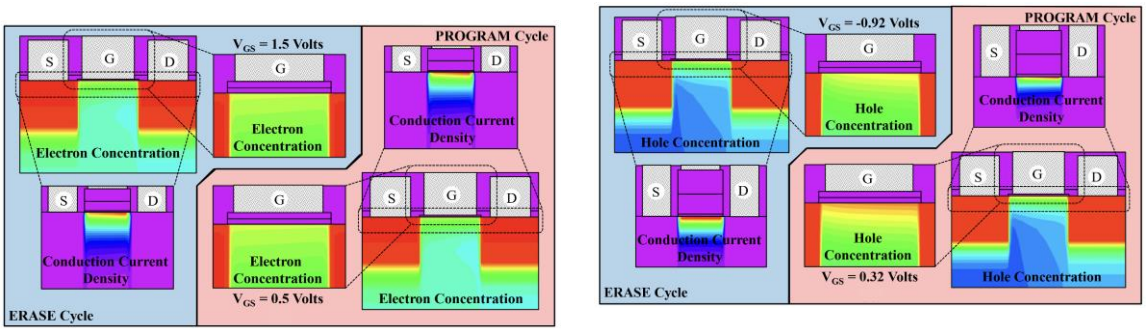
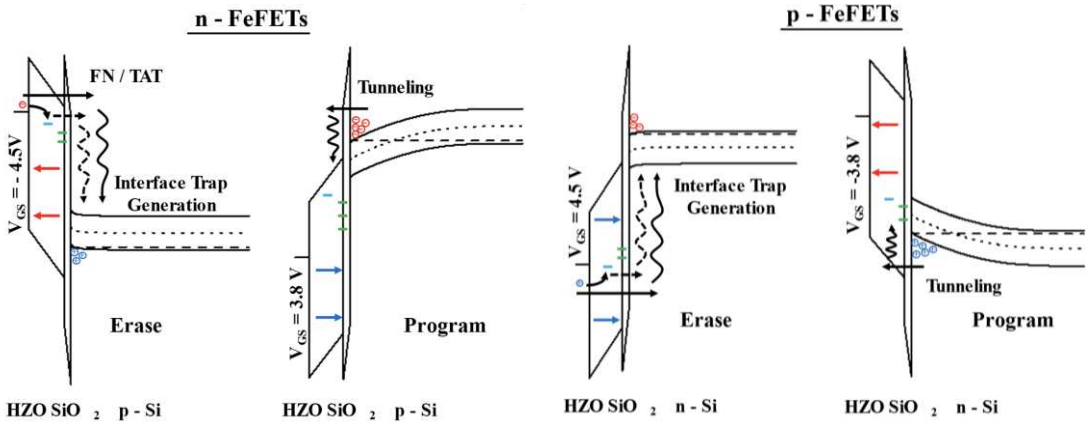
significant change in both the hole concentration as well as the conduction current density is observed in Figure 9(b), which accounts for the shift in V_{TH} observed in both Figure 7(c-d) and Figure 5(b) after subjecting the gate stack to the necessary program cycle.



(**a**) (**b**)

Figure 9. Depiction of electron/hole concentration and conduction current density contour plots for **(a)** n-FeFETs, and **(b)** p-FeFETs.

The trapping effects on the MW can be understood by observing the band diagrams recorded at erase and program conditions. This is shown in Figure 10(a) and Figure 10(b) for the n-and p-channel devices, respectively. For the n-FeFET devices, as depicted in Figure 10(a), the carriers can directly tunnel through the HZO and the IL (SiO_2) through Fowler-Nordheim (FN) tunneling [33]. The carriers can also participate in tunneling with the help of acceptor type traps defined at the HZO/IL interface and at the HZO bulk through the trap-assisted tunneling (TAT) [33]. The injected carriers are 'hot', in the sense that these carriers are energetic and can further participate in the generation of interface traps at the SiO_2 (IL)/Si interface, thereby degrading the quality of the memory window or the devices over time. Consequently, there is a charge sharing directly between the HZO and the silicon channel, which is responsible for modulating the subthreshold characteristics observed in Figure 5(a) and Figure 8(a). Under the program cycle, as depicted in Figure 10(b), the electron carriers tunnel through the SiO_2 layer, which is translated to the shift observed in the device threshold voltage. Further, on observing the position of the traps with respect to the fermi level under both erase and program conditions, as seen in Figure 10(a), it can be inferred that most of the tunneled carriers during the program pulse are trapped courtesy of the bulk traps in HZO and at HZO/IL interface. Consequently, the span of the memory window for the n-FeFETs gets limited.



(**a**) (**b**)

Figure 10. Band diagrams under erase and program conditions for **(a)** n-FeFETs, and **(b)** p-FeFETs. Red arrows (→) in the SiO_2 dictate the orientation of the polarization field, while the green and blue symbols (-/-) represent the traps in bulk HZO and HZO/IL interface.

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The band diagrams under erase/program conditions depicted in Figure 10(b) for p-channel devices follow a similar approach. The tunneling probabilities for the holes, however, is much lower than that of the electrons and the charge sharing through FN/TAT is effectively minimized. At a sufficiently higher gate bias, there is still a possibility of 'hot' hole injection, which may result in the generation of traps at the SiO_2/Si interface. Under the program cycle, similar to the n-channel case, the tunneling of the hole carriers through the SiO_2 is responsible for the shift in the device threshold voltage observed in Figure 5(b) and Figure 8(b). Further, it is also identified that there are multi-level traps present at the HZO/IL interface. These traps are relatively deeper, as discussed in Section 3.1.1, and are responsible for the roll-off in the device V_{TH} observed during the pulse characterization of the p-FeFET devices in Figure 7(c).

4. Discussion

In this work, n-FeFETs and p- FeFET devices have been designed, fabricated and investigated using a similar process flow, which is important for their integration in CMOS circuitry. A systematic and calibrated TCAD study is presented to investigate trapping effects on the asymmetric behavior observed in the transfer and pulse characteristics of n- and p-channel FeFET devices. For model validation, fabricated MFM capacitors are realized, and the P-E hysteresis loops are calibrated against the experimental set. The calibrated deck is then used to model the FeFETs to identify the trapping parameters. The n-FeFETs demonstrate faster complete polarization switching compared to their p-channel counterparts. It has been observed that the fixed charges and interface traps at HZO/IL modulate the subthreshold characteristics of the fabricated FeFETs and are responsible for the asymmetricity observed in the transfer characteristics of the two devices. Further, the IL facilitates the tunneling current due to the presence of traps in the bulk HZO and at HZO/IL. This is responsible for the charge sharing directly between the HZO and the silicon channel and limits the span of the memory window for the fabricated devices. The n-channel devices, as observed, are identified to be more affected compared to p-channel devices, suggesting that electrons are more easily trapped than holes. Further, the characteristic crossover point observed in n-FeFETs was found to be associated with the partial recovery of the polarization dipoles due to the charge trapping mechanism, which results in a temporary switch between ferroelectric based operation to charge based operation.

Author Contributions: Conceptualization, S.K.; methodology, S.K., P.J. and P.C.P; software, M.S., K.S., M.G.; validation, D.M., K.N. and S.D.; formal analysis, P.J., K.S., K.N. and S.D.; investigation, P.J., K.N. and S.K.; resources, S.K. and K.N.; data curation, P.J., S.K; writing—original draft preparation, K.S., P.J. and S.K; writing—review and editing, P.J., S.K; visualization, K.N., D.M. and S.D; supervision, S.K.; project administration, S.K.; funding acquisition, S.K. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: All data are available upon request from the corresponding author.

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Conflicts of Interest: The authors declare no conflict of interest.

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