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Posted Date: 28 September 2023

doi: 10.20944/preprints202309.1956.v1

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Generalization of Bidirectional Dual Active Bridge DC/DC Converter Modulations Schemes: State of Art Analysis under Triple Phase Shift Control

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Abstract: The main objective of the paper is to provide a thorough analysis of currently used modulation control schemes for single phase bidirectional dual active bridge DC/DC converter. In this article, it will be shown that single phase shift, extended phase shift and Dual phase shift modulation schemes are special cases of triple phase shift (TPS) modulation scheme. The article aims to highlight six TPS switching modes and their complements with the operational constraints. Unlike previous studies that regarded TPS as a complex scheme, this paper simplifies the analysis of each mode and aims to standardize the understanding of TPS modulation in DAB converters. Power equations, range of power transferred and zero voltage switching (ZVS) are derived for all the modes under TPS without assuming fundamental component analysis. Additionally, a generic optimization algorithm is developed to show the advantages of TPS modulation and thus, detailed analysis presented in this paper provides valuable insights for single phase DAB converter designers in identifying a wide range of optimization algorithms to achieve higher efficiency under TPS modulation. This analysis contributes to the advancement of bidirectional DAB converter technology and facilitates its application in various power electronic systems.

Keywords: dual active bridge converter (DAB); triple phase shift control (TPS); modes of operation; reactive power; zero voltage switching (ZVS)

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1. Introduction

DC/DC converter is a key component in various power electronic systems and several bidirectional DC-DC topologies have been suggested in literature for low to medium power applications, such as solid-state transformers, battery charging/discharging, electric vehicles, and interruptible power supplies (UPS) [1-5]. These DC/DC converters are generally categorised into, hard switched or soft switched, single, or multi-phase, voltage source or current source, transformer isolated or non-isolated DC-DC converters [6-8]. Single phase isolated bidirectional dual active bridge DC/DC converter (DAB) of Figure 1 (a) comprises of two active H bridges, two DC link filter capacitors, external series inductor (L_{ext}) and AC transformer. Bridge A and B, consist of four switches, S_1- S_4 and Q_1-Q_4 with integrated anti-parallel diodes. It offers the advantages of reduced passive components (only a single series inductor), galvanic isolation, extended region of soft switching, fast power reversal, high power density, buck/boost operation, possibility of high stepping ratio of conversion, simple control methods and its inherent fault isolation capability without a need for a very fast controller to limit fault current or blocking of the IGBT switches during the fault duration [9-11]. AC equivalent circuit of the DAB converter is illustrated in Figure 1 (b) by referring the converter to the transformer primary

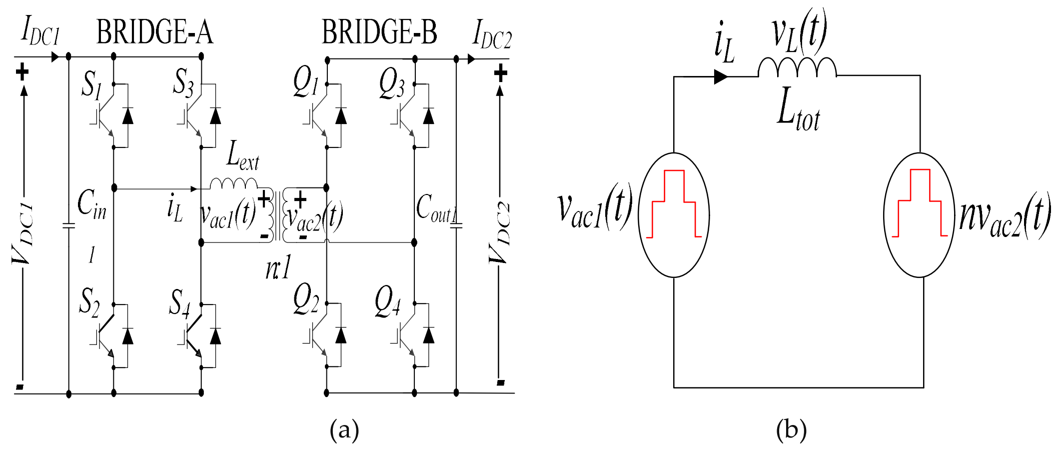

Figure 1. (a) DAB circuit diagram (b) Lossless AC equivalent circuit diagram.

side, neglecting transformer magnetizing inductance, adding transformer leakage inductance to the external inductor to form $L_{tot,}$ and with *n:1* transformer turns ratio. The magnitude of the external phase shift between switches S_1 and Q_1 of Figure 1 (a) regulates the amount of power transferred between the two converter H- bridges while direction of power flow is achieved by changing its polarity.

The primary emphasis of recent research on dual active bridge (DAB) converters has been on enhancing efficiency through the development of modulation control strategies [9-10, 12-24]. closed loop control [25-29], circuit topology [30-31] and use of low loss switching devices [32-33]. Modulation schemes for dual active bridge (DAB) converters have emerged as a significant research area, with a focus on optimizing existing methods. Several proposed modulation schemes have been explored in literature, which primarily target overall efficiency maximisation. This includes conventional s/single phase shift (CPS/SPS) modulation [10], Dual phase shift (DPS) modulation [13,14,16,17], extended phase shift (EPS) modulation [18-19], Triple phase shift (TPS) modulation [34], Pulse width modulation (PWM) [15] and variations of this direct phase shift schemes to achieve better dynamic response and eliminate the DC current in AC link [35, 36].

There have been multiple articles in literature that differentiates TPS from CPS, EPS and DPS modulations schemes [13-19,35-36]. Nevertheless, as widely reported in literature all this modulation control schemes falls under TPS modulation, thus they are all a special case of TPS modulation. The paper extends the work presented originally by author 1 in [34], by performing detailed mathematical analysis of DAB converter under TPS. The uniqueness of this manuscript is that it identifies all the possible modes of operation under TPS scheme for both forward and reverse power flow directions. It focuses on simplifying analysis of each mode, contrary to [35], that reported TPS to be complex scheme and with an intent to focus on standardizing all the phase shift modulation schemes for DAB DC/DC converter. In addition, a generic optimization algorithm is developed to show the key advantages of TPS. Analytical assessment of each mode is performed to investigate each modes active power, inductor currents, RMS current of the AC link, RMS voltage of the AC link, reactive power, power range operation of the mode, ZVS switching possibility and reactive power. The authors expect the detailed analysis of DAB converter performed in this manuscript to facilitate DAB DC/DC converter designers in identifying a wide range of optimization algorithms to achieve higher efficiency under TPS scheme.

The manuscript consists of four sections. The first section introduces CPS, EPS and DPS modulation schemes. The second section, a qualitative discussion and performance analysis of every conceivable TPS operational mode is presented. Graphical representations of voltage and current waveforms for each mode are provided, along with a derivation of key performance metrics, including peak/RMS current flow, active power, reactive power, and ZVS boundary. The derivation process begins by establishing mode constraints/boundaries, which are determined by analyzing the AC voltage waveform patterns for each mode. Next, the DAB inductor current waveform is derived, and the instantaneous currents for each sub-period are determined using the DAB converter

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equivalent circuit. From this, parameters such as average power and reactive power are calculated for each operating mode. A generic per unit TPS algorithm is used as an example to highlight the advantages of TPS modulation scheme that is discussed in section three. To validate the accuracy of the proposed TPS algorithm, a 100kW 1kV/4kV DAB model that is integral part of a high-power multi-module DAB converter is simulated using Matlab/Simulink and down scaled experimental prototype is built to validate the algorithm in section five.

2. Basic operating principle of DAB using conventional phase shift, Dual phase, and Extended phase shift control.

Using CPS control, the cross connected switches (S_1 and S_4, Q_1 and Q_4) of Figure 1(a) are switched simultaneously, resulting in DAB waveforms shown in Figure 3 (a) at the transformer primary and secondary terminals by assuming $V_{DC1} \geq nV_{DC2}$ (similar analysis results for $V_{DC1} \leq nV_{DC2}$). V_{DC1} and V_{DC2} are DC link voltages, v_L is the voltage across the inductor, i_L is the inductor current, v_{ac1} and nv_{ac2} (referred to primary) are transformer terminal voltages, T_s is the period (T_h=1/2T_s) and D is the external phase shift (0≤D≤1). The amount of power transferred, and direction is regulated by controlling the phase shift (D) between v_{ac1} and v_{ac2}.

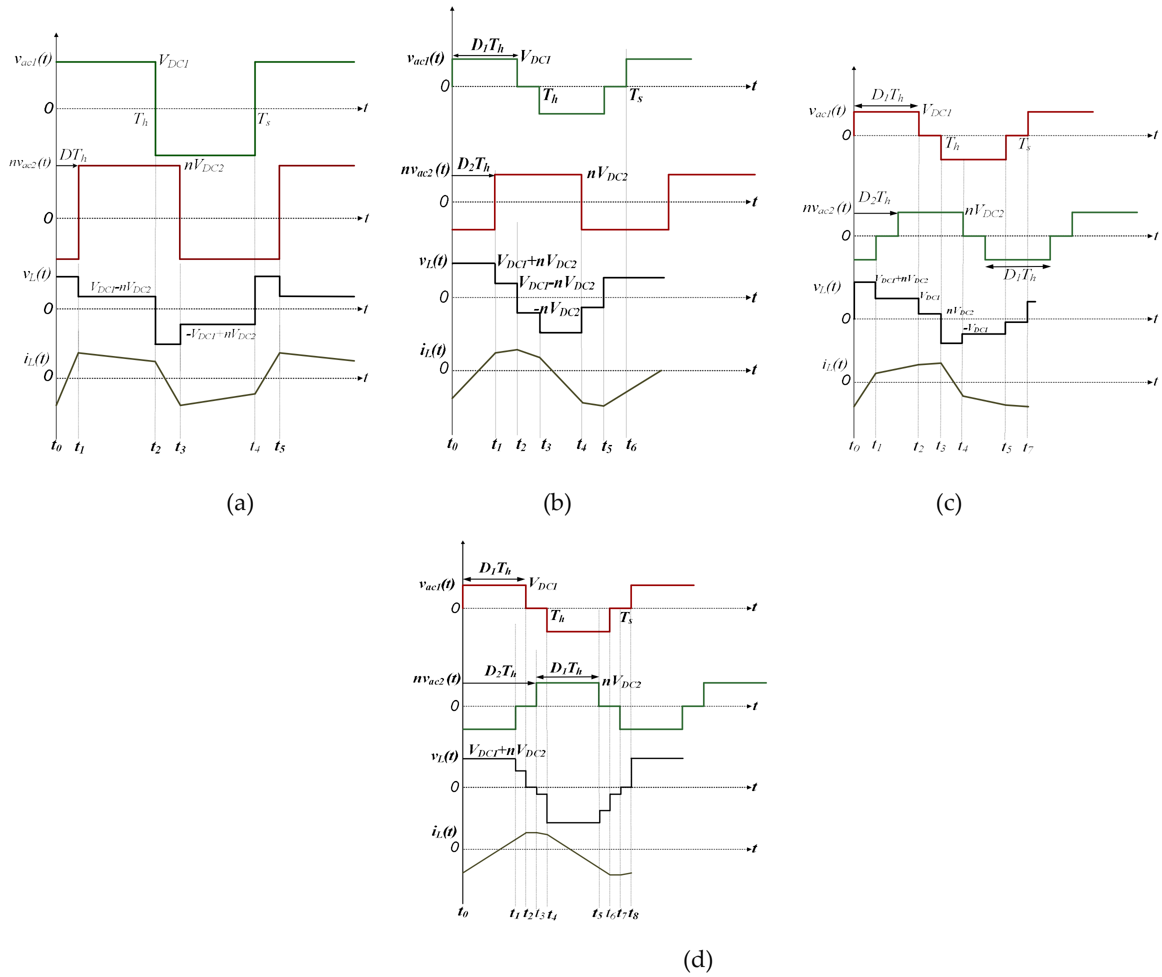

Figure 2. (a) DAB waveforms for (a) CPS (b) EPS (c) DPS for condition $0 \leq D_2 \leq D_1 \leq 1$ (d) DPS for condition $0 \leq D_1 \leq D_2 \leq 1$.

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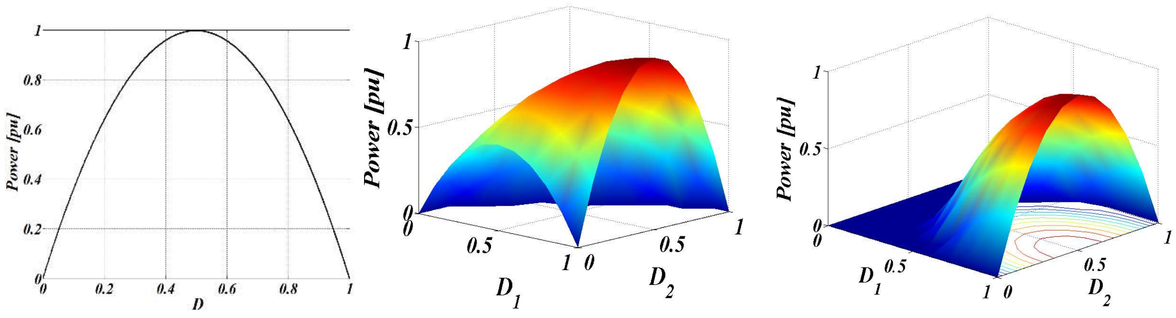

(a) (b) (c)

Figure 3. Power characteristics under (a) CPS (b) EPS (c) DPS.

From the voltages and current waveforms of Figure 2(a), the expression for the current for the first half-cycle by assuming, $t_0=0$, $t_1=DT_h$ and $t_2=T_h$ is given by:

$$i_L(t_o) = -\left[\frac{V_{DC1} - nV_{DC2} + 2nV_{DC2}D}{4f_sL_{tot}}\right]$$
$$i_L(t_1) = \left[\frac{2V_{DC1}D - V_{DC1} + nV_{DC2}}{4f_sL_{tot}}\right] \quad (1)$$
$$i_L(t_2) = \left[\frac{V_{DC1} - nV_{DC2} + 2nV_{DC2}D}{4f_sL_{tot}}\right]$$

Where, f_s is the switching frequency and L_{tot} is the total inductance.

Therefore, the equation for the output power under CPS control can be written as:

$$P_{cps} = \frac{1}{T_h}\int_0^{T_h} v_{ac1} i_L(t)\,dt$$
$$= \frac{1}{T_h}\left[\int_{t_0}^{t_1}\left\{v_{ac1}(t)\times\left(\left[\frac{V_{DC1}+nV_{DC2}}{L_{tot}}t + i_L(t_0)\,dt\right]\right)\right\} + \int_{t_1}^{t_2}\left\{v_{ac1}(t)\times\left(\frac{V_{DC1}-nV_{DC2}}{L_{tot}}t + i_L(t_1)\right)\right\}\right]dt$$

$$P_{cps} = \frac{nV_{DC1}V_{DC2}D[1-D]}{2f_sL_{tot}} \quad (2)$$

CPS control algorithm is simple to implement, since only a single parameter, the phase shift angle is required to control the power flow. The power output characteristic is illustrated in Figure 3 (a) for positive power flow. As can be observed, the maximum power can be obtained when D=0.5 and power is zero for D=0. However, CPS control is an active power centred algorithm, where applications involving large voltage conversion ratios, results in increased current stress, loss of soft switching and high circulating reactive power at the AC link [37].

EPS and DPS control were introduced to overcome some of the limitations of CPS modulation. The aim of these switching patterns is to extend soft switching region and minimise/ exclude the reactive power circulating within the converter bridges, thereby improving overall efficiency of the converter. With EPS control, additional inner parameter, D_1 which is the phase shift between the legs of one H-bridge is introduced, while in H- bridge two, the cross connected switches are switched simultaneously. This results in a quasi-square AC output waveform for the bridge where inner shift D_1 is used and a full AC square waveform for the second H- bridge as Figure 2 (b) depicts. D_1 is the parameter used to extend the ZVS and reduce the reactive power. The phase shift D_2, is the outer phase shift angle that controls the power flow magnitude and direction, which is equivalent to D in CPS modulation.

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$$
\begin{aligned}
i_L(t_o) &= \left[\frac{-V_{DC1}D_1 - 2nV_{DC2}D_2 + nV_{DC2}}{4f_sL_{tot}}\right] \\
i_L(t_1) &= \left[\frac{2V_{DC1}D_2 - V_{DC1}D_1 + nV_{DC2}}{4f_sL_{tot}}\right] \\
i_L(t_2) &= \left[\frac{V_{DC1}D_1 + 2V_{DC2}D_2 - 2V_{DC2}D_1 + nV_{DC2}}{4f_sL_{tot}}\right] \\
i_L(t_3) &= \left[\frac{V_{DC1}D_1 + 2V_{DC2}D_2 - nV_{DC2}}{4f_sL_{tot}}\right]
\end{aligned}
\tag{3}
$$

Thus, average power when EPS modulation is used, can be obtained as

$$
\begin{aligned}
P_{EPS} &= \frac{1}{T_h}\int_0^{T_h} v_{ac1} i_L(t)\,dt \\
&= \frac{1}{T_h}\left[\begin{array}{l}\int_{t_0}^{t_1}\left\{v_{ac1}(t)\times\left(\left[\frac{V_{DC1}+nV_{DC2}}{L_{tot}}t + i_L(t_0)\,dt\right]\right)\right\} + \int_{t_1}^{t_2}\left\{v_{ac1}(t)\times\left(\frac{V_{DC1}-nV_{DC2}}{L_{tot}}t + i_L(t_1)\right)\right\} \\ \int_{t_3}^{t_4}\left\{v_{ac1}(t)\times\left(\frac{nV_{DC2}}{L_{tot}}t + i_L(t_2)\right)\right\}\end{array}\right]dt
\end{aligned}
$$

$$
P_{EPS} = \frac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}\left[2D_1D_2 - 2D_2^{\,2} - D_1^2 + D_1\right] \tag{4}
$$

From (4), the additional modulation parameter D_2, improves the regulation flexibility of the converter as power diagram of Figure 3 (b) shows. Similar to CPS control, the maximum power is obtained when values of D_1=1 and D_2=0.5. This shows that only under CPS is maximum output power attainable. For other loading scenarios, different combination of control variables D_1 and D_2 may result in the same power output. In EPS, the operation of the two H-bridges is required to be swapped when the voltage conversion ratio and power direction is changed in order to operate the converter at minimal circulating power [18]. This complicates the operation of the converter further as the power flow direction has to be sensed continually, thus introducing additional overhead for the controller.

DPS control aims to address some of these limitations by not restricting one of the AC link voltages to a full square wave operation, but rather, zero states are introduced for both H-bridges, unlike EPS control, in addition to enhancing the regulation flexibility further. This is achieved by additional inner phase shift between both the converter switch pairs S_1-S_3 and Q_1-Q_3 (leg 1 and leg 2 of bridge A and Leg 1 and 2 of bridge B). Figure 2 (c) and (d), illustrates the resulting waveforms under DPS control. D_1 is the inner phase shift for both H-bridges and D_2 is the external phase shift (D_2=D in CPS control). The resulting waveforms when DPS control is applied can be divided into two operating conditions, which are:

$$
\begin{aligned}
0 \le\ & D_2 \le D_1 \le 1 \\
0 \le\ & D_1 \le D_2 \le 1
\end{aligned}
\tag{5}
$$

When,

$$
0 \le\ D_2 \le D_1 \le 1
$$

The current expression of each segment for the first half cycle is derived by assuming t_0=0, t_0=0, t_1= D_2T_h, t_2= D_1T_h and t_3= T_h:

$$
\begin{aligned}
i_L(t_o) &= \left[\frac{-V_{DC1}D_1 - 2nV_{DC2}D_2 - nV_{DC2}D_1 + 2nV_{DC2}}{4f_s L_{tot}}\right] \\
i_L(t_1) &= \left[\frac{V_{DC1}D_1 + 2V_{DC1}D_2 - 2V_{DC1} + nV_{DC2}D_1}{4f_s L_{tot}}\right] \\
i_L(t_2) &= \left[\frac{2V_{DC1}D_2 - V_{DC1}D_1 + nV_{DC2}D_1}{4f_s L_{tot}}\right] \\
i_L(t_3) &= \left[\frac{V_{DC1}D_1 + 2V_{DC1}D_2 - nV_{DC2}D_1}{4f_s L_{tot}}\right] \\
i_L(t_4) &= \left[\frac{V_{DC1}D_1 + 2nV_{DC2}D_2 + nV_{DC2}D_1 - 2nV_{DC2}}{4f_s L_{tot}}\right]
\end{aligned} \tag{6}
$$

From (6), the ideal power transferred by the converter is given for this condition as

$$
\begin{aligned}
P_{DPS1} &= \frac{1}{T_h}\int_0^{T_h} v_{ac1} i_L(t)\, dt \\
&= \frac{1}{T_h}\left[\int_{t_0}^{t_1}\left\{v_{ac1}(t)\times\left(\left[\frac{V_{DC1}}{L_{tot}}t + i_L(t_0)\, dt\right]\right)\right\} + \int_{t_1}^{t_2}\left\{v_{ac1}(t)\times\left(\frac{V_{DC1} - nV_{DC2}}{L_{tot}}t + i_L(t_1)\right)\right\}\right]dt
\end{aligned} \tag{7}
$$

$$
P_{DPS1} = \frac{nV_{DC1}V_{DC2}}{4f_s L_{tot}}\left[-2D_2^{\,2} + 2D_2 - D_1^2 + 2D_1 - 1\right] \tag{8}
$$

Similar analysis can be performed for the second operating condition in (5). By assuming, $t_1=(D_2+D_1-1)T_h$, $t_2=D_1T_h$, $t_3= D_2T_h$ and $t_4=T_h$. Therefore, current expression of each segment for the first half cycle is:

$$
\begin{aligned}
i_L(t_o) &= \left[\frac{-V_{DC1}D_1 - 2nV_{DC2}D_2 - nV_{DC2}D_1 + 2nV_{DC2}}{4f_s L_{tot}}\right] \\
i_L(t_1) &= \left[\frac{V_{DC1}D_1 + 2V_{DC1}D_2 - 2V_{DC1} + nV_{DC2}D_1}{4f_s L_{tot}}\right] \\
i_L(t_2) &= \left[\frac{V_{DC1}D_1 + nV_{DC2}D_1}{4f_s L_{tot}}\right] \\
i_L(t_3) &= i_L(t_2) \\
i_L(t_4) &= \left[\frac{V_{DC1}D_1 + nV_{DC2}D_1 + 2nV_{DC2}D_2 - 2nV_{DC2}}{4f_s L_{tot}}\right]
\end{aligned} \tag{9}
$$

The ideal power for this condition is also computed as:

$$
\begin{aligned}
P_{DPS2} &= \frac{1}{T_h}\int_0^{T_h} v_{ac1} i_L(t)\, dt \\
&= \frac{1}{T_h}\left[\int_{t_0}^{t_1}\left\{v_{ac1}(t)\times\left(\left[\frac{V_{DC1} + nV_{DC2}}{L_{tot}}t + i_L(t_0)\, dt\right]\right)\right\} + \int_{t_1}^{t_2}\left\{v_{ac1}(t)\times\left(\frac{V_{DC1}}{L_{tot}}t + i_L(t_1)\right)\right\}\right]dt
\end{aligned} \tag{10}
$$

$$
P_{DPS2} = \frac{nV_{DC1}V_{DC2}}{4f_s L_{tot}}\left[-D_2^{\,2} + 2D_2 - 2D_1D_2 + D_1 - 1\right] \tag{11}
$$

The power output for different combinations of D_1 and D_2 is illustrated in Figure 3 (c). It can be observed from the figure, as was in EPS control, maximum power output can be achieved for values of D_1=1 and D_2 =D =0.5. While for partial power operation, same output power results for different combinations of D_1 and D_2.

The triple phase shift control/modulation scheme (TPS) is an extension of the dual phase shift control (DPS), where a time delay is introduced in the gate signals of cross-connected switch pairs of each H-bridge of DAB converter. Compared to DPS, the inner phase shift might be unequal in both bridges. TPS was partially studied in [15,17,20-22] to enhance the converter's performance by extending the soft switching range, improving regulation flexibility, and increasing overall DAB DC-

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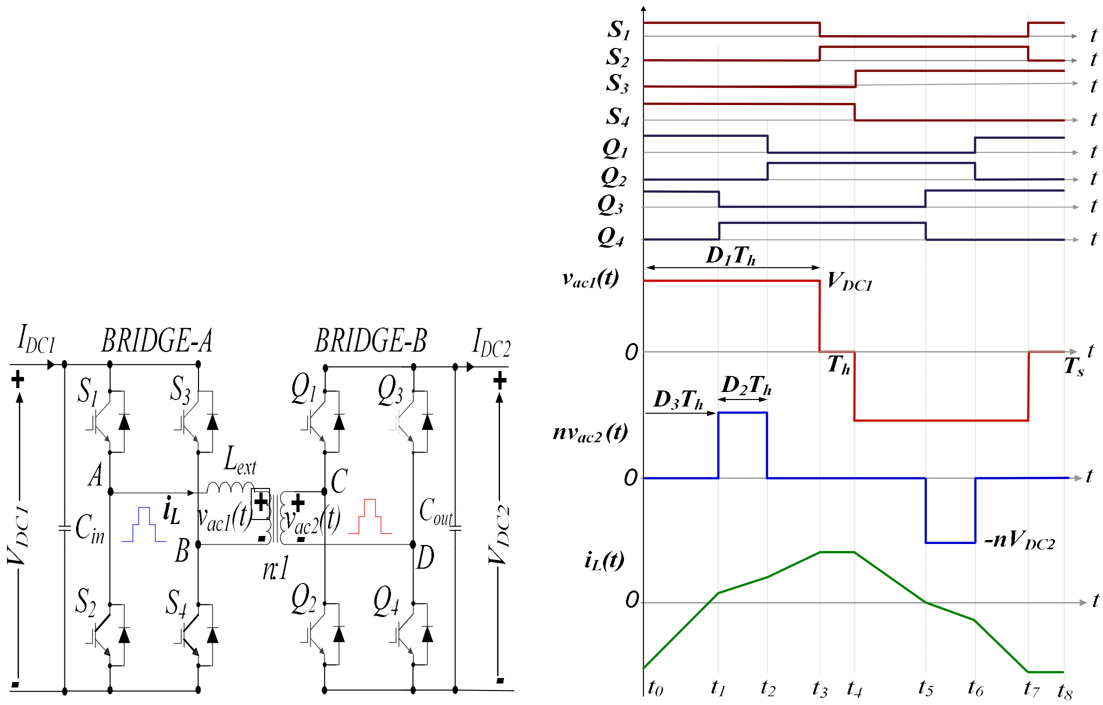
DC converter efficiency. [20] investigated the converter's stability using TPS control, but without emphasizing the important issue of efficiency improvement. [21] characterized only four TPS modes to extend the zero-voltage switching (ZVS) operating range and increase the converter efficiency. [15,17] identified twelve switching modes, and partial analysis was performed only for some of the modes using fundamental component approximation. In [22], a multiphase shift scheme including DPS and TPS was investigated to determine optimal sub modes based on waveform features.

2. Basic operating principle of DAB using TPS Control

By utilising TPS modulation scheme to control DAB converter, three control parameters symbolised as, D_1, D_2 and D_3 are used to modulate the converter. D_1 is the inner phase shift between switches S_1 & S_4, D_2 is the inner phase shift between the switches Q_1 & Q_4 while D_3 is the outer/external phase shift between S_1 & Q_1 as illustrated in Figure 3 (a). Magnitude and direction of power flow is controlled by adjusting D_3 between the two H-bridges. Figure 3 (b), depicts example waveforms showing switching waveforms for TPS modulation scheme, the resulting AC voltages at transformer terminals *AB* and *CD* (referred to the primary side) and inductor current i_L.



(a) (b)

Figure 3. (a) DAB circuit diagram (b) Switches turn on/turn off signals and ideal voltage/current waveforms under TPS scheme.

2.1. TPS Modes of operation

Based on all possible combinations of phase shifts D_1, D_2 and D_3; full, partial and no overlaps of both transformer terminal voltage waveforms, give rise to six different switching modes for forward power flow, and their complements for reverse power flow. Importantly it's the modes boundaries that set the number of TPS modes. In this section, a comprehensive analysis of the converter performance indices will be performed for each mode. TPS control involves different operating modes, in addition to loading condition (whether the converter is lightly or heavily loaded).

In the analysis, the following assumptions are made:

- Lossless DAB converter.
- Fixed V_{DC1} & V_{DC2} DC link voltages.

- Buck mode operation ($V_{DC1}>nV_{DC2}$), boost mode operation ($V_{DC1}<nV_{DC2}$) is similar to buck mode and will be omitted in this chapter.
- The turn's ratio of the transformer is n and f_s is the switching frequency.
- The transformer magnetising inductance is neglected.
- The H-bridge B is referred to the primary side, while the transformer leakage inductance is added to external inductor, resulting in a total inductance L_{tot}.
- Other short time scale factors such as switching dynamics and dead band effects are also neglected.

a) Modes 1 and 1′

Ideal operating waveforms of the modes are depicted in Figure 4. Mode 1 shown in Figure 4 (a), is characterised by a full positive-half-cycle overlap of both bridges terminal voltages with $D_1 \geq D_2$, while complimentary mode 1′ waveforms, in Figure 4 (b), are graphically described by full overlap of positive and negative half cycles of AC link voltages with bridge B waveform being shifted by 180^0, to reverse the converter operation resulting in equal but negative power. The remaining part of this section performs derivation of several key performance indicators for each of the following operating mode.

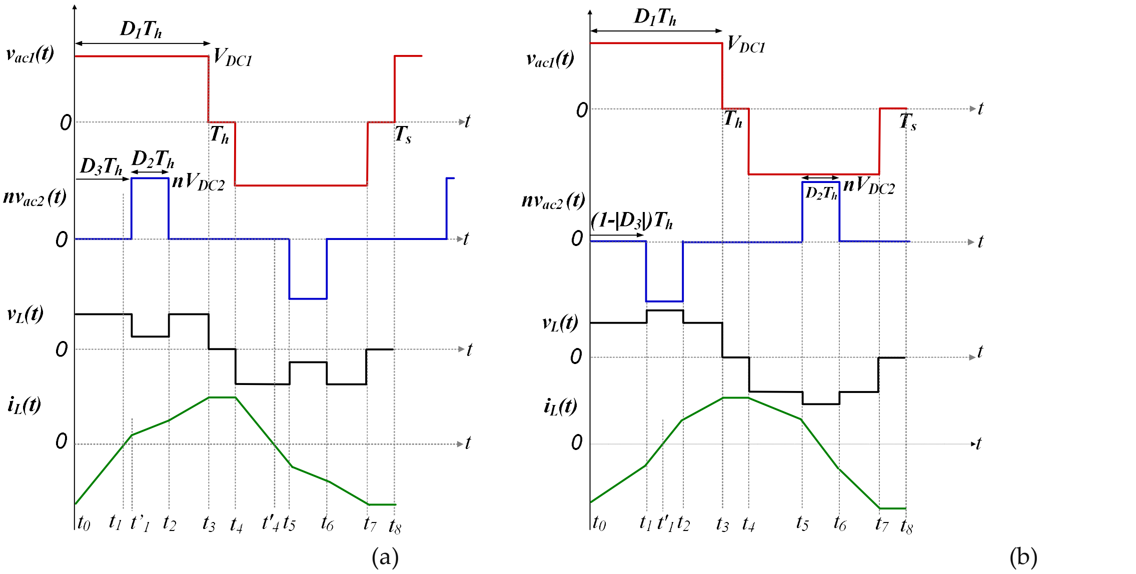


Figure 4. Steady state voltage/current waveforms for (a) Mode 1 (b) Mode 1′.

i. Mode 1

The mode boundary conditions should ensure that full overlap of both bridge AC voltages is strictly maintained. Thus, by observing Figure 4 (a), the following two constraints are defined,

$$\begin{aligned} D_1 &\geq D_2 \\ 0 \leq D_3 &\leq D_1 - D_2 \end{aligned} \tag{12}$$

Inductor current, is crucial for active and reactive power calculations. Thus, applying Kirchhoff voltage law (KVL) in the equivalent circuit diagram of Figure 1 (b), the analytical expression for the current can be written as

$$i_L(t) = \frac{1}{L_{tot}} \int_{t_n}^{t} \left(v_{ac1}(t) - v'_{ac2}(t) \right) dt + i_L(t_n) \qquad t_n \leq t \leq t_{n+1} \tag{13}$$

Where t_n represents n^{th} switching instant, $v_{ac1}(t)$ is the coupling transformer primary voltage and $v'_{ac2}(t)$ is the secondary transformer voltage referred to the primary side. According to Figure 4 (a), nine different switching segments emerge that will completely be analysed for this mode.

Interval t_0 - t_1: Figure 5 (a) shows the equivalent circuit during this switching instant. Since the current is negative; i_L, flows through freewheeling diodes D_{S1} and D_{S4} in bridge A due to positive bridge A output voltage. For bridge B, diode D_{Q1} and switch Q_3 conduct the current. The inductor voltage is clamped at V_{DC1}. Therefore, the current is expressed by,

$$i_L(t) = \frac{V_{DC1}}{L_{tot}}\left(t - t_0\right) + i_L(t_0) \tag{14}$$

***Interval** $t_1 - t_1'$:* The polarity of inductor current changes from negative to positive at t_1'. In bridge A, the current flows through switches S_1 and S_4, while for bridge B, the current flows through D_{Q1} and Q_3. The current remains the same as in previous switching instant while continuing to increment. The voltage across the coupling inductor is V_{DC1}. This is depicted in Figure 5 (b).

***Interval** t_1' - t_2:* The equivalent circuit for this segment is shown in Figure 5 (c). Since it is assumed that converter works in buck mode where $V_{DC1} > nV_{DC2}$, therefore current slope is increasing. With both bridges output voltage been positive and a positive inductor current polarity, switches S_1 and S_2 of bridge A remain on. In bridge B, i_L, flows through the reverse recovery diodes, D_{Q1} and D_{Q4}.The resultant voltage across the inductor is V_{DC1}-nV_{DC2}, thus, the inductor current is given by,

$$i_L(t) = \frac{V_{DC1} - nV_{DC2}}{L_{tot}}(t - t_1) + i_L(t_1) \tag{15}$$

***Interval** t_2 - t_3:* S_1 and S_2 of bridge A are still conducting. In secondary bridge B, current flows through Q_2 and D_{Q4} as illustrated in Figure 5 (d). The voltage impressed across inductor is V_{DC1}, thus, current through L_{tot} can be expressed as

$$i_L(t) = \frac{V_{DC1}}{L_{tot}}(t - t_2) + i_L(t_2) \tag{16}$$

***Interval** t_3 - t_4:* Both bridge A and bridge B voltages are zero and Figure 5 (e), depicts, the equivalent circuit. The inductor current remains unchanged and circulates in D_{S2}, S_4, Q_2 and D_{Q4} of both bridges. The voltage across the inductor is zero and thus, the inductor current is

$$i_L(t) = i_L(t_3) \tag{17}$$

***Interval** t_4 - t_4':* Figure 5 (f) shows the equivalent circuit for this duration. Switch S_4 of bridge A is turned off and the current flows through the diagonal anti-parallel diodes D_{S2} and D_{S3} since bridge A voltage is negative. The status of bridge B remains unchanged, where i_L, decreases linearly and is carried by Q_2 and D_{Q4}. Voltage across the inductor is - V_{DC1}. Thus,

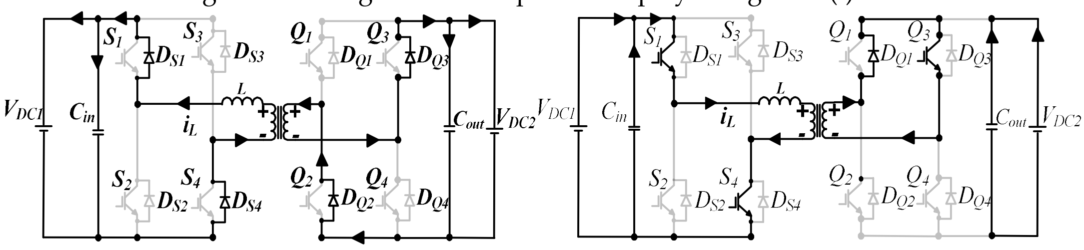
$$i_L(t) = \frac{-V_{DC1}}{L_{tot}}\left(t - t_4\right) + i_L(t_4) \tag{18}$$

***Interval** t_4' - t_5:* The inductor current polarity changes S_2 and S_3 of bridge A freewheel. In bridge B i_L, flows through D_{Q2} and Q_4. The equivalent circuit structure is shown in Figure 5 (g). The inductor voltage remains at -V_{DC1} and the value of inductor current is given by expression (18).

***Interval** t_5 - t_6:* During this sub-period, S_2 and S_3 of bridge A are still on, while D_{Q2} and D_{Q3} conduct for bridge B as Fig.5 (h) demonstrates. The inductor voltage is V_{DC1}+nV_{DC2}. Thus, the inductor current is

$$i_L(t) = \frac{-V_{DC1} + nV_{DC2}}{L_{tot}}(t - t_5) + i_L(t_5) \tag{19}$$

***Interval** t_6 - t_7:* The switching pattern for this sub-period is similar to previous segment t_5-t_6 and equivalent circuit diagram showing the current path is displayed Figure 5 (i). S_2 and S_3 of



(a) (b)

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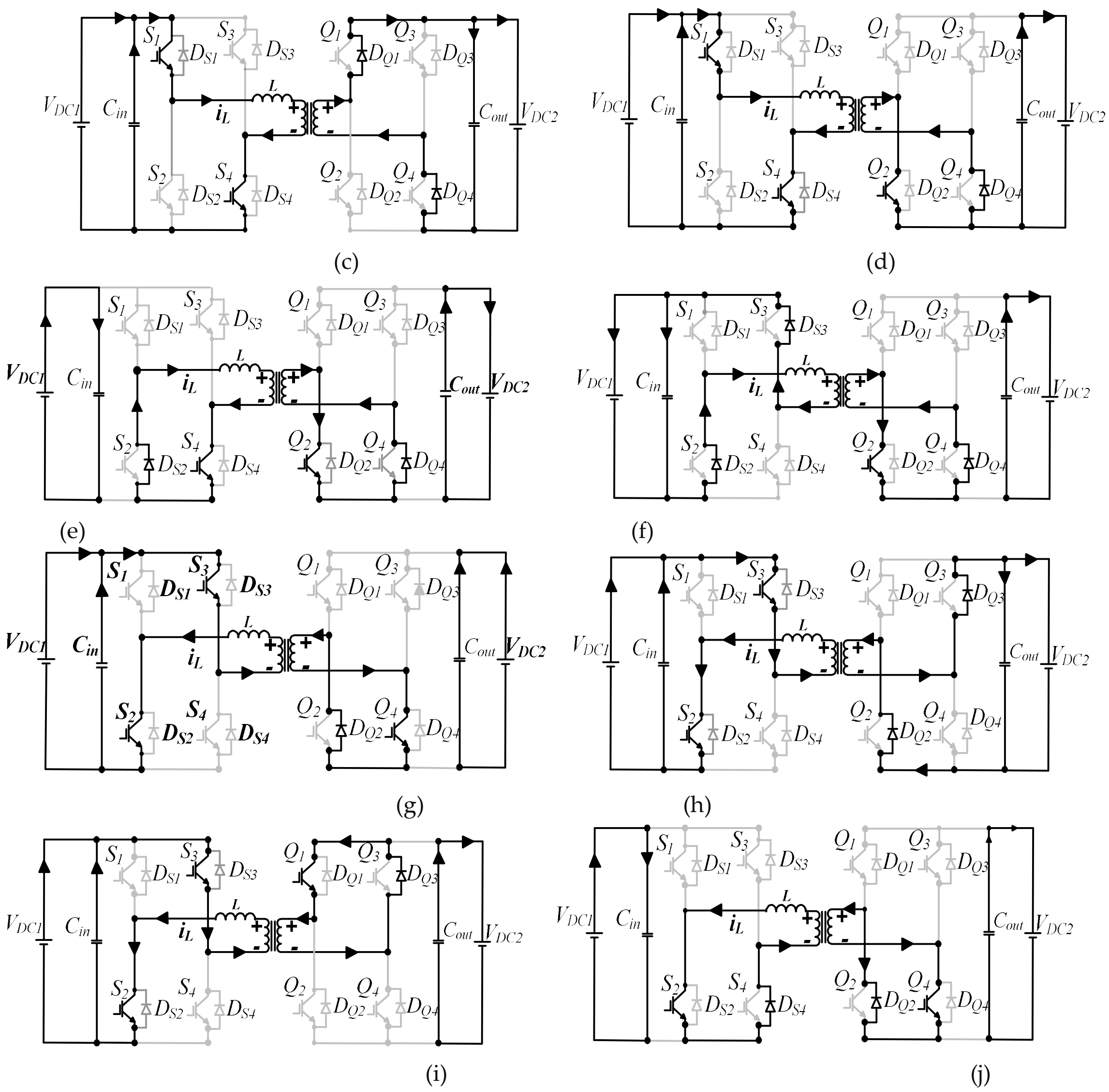

Figure 5. Mode 1 equivalent circuits sub-periods for inductor current (a) t_0-t_1 (b) t_1- t_1' (c) t_1'-t_2 (d) t_2- t_3 (e) t_3- t_4 (f) t_4- t_4' (g) t_4' - t_5 (h) t_5- t_6 (i) t_6- t_7 (i) t_7- t_8.

bridge A continue to conduct. For bridge B switch Q_1 and D_{Q3} conduct. The voltage across the inductor is -V_{DC1}. Therefore, the inductor current is,

$$i_L(t) = \frac{-V_{DC1}}{L_{tot}}\left(t - t_5\right) + i_L(t_6) \tag{20}$$

Interval t_7 **-** t_8**:** Bridge A and bridge B voltages are both zero and thus, the voltage across the inductor is likewise zero as demonstrated by Figure 5 (j). For both H-bridges, S_2, D_{S4}, D_{Q2} and Q_4 conduct respectively. The inductor current during this sub-period is

$$i_L(t) = i_L(t_7) \tag{21}$$

Since the average value of the inductor current $i_L(t)$ for one complete cycle (T_s), has to be zero, it is therefore only necessary to compute the current for the first half cycle. Moreover, due to half-wave symmetry of the inductor current waveform, it can be shown that,

$$\begin{aligned} i_L(t_4) &= -i_L(t_0) \\ i_L(t_5) &= -i_L(t'_1) \\ i_L(t_6) &= -i_L(t_2) \\ i_L(t_7) &= -i_L(t_3) \end{aligned} \tag{22}$$

Considering the volts-second balance of the inductor current, initial inductor current, $i_L(t_o)$, can be derived from equations (14) to (17), by assuming, t_n values of, $t_0=0$, $t'_1=D_3T_h$, $t_2=(D_3+D_2)T_h$, $t_3=D_1T_h$ and $t_4=T_h$. Where, $T_h=T_s/2$.

$$-2i_L(t_0)=\frac{V_{DC1}}{L_{tot}}(t_4-t_3)+\frac{V_{DC1}-nV_{DC2}}{L_{tot}}(t_3-t_2)+\frac{V_{DC1}}{L_{tot}}(t_2-t_1) \tag{23}$$

Substituting values of t_n, in the expression (23) above, $i_L(t_0)$ can be obtained

$$i_L(t_0)=-\left[\frac{V_{DC1}D_1-nV_{DC2}D_2}{4f_sL_{tot}}\right] \tag{24}$$

From (24), the currents for each switching interval can be derived as,

$$\begin{aligned} i_L(t_1)&=\frac{V_{DC1}}{L_{tot}}(t_1-t_0)-\left[\frac{V_{DC1}D_1-nV_{DC2}D_2}{4f_sL_{tot}}\right] \\ &=\left[\frac{2V_{DC1}D_3-V_{DC1}D_1+nV_{DC2}D_2}{4f_sL_{tot}}\right] \end{aligned} \tag{25}$$

$$\begin{aligned} i_L(t_2)&=\frac{V_1-nV_2}{L_{tot}}(t-t_1)+i_L(t_1) \\ &=\left[\frac{2V_{DC1}D_2+2V_{DC1}D_3-V_{DC1}D_1+nV_{DC2}D_2}{4f_sL_{tot}}\right] \end{aligned} \tag{26}$$

$$\begin{aligned} i_L(t_3)&=\frac{V_{DC1}}{L_{tot}}(t_3-t_2)+i_L(t_2) \\ &=\frac{2V_{DC1}D_1-2V_{DC1}D_3-2V_{DC1}D_2}{4f_sL_{tot}}+\left[\frac{2V_{DC1}D_2+2V_{DC1}D_3-V_{DC1}D_1+nV_{DC2}D_2}{4f_sL_{tot}}\right] \\ &=\left[\frac{V_{DC1}D_1-nV_{DC2}D_{DC2}}{4f_sL_{tot}}\right] \end{aligned} \tag{27}$$

$$i_L(t_4)=i_L(t_3) \tag{28}$$

The peak current for this mode of operation is given by

$$i_{peak}=i_L(t_3)=\left|i_L(t_0)\right|=\left[\frac{V_{DC1}D_1-nV_{DC2}D_2}{4f_sL_{tot}}\right] \tag{29}$$

The rms current can be expressed as follows:

$$\begin{aligned} i_{rms(model)}&=\sqrt{\frac{1}{T_h}\int_0^{T_h}\left(i_L(t)^2\right)dt} \\ &=\frac{1}{T_h}\left(\begin{aligned}&\int_{t_0}^{t_1}\left[\frac{V_{DC1}}{L_{tot}}t+i_L(t_0)\,dt\right]^2+\int_{t_1}^{t_2}\left[\frac{V_{DC1}-nV_{DC2}}{L_{tot}}t+i_L(t_1)\,dt\right]^2\\&+\int_{t_2}^{t_3}\left[\frac{V_{DC1}}{L_{tot}}t+i_L(t_2)\,dt\right]^2+\int_{t_3}^{t_4}\left[\frac{V_{DC1}}{L_{tot}}t+i_L(t_3)\,dt\right]^2\end{aligned}\right)^{1/2} \end{aligned} \tag{30}$$

Inserting $t_0=0$, $t_1=D_3T_h$, $t_2=(D_3+D_2)T_h$, $t_3=D_1T_h$,$t_4=T_h$ in (3.19) and rearranging yields,

$$i_{rms(\text{mode1})}=\left(\left[i_L^{2}(t_3)(1-D_1)\right]+\left[\frac{2f_sL_{tot}}{3}\left\{\begin{matrix}\left[\dfrac{i_L^{3}(t_1)-i_L^{3}(t_0)}{V_{DC1}}\right]+\\ \left[\dfrac{i_L^{3}(t_2)-i_L^{3}(t_1)}{V_{DC1}-nV_{DC2}}\right]+\left[\dfrac{i_L^{3}(t_3)-i_L^{3}(t_2)}{V_{DC1}}\right]\end{matrix}\right\}\right]\right)^{1/2} \tag{31}$$

Based on the derived expressions, derivations for active power, reactive power, and ZVS operation possibility for each switch and its range are presented below.

Average power transferred by the converter can be calculated at either bridge, by considering the assumptions made previously,

$$P=\frac{1}{T_h}\int_0^{T_h} v_{ac1}i_L(t)\,dt=\frac{1}{T_h}\int_0^{T_h} v'_{ac2}\,i_L(t)\,dt \tag{32}$$

The transmitted power is obtained as,

$$P_{model}=\frac{1}{T_h}\left[\begin{matrix}\displaystyle\int_0^{t_1-t_0}\left\{v_{ac1}(t)\times\left(\left[\frac{V_{DC1}}{L_{tot}}t+i_L(t_0)\,dt\right]\right)\right\}+\int_0^{t_2-t_1}\left\{v_{ac1}(t)\times\left(\frac{V_{DC1}-nV_{DC2}}{L_{tot}}t+i_L(t_1)\right)\right\}+\\ \displaystyle\int_0^{t_3-t_2}\left\{v_{ac1}(t)\times\left(\frac{V_{DC1}}{L_{tot}}t+i_L(t_2)\right)\right\}+\int_0^{t_4-t_3}\left\{v_{ac1}(t)\times\left(\frac{0}{L_{tot}}t+i_L(t_3)\right)\right\}\end{matrix}\right]dt \tag{33}$$

Simplifying and rearranging expression (3.22) results in,

$$P_{model}=\frac{1}{T_h}\left[\begin{matrix}\displaystyle\int_0^{t_1-t_0}\left\{v_{ac1}(t)\times\left(\left[\frac{V_{DC1}}{L_{tot}}t+i_L(t_0)\,dt\right]\right)\right\}+\int_0^{t_2-t_1}\left\{v_{ac1}(t)\times\left(\frac{V_{DC1}-nV_{DC2}}{L_{tot}}t+i_L(t_1)\right)\right\}+\\ \displaystyle\int_0^{t_3-t_2}\left\{v_{ac1}(t)\times\left(\frac{V_{DC1}}{L_{tot}}t+i_L(t_2)\right)\right\}+\int_0^{t_4-t_3}\left\{v_{ac1}(t)\times\left(\frac{0}{L_{tot}}t+i_L(t_3)\right)\right\}\end{matrix}\right]dt \tag{34}$$

$$=\frac{V_{DC1}}{T_h}\left\{\left[\left(\frac{V_{DC1}}{L_{tot}}\frac{t^2}{2}+i_L(t_0)\times t\right)\right]_{t_0}^{t_1}+\left[\left(\frac{V_{DC1}-nV_{DC2}}{L_{tot}}\frac{t^2}{2}+i_L(t_1)\times t\right)\right]_{t_1}^{t_2}+\left[\left(\frac{V_{DC1}}{L_{tot}}\frac{t^2}{2}+i_L(t_2)\times t\right)\right]_{t_2}^{t_3}\right\}$$

After inserting t_n values and further manipulation of (34), mode 1 active power equation can be derived as

$$P_{model}=\frac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}\left[D_2^{2}-D_1D_2+2D_2D_3\right] \tag{35}$$

From (35), range of power transfer can be determined, in order to characterise mode upper and lower power operation limits. This is performed by first normalising the power equation with respect to maximum power achievable by the converter. This base power is obtained through CPS equation (2) of previous chapter, when external phase shift D=0.5.

$$P_{base}=\frac{nV_{DC1}V_{DC2}}{8f_sL_{tot}} \tag{36}$$

Thus,

$$P_{model(pu)}=2\left[D_2^{2}-D_1D_2+2D_2D_3\right] \tag{37}$$

The maximum and minimum power transfer in per unit and corresponding maximum and minimum TPS control values can be obtained by solving a basic optimisation problem for the normalized power formula (37) and applying the mode operational constraints (12). The required steps to determine these parameters is summarised by flow chart of Figure 6. Results obtained from this are:

$$\begin{aligned}P_{max}&=0.5pu\ \ (D_1=1,D_2=0.5,D_3=0.5)\\ P_{min}&=-0.5pu\ (D_1=1,D_2=0.5,D_3=0.0)\end{aligned} \tag{38}$$

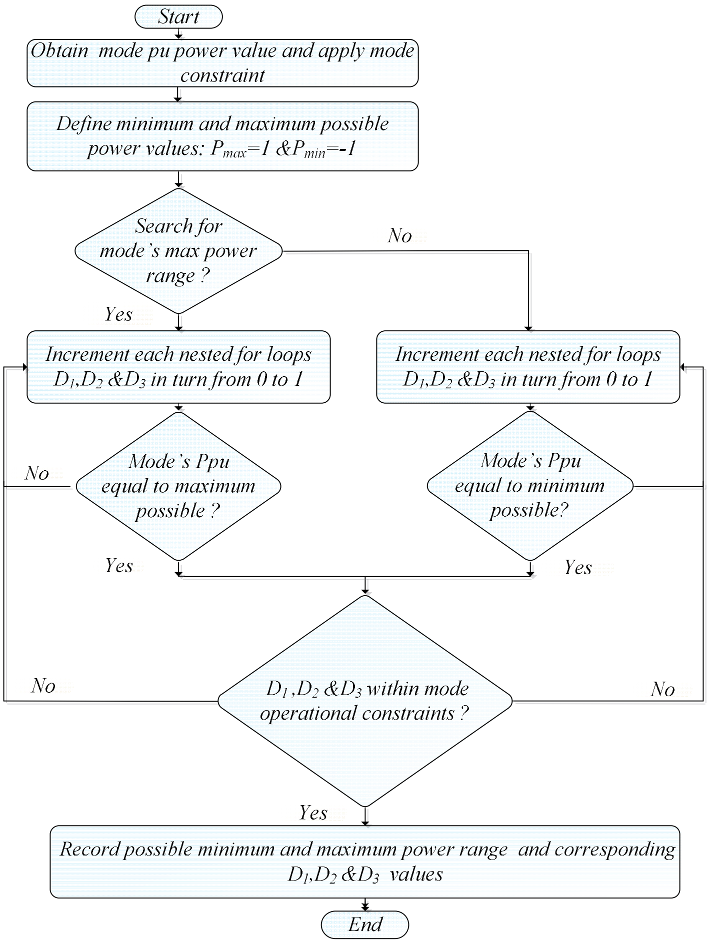

Figure 6. Steps required to establish maximum and minimum power range.

Reactive power is a parameter of interest to investigate in DAB converter, since by reducing reactive power consumption; RMS inductor current is minimised for a specified level of power transfer. This reduces conduction and copper losses. In this paper, reactive power is calculated by computing the apparent power S_L at the inductor. Since inductors do not absorb active power, the apparent power is therefore equivalent to the reactive power consumption by the inductor. This is, by definition equivalent to the total reactive power consumption at the converter H-bridges. Hence, reactive power Q, can be defined by,

$$Q = S_L = V_{L_{RMS}} I_{L_{RMS}} \tag{39}$$

Equation for mode 1 RMS current is denoted in (31). The RMS value for the inductor voltage can be calculated by referring to Figure 4 (a),

$$\begin{aligned} v_{Lrms(\text{mode1})} &= \sqrt{\frac{1}{T_h}\int_0^{T_h} V_L^{\,2}(t)dt} \\ &= \frac{1}{T_h}\left(V^2{}_{DC1}\left(t_1 - t_0\right) + \left(V_{DC1} - nV_{DC2}\right)^2\left(t_2 - t_1\right) + V^2{}_{DC1}\left(t_3 - t_2\right)\right)^{1/2} \end{aligned} \tag{40}$$

Substituting t_n values into (40), mode 1 RMS voltage is

$$v_{Lrms(\text{mode1})} = \left(V_{DC1}{}^2 D_1 + (nV_{DC2})^2 D_2 - 2nV_{DC1}V_{DC2}D_2\right)^{1/2} \tag{41}$$

By, merging equations (31) and (41), a more accurate definition of DAB true reactive power emerges

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$$Q_{\mathrm{mode1}} = \left(\left[\left(V_{DC1}^{\ 2} D_1 + (nV_{DC2})^2 D_2 - 2nV_{DC1} V_{DC2} D_2 \right) \right] \times \left(\begin{array}{l} \left[i_L^{\ 2}(t_3)(1-D_1) \right] + \\ \left[\frac{2 f_s L_{tot}}{3} \left\{ \begin{array}{l} \left[\frac{i_L^{\ 3}(t_1) - i_L^{\ 3}(t_0)}{V_{DC1}} \right] + \left[\frac{i_L^{\ 3}(t_2) - i_L^{\ 3}(t_1)}{V_{DC1} - nV_{DC2}} \right] \\ + \left[\frac{i_L^{\ 3}(t_3) - i_L^{\ 3}(t_2)}{V_{DC1}} \right] \end{array} \right\} \right] \end{array} \right) \right)^{1/2} \quad (42)$$

Assuming IGBT switches, in order to ensure that the converter switches are operating with zero voltage switching (ZVS), anti-parallel diodes must conduct prior to switch turn on. After switch voltage drops to zero, current commutates from the anti-parallel diode to the switch enabling turn on at zero voltage, resulting in zero turn on power loss.Thus , at the instant of switch turn on, current in the switch must be negative. This provides the condition for ZVS. With respect to the switches in Figure 1 (a) and their respective conducting current directions, conditions for the switches ZVS can be summarised as

$$For\ \ S_1, S_4, Q_2, Q_3 \quad i_L\big|_{t=turn\,on} < 0 \ \ \& \ \ For\ \ S_2, S_3, Q_1, Q_4 \quad i_L\big|_{t=turn\,on} > 0 \quad (43)$$

- Generation of inequality for each switch, by observing the instant the switch starts to conduct first.

$$\left\{ \begin{array}{l} S_1 = \left\{ \begin{array}{l} i_L(t_7) < 0 \\ i_L(t_3) > 0 \\ i_L(t_0) < 0 \end{array} \right\} \\ S_2 = \left\{ \begin{array}{l} i_L(t_3) > 0 \\ i_L(t_0) < 0 \end{array} \right\} \\ S_3 = \left\{ \begin{array}{l} i_L(t_4) > 0 \\ i_L(t_0) < 0 \end{array} \right\} \\ S_4 = \left\{ i_L(t_0) < 0 \right\} \end{array} \right. \quad \& \quad \left\{ \begin{array}{l} Q_1 = \left\{ \begin{array}{l} i_L(t_6) > 0 \\ i_L(t_2) < 0 \end{array} \right\} \\ Q_2 = \left\{ i_L(t_2) < 0 \right\} \\ Q_3 = \left\{ \begin{array}{l} i_L(t_5) < 0 \\ i_L(t_1) > 0 \end{array} \right\} \\ Q_4 = \left\{ i_L(t_1) > 0 \right\} \end{array} \right. \quad (44)$$

- Summarise inequalities of expression (44) by removing redundant expressions and check if the inequality doesn't contradict the current waveform.

$$\begin{array}{l} i_L(t_0) < 0 \\ i_L(t_1) > 0 \\ i_L(t_2) < 0 \end{array} \quad (45)$$

- By mapping (45) to the respective segments of the inductor current of Figure 3 (a), inequality $i_L(t_2) < 0$ introduces a conflict and hence, for this mode, it can be concluded that soft switching is not possible for all DAB converter switches.Note that, this is applicable when the voltage conversion ratio $\frac{nV_{DC2}}{V_{DC1}} < 0$. When, $\frac{nV_{DC2}}{V_{DC1}} > 0$, the resulting condition might be different.

i. **Mode 1'**

Mode1' is essentially the mode generating equal power in magnitude to mode 1 but in reverse direction. Hence, bridge B voltage waveform is shifted by 180°. Therefore, the boundary condition is defined by full overlap of positive and negative half cycles of the bridges AC voltage waveforms as Figure 4 (b) depicts. The same methodology can be adapted to derive the mode constraint as in previous mode and by extending the mode voltage waveforms to the negative half plane, it can be concluded that the following mode 1'constraints have to be maintained,

$$\begin{array}{l} D_2 \le D_1 \\ -1 \le D_3 \le -1 + D_1 - D_2 \end{array} \quad (50)$$

Analysis for various switching instants of the inductor current is performed prior to deriving key parameters. Nine distinct segments emerge as illustrated in the Figure 4 (b). The second half cycle

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operation is similar, but with inverted inductor current and complimentary switches conducting, the equivalent circuit and steady state value of the inductor current for the first half period is defined for convenience and this will, likewise, also be the case for all the remaining operating modes.

Interval t_0 **-** t_1**:** The inductor current is negative during this switching state and the resulting equivalent circuit is demonstrated by Figure 7 (a). Switches S_1 and S_4, are in the direct conduction path, the current free wheels through integrated anti-parallel diodes D_{S1} and D_{S4} for Bridge A. While for Bridge B, the current flows through D_{Q2} and Q_4 respectively. The voltage across the inductor is V_{DC1}. Inductor current is given by

$$i_L(t) = \frac{V_{DC1}}{L_{tot}}(t - t_0) + i_L(t_0) \tag{51}$$

Interval t_1 **-** t_1'**:** Figure 7 (b) depicts the equivalent circuit for this time segment. In bridge A, i_L flows through diodes D_{S1} and D_{S4}. Similarly, the current in bridge B freewheels through reverse recovery diodes D_{Q2} and D_{Q3}.Inductor voltage is clamped at V_{DC1}+nV_{DC2}.

$$i_L(t) = \frac{V_{DC1} + nV_{DC2}}{L_{tot}}(t - t_1) + i_L(t_1) \tag{52}$$

Interval t_1'**-** t_2**:** Current polarity reverses for this time duration, whilst linearly increasing, plotted by circuit diagram of Figure 3.6 (c). Switches S_1 and S_4 of bridge A are condu cting, while in Bridge B the current flows through Q_2 and Q_3. Inductor voltage is still clamped at $V_{DC1}+nV_{DC2}$. The current is similarly given by (52). The interval ends upon Q_2 turn off.

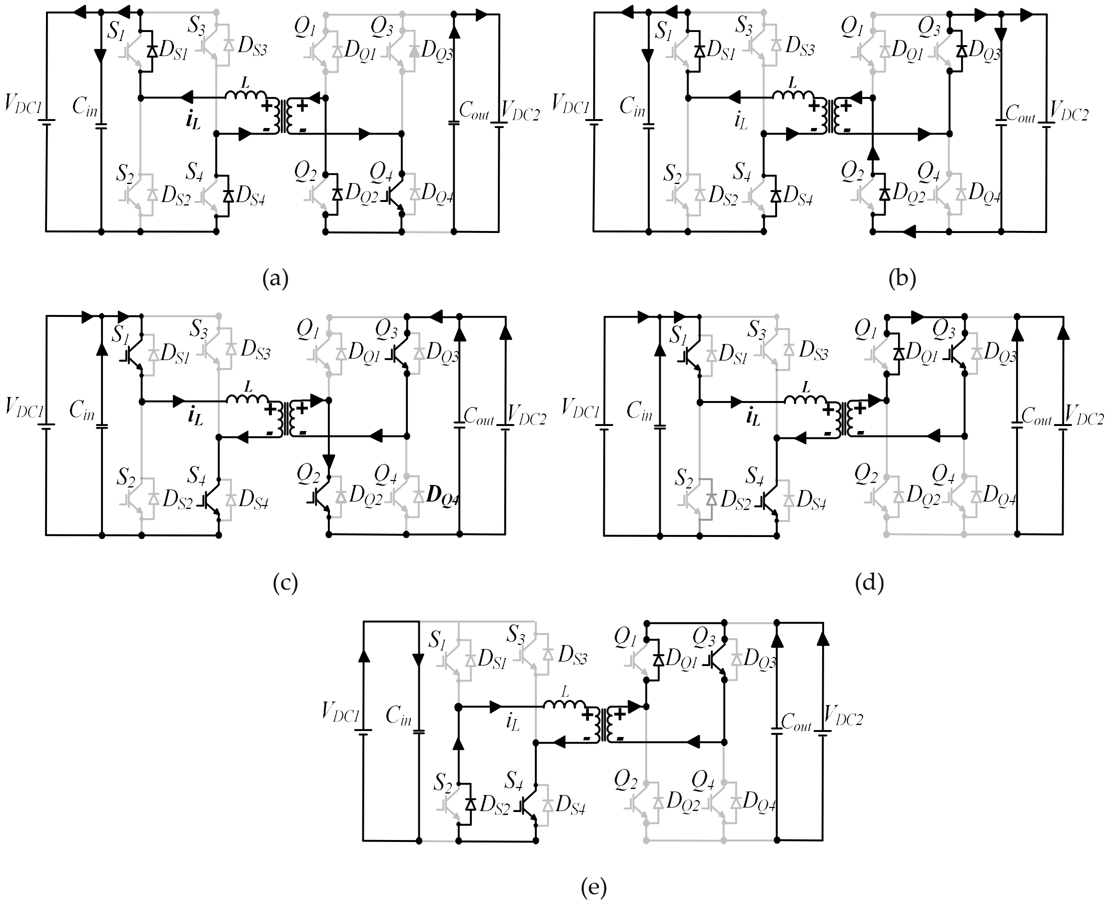

Figure 7. Mode 1′ equivalent circuits sub-periods for inductor current (a) t_0-t_1 (b) t_1-t'_1 (c) t'_1-t_2 (d) t_2- t_3 (e) t_3- t_4 .

Interval t_2 **-** t_3**:** Figure 7 (d), demonstrates the equivalent circuit showing the current path during this duration. For bridge A, the same switches continue to conduct as in previous segment,

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while in bridge B the current freewheels in diode D_{Q1} and flows through switch Q_3. The inductor voltage is V_{DC1}. Inductor current for this segment can be written as

$$i_L(t) = \frac{V_{DC1}}{L_{tot}}(t - t_2) + i_L(t_2) \tag{53}$$

Interval $t_3 - t_4$: The schematic circuit showing the current path during this time instant is displayed in Figure 3.6 (e). Both bridge terminal voltages are zero and thus no power is transferred. The current circulates through D_{S1} and S_4, in bridge A. For bridge B the current path remains the same as in previous interval. The inductor current slope is zero and thus, its value is given by (3.38).

By substituting, t_n values of, $t_0=0$, $t_1=(1-|D_3|)T_h$, $t_2=(1-|D_3|+ D_2)T_h$, $t_3=D_1T_h$ and $t_4=T_h$, one can evaluate expressions comprising the inductor current at various switching instant, peak current, , RMS current, along with, the average power, reactive power and ZVS constraints,

Table 1. Key expressions for Mode 1′.

Variable	
Currents at each switching instants	$i_L(t_0) = -\left[\frac{V_{DC1}D_1 + nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_1) = \left[\frac{-V_{DC1}D_1 - 2V_{DC1}\lvert D_3\rvert + 2V_1 - nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_2) = \left[\frac{-V_{DC1}D_1 + 2V_{DC1} + 2V_{DC1}D_2 - 2V_{DC1}\lvert D_3\rvert + nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_3) = \left[\frac{V_{DC1}D_1 + nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_4) = i_L(t_3)$
RMS current	$I_{rms(model')} = \left(\left[i_L^2(t_3)(1-D_1)\right] + \left[\frac{2f_sL_{tot}}{3}\left\{\left[\frac{i_L^3(t_1) - i_L^3(t_0)}{V_{DC1}}\right] + \left[\frac{i_L^3(t_2) - i_L^3(t_1)}{V_{DC1} + nV_{DC2}}\right] + \left[\frac{i_L^3(t_3) - i_L^3(t_2)}{V_{DC1}}\right]\right\}\right]\right)^{1/2}$
RMS voltage	$V_{Lrms(model')} = \left(V_{DC1}{}^2D_1 + (nV_{DC2})^2 D_2 + 2nV_{DC1}V_{DC2}D_2\right)^{1/2}$
Average power & range	$P_{(model')} = -\frac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}\left[D_2^2 + 2D_2 - D_1D_2 - 2D_2\lvert D_3\rvert\right]$ ***Range:*** ➡ $\begin{cases} P_{max} = 0.5pu & (D_1 = 1, D_2 = 0.5, D_3 = -1) \\ P_{min} = -0.5pu & (D_1 = 1, D_2 = 0.5, D_3 = -0.5) \end{cases}$
Reactive power	$Q_{model'} = v_{rms(model')} \times i_{rms(model')}$
ZVS	*Achievable for all switches* ***Constraints:*** $i_L(t_0) < 0, i_L(t_1) < 0 \ \& \ i_L(t_2) > 0$

following similar steps outlined in mode 1. To reduce the number of equations, the final derivation of this expressions is summarized in Table 1.

According to the results obtained, it can be observed in Table 1 that mode peak current is given by $i_L(t_3)$. The derived per unit values for upper and lower mode active power limits which is ±0.5 *pu*, is also evaluated by applying a similar optimization problem procedure as in mode 1, while decrementing D_3 from 0 to -1 (rather than incrementing). The corresponding TPS modulation parameters that achieve these limits are also tabulated. By also taking a similar approach for determination of ZVS, as in mode 1, soft switching operation is possible for all the switches as long as the ZVS constraint given in Table 3.1, are satisfied.

Even though, the obtained mode steady state equations look dissimilar to previous derivations defined for mode 1, it can be shown that by substituting $|D_3| = 1 - D_3$, in expressions of mode1′, results in inverted but identical equations of mode 1, which verifies the complementary nature of this mode, compared to mode 1.

All other remaining modes of operations 2 to 6 and their respective complements, which are graphically represented in Figure 8, are analysed in Appendix A, following similar procedure as in preceding TPS modes above.

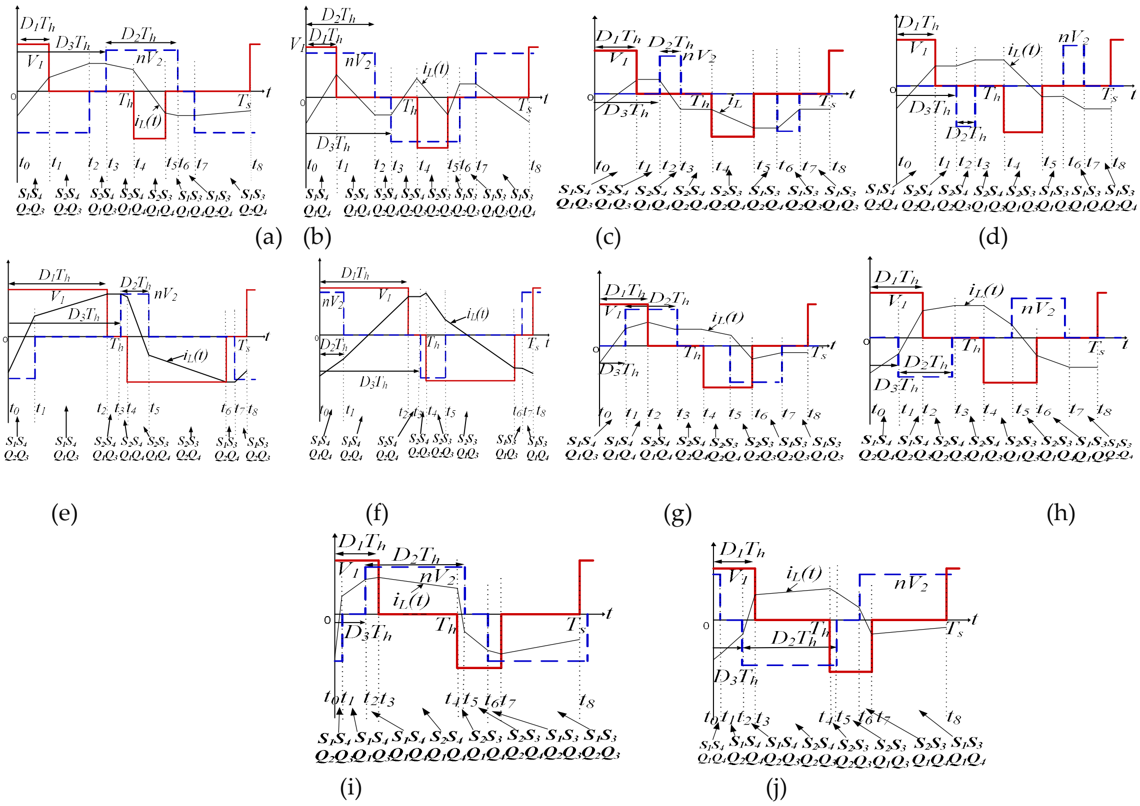

Figure 8. Remaining modes steady state voltages and current (a) Mode 2 (b) Mode 2′(c) Mode3 (d) Mode 3′ (e) Mode 4 (f) Mode 4′(g) Mode 5 (g) Mode 5′ (h) Mode 6 (i) Mode 6′.

Normalised inductor currents to $(1/4f_sL)$, for the positive half cycle switching instants are derived and listed for the remaining modes in Table II (where f_s is the switching frequency). Detailed derivation of the currents for each mode can be found in the appendix. Due to inductor current half-wave symmetry, negative half cycle values are omitted. These can be calculated by counter positive half cycle values.

The per unit average power normalised to maximum power transferred by the converter is listed in Table 3 for the remaining modes. The base power used is obtained with CPS modulation at 90^0 phase shift between the two half bridge voltages.

$$P_{base} = \frac{nV_1V_2}{8f_sL} \quad (54)$$

Range of power transfer for each mode is also computed to characterise mode limits, by applying the mode operational constraints to the computed power equations. This shows the converter, power transfer, capability with respect to the full range under specific mode of operation. In complementary modes, bridge 2 waveform is shifted by 180^0 from non-complimentary mode, hence resulting in the exact but negative power range. From Table 3, it can be seen that modes 6 and 6′ are the only modes that cover the whole converter operating power range.

Modes 1, 1′, 2 and 2′are capable of charging and discharging operation, but only for half the power range. Modes 3, 4, 5 and 6 with their complements only provide unidirectional power transfer capability each. Finally, it is worth noting that, in mode 3 and 3′ power transfer is independent of D_3, meaning that it can be solely controlled by controlling bridge voltages. The ZVS constraints are derived and also listed in Table 4. Only modes where ZVS is realisable for all switches are indicated with their constraints. Otherwise ZVS is only partially obtained for the converter, i.e., for some switches only as indicated by modes 1, 3, 3′ and 5. The, RMS current, RMS voltage and and the reactive power for the remaining modes are listed in Table 4.

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Table 2. Inductor currents (i_L) for positive half cycle switching intervals normalized to $1/4f_sL$.

Modes	$i_L(t_0)$	$i_L(t_1)$	$i_L(t_2)$	$i_L(t_3)$
2	$-[V_1D_1-2nV_2+nV_2D_2+2nV_2D_3]$	$[V_1D_1+2nV_2D_1-nV_2D_2+2nV_2-2nV_2D_3]$	$[V_1D_1+nV_2D_2]$	$[V_1D_1+nV_2D_2]$
2′	$-[V_1D_1+2nV_2-nV_2D_2-2nV_2D_3]$	$[V_1D_1-2nV_2-2nV_2D_1+nV_2D_2+2nV_2D_3]$	$[V_1D_1-nV_2D_2]$	$[V_1D_1-nV_2D_2]$
3	$-[V_1D_1-nV_2D_2]$	$[V_1D_1+nV_2D_2]$	$[V_1D_1+nV_2D_2]$	$[V_1D_1-nV_2D_2]$
3′	$-[V_1D_1+nV_2D_2]$	$[V_1D_1-nV_2D_2]$	$[V_1D_1-nV_2D_2]$	$[V_1D_1+nV_2D_2]$
4	$-[V_1D_1-2nV_2+nV_2D_2+2nV_2D_3]$	$[-V_1D_1-2V_1+2V_1D_2+nV_2D_2+2V_1D_3]$	$[V_1D_1+nV_2D_2]$	$[V_1D_1+nV_2D_2]$
4′	$-[V_1D_1+2nV_2-nV_2D_2-2nV_2D_3]$	$[-V_1D_1-2V_1+2V_1D_2+2V_1D_3-nV_2D_2]$	$[V_1D_1-nV_2D_2]$	$[V_1D_1-nV_2D_2]$
5	$-[V_1D_1-nV_2D_2]$	$[-V_1D_1+2V_1D_3+nV_2D_2]$	$[V_1D_1-2nV_2D_1+nV_2D_2+2nV_2D_3]$	$[V_1D_1-nV_2D_2]$
5′	$-[V_1D_1+nV_2D_2]$	$[-V_1D_1+2V_1D_3-nV_2D_2]$	$[V_1D_1+2nV_2D_1-nV_2D_2-2nV_2D_3]$	$[V_1D_1+nV_2D_2]$
6	$-[V_1D_1+nV_2D_2+2nV_2D_3-2nV_2]$	$[-V_1D_1+2V_1D_2+2V_1D_3+nV_2D_2-2V_1]$	$[-V_1D_1+2V_1D_3+nV_2D_2]$	$[V_1D_1-2nV_2D_1+nV_2D_2+2nV_2D_3]$
6′	$-[V_1D_1-nV_2D_2-2nV_2D_3+2nV_2]$	$[-V_1D_1+2V_1D_2+2V_1D_3-nV_2D_2-2V_1]$	$[-V_1D_1+2V_1D_3-nV_2D_2]$	$[V_1D_1+2nV_2D_1-nV_2D_2-2nV_2D_3]$

Table 3. Remaining DAB modes of operation & power equations using TPS control.

			Mode 2	*Mode 2′*
Mode operational constraints			$D_2 \geq D_1$ $(1+D_1-D_2) \leq D_3 \leq 1$	
Power & power range (pu)			$P_{pu}=2[D_1^2-D_1D_2+2D_1-2D_1D_3]$ $Range: P_{max}=0.5pu, P_{min}=-0.5pu$	$P_{pu}=-2[D_1^2-D_1D_2+2D_1-2D_1D_3]$ $Range: P_{max}=0.5pu, P_{min}=-0.5pu$
	Mode 3	*Mode 3′*	*Mode 4*	*Mode 4′*
	$t_o=0, t_1=D_1T_h, t_2=D_3T_h, t_3=(D_2+D_3)T_h, t_4=T_h=\frac{1}{2f_s}$		$t_o=0, t_1=(D_2+D_3-1)T_h, t_2=D_1T_h, t_3=D_3T_h, t_4=T_h=\frac{1}{2f_s}$	
Mode operational constraints	$D_2 \leq 1-D_1$ $D_1 \leq D_3 \leq 1-D_2$		$D_1 \leq D_3 \leq 1$ $1-D_3 \leq D_2 \leq 1-D_3+D_1$	

Power & power range (pu)	$P_{pu} = 2\left[D_1 D_2\right]$ $Range: P_{\max} = 0.5\,pu\,, P_{\min} = 0\,pu$	$P_{pu} = -2\left[D_1 D_2\right]$ $Range: P_{\max} = 0.0\,pu\,, P_{\min} = -0.5\,pu$	$P_{pu} = 2\begin{bmatrix} -D_2^2 - D_3^2 + 2D_2 + 2D_3 \\ -2D_2 D_3 + D_1 D_2 - 1 \end{bmatrix}$ $Range: P_{\max} = 0.67\,pu\,, P_{\min} = 0\,pu$	$P_{pu} = -2\begin{bmatrix} -D_2^2 - D_3^2 + 2D_2 + 2D_3 \\ -2D_2 D_3 + D_1 D_2 - 1 \end{bmatrix}$ $Range: P_{\max} = 0\,pu\,, P_{\min} = -0.67\,pu$
	Mode 5	***Mode 5′***	***Mode 6***	***Mode 6′***
	$t_o = 0, t_1 = D_3 T_h, t_2 = D_1 T_h, t_3 = \left(D_2 + D_3\right) T_h, t_4 = T_h = \dfrac{1}{2 f_s}$		$t_o = 0, t_1 = \left(D_2 + D_3 - 1\right) T_h, t_2 = D_3 T_h, t_3 = D_1 T_h, t_4 = T_h = \dfrac{1}{2 f_s}$	
Mode operational constraints	$D_1 - D_3 \le D_2 \le 1 - D_3$ $0 \le D_3 \le D_1$		$1 - D_2 \le D_1$ $1 - D_2 \le D_3 \le D_1$	
Power & power range (pu)	$P_{pu} = 2\left[-D_1^2 - D_3^2 + D_2 D_1 + 2D_1 D_3\right]$ $Range: P_{\max} = 0.667\,pu, P_{\min} = 0\,pu$	$P_{pu} = -2\left[-D_1^2 - D_3^2 + D_2 D_1 + 2D_1 D_3\right]$ $Range: P_{\max} = 0\,pu, P_{\min} = -0.667\,pu$	$P_{pu} = 2\begin{bmatrix} -D_1^2 - D_2^2 - 2D_3^2 + 2D_3 - 2D_2 D_3 \\ +D_1 D_2 + 2D_1 D_3 + 2D_2 \ -1 \end{bmatrix}$ $Range: P_{\max} = 1\,pu, P_{\min} = 0\,pu$	$P_{pu} = -2\begin{bmatrix} -D_1^2 - D_2^2 - 2D_3^2 + 2D_3 - 2D_2 D_3 \\ +D_1 D_2 + 2D_1 D_3 + 2D_2 \ -1 \end{bmatrix}$ $Range: P_{\max} = 0\,pu, P_{\min} = -1\,pu$

Table 4. ZVS constraints, RMS currents and reactive power for the remaining modes.

			Mode 2	***Mode 2′***
ZVS possible for all switches? Constraints			*YES* $i_L(t_0) < 0, i_L(t_1) > 0 \,\&\, i_L(t_2) > 0$	*YES* $i_L(t_0) < 0, i_L(t_1) > 0 \,\&\, i_L(t_2) < 0$
Reactive power (Q)			$v_{rms2} = \sqrt{\left[V_1^2 D_1 + n^2 V_2^2 D_2 + 2nV_1 V_2 D_1\right]}$ $i_{rms2} = \sqrt{\left\{\begin{matrix} \left[i_L^2(t_2)\left(1 - D_2\right)\right] + \\ \left[\dfrac{2 f_s L}{3}\left\{\begin{matrix} \left[\dfrac{i_L^3(t_1) - i_L^3(t_0)}{V_1 + nV_2}\right] + \\ \left[\dfrac{i_L^3(t_2) - i_L^3(t_1)}{nV_2}\right] + \left[\dfrac{i_L^3(t_0) + i_L^3(t_3)}{nV_2}\right] \end{matrix}\right\}\right] \end{matrix}\right\}}$ $Q_2 = v_{rms2} \times i_{rms2}$	$v_{rms2'} = \sqrt{\left[V_1^2 D_1 + n^2 V_2^2 D_2 - 2nV_1 V_2 D_1\right]}$ $i_{rms2'} = \sqrt{\left\{\begin{matrix} \left[i_L^2(t_2)\left(1 - D_2\right)\right] + \\ \left[\dfrac{2 f_s L}{3}\left\{\begin{matrix} \left[\dfrac{i_L^3(t_1) - i_L^3(t_0)}{V_1 - nV_2}\right] - \\ \left[\dfrac{i_L^3(t_2) - i_L^3(t_1)}{nV_2}\right] - \left[\dfrac{i_L^3(t_0) + i_L^3(t_3)}{nV_2}\right] \end{matrix}\right\}\right] \end{matrix}\right\}}$ $Q_{2'} = v_{rms2'} \times i_{rms2'}$
	Mode 3	***Mode 3′***	***Mode 4***	***Mode 4′***
	NO	*NO*	*YES*	*NO*

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ZVS possible for all switches? *Constraints*	-	-	$i_L(t_0)<0, i_L(t_1)>0 \,\&\, i_L(t_2)>0$	-
Reactive power (Q)	$v_{rms3}=\sqrt{\left[V_1^2D_1+n^2V_2^2D_2\right]}$ $i_{rms3}=\sqrt{\left\{\left[\left[i_L^2(t_1)(D_3-D_1)\right]+\left[i_L^2(t_3)(1-D_2-D_3)\right]\right]+\left[\frac{2f_sL}{3}\left\{\left[\frac{i_L^3(t_1)-i_L^3(t_0)}{V_1}\right]-\left[\frac{i_L^3(t_3)-i_L^3(t_2)}{nV_2}\right]\right\}\right]\right\}}$ $Q_3=v_{rms3}\times i_{rms3}$	$v_{rms3'}=\sqrt{\left[V_1^2D_1+n^2V_2^2D_2\right]}$ $i_{rms3'}=\sqrt{\left\{\left[\left[i_L^2(t_1)(D_3-D_1)\right]+\left[i_L^2(t_3)(1-D_2-D_3)\right]\right]+\left[\frac{2f_sL}{3}\left\{\left[\frac{i_L^3(t_1)-i_L^3(t_0)}{V_1}\right]+\left[\frac{i_L^3(t_3)-i_L^3(t_2)}{nV_2}\right]\right\}\right]\right\}}$ $Q_{3'}=v_{rms3'}\times i_{rms3'}$	$v_{rms4}=\sqrt{\left[V_1^2D_1+n^2V_2^2D_2+2nV_1V_2(D_2+D_3-1)\right]}$ $i_{rms4}=\sqrt{\left\{\left[i_L^2(t_3)(D_3-D_1)\right]+\left[\frac{2f_sL}{3}\left\{\left[\frac{i_L^3(t_1)-i_L^3(t_0)}{V_1+nV_2}\right]+\left[\frac{i_L^3(t_2)-i_L^3(t_1)}{V_1}\right]+\left[\frac{i_L^3(t_3)+i_L^3(t_0)}{nV_2}\right]\right\}\right]\right\}}$ $Q_4=v_{rms4}\times i_{rms4}$	$v_{rms4'}=\sqrt{\left[V_1^2D_1+n^2V_2^2D_2-2nV_1V_2(D_2+D_3-1)\right]}$ $i_{rms4'}=\sqrt{\left\{\left[i_L^2(t_3)(D_3-D_1)\right]+\left[\frac{2f_sL}{3}\left\{\left[\frac{i_L^3(t_1)-i_L^3(t_0)}{V_1-nV_2}\right]+\left[\frac{i_L^3(t_2)-i_L^3(t_1)}{V_1}\right]-\left[\frac{i_L^3(t_3)+i_L^3(t_0)}{nV_2}\right]\right\}\right]\right\}}$ $Q_{4'}=v_{rms4'}\times i_{rms4'}$
	Mode 5	***Mode 5′***	***Mode 6***	***Mode 6′***
ZVS possible for all switches? *Constraints*	NO -	YES $i_L(t_0)<0, i_L(t_1)<0 \,\&\, i_L(t_2)>0$	YES $i_L(t_0)<0, i_L(t_1)>0, i_L(t_2)>0 \,\&\, i_L(t_3)>0$	YES $i_L(t_0)<0, i_L(t_1)<0, i_L(t_2)<0 \,\&\, i_L(t_3)>0$
Reactive power (Q)	$v_{rms5}=\sqrt{\left[V_1^2D_1+n^2V_2^2D_2+2nV_1V_2(D_3-D_1)\right]}$ $i_{rms5}=\sqrt{\left\{\left[i_L^2(t_3)(1-D_2-D_3)\right]+\left[\frac{2f_sL}{3}\left\{\left[\frac{i_L^3(t_1)-i_L^3(t_0)}{V_1}\right]+\left[\frac{i_L^3(t_2)-i_L^3(t_1)}{V_1-nV_2}\right]-\left[\frac{i_L^3(t_3)-i_L^3(t_2)}{nV_2}\right]\right\}\right]\right\}}$ $Q_5=v_{rms5}\times i_{rms5}$	$v_{rms5'}=\sqrt{\left[V_1^2D_1+n^2V_2^2D_2+2nV_1V_2(D_1-D_3)\right]}$ $i_{irms5'}=\sqrt{\left\{\left[i_L^2(t_3)(1-D_2-D_3)\right]+\left[\frac{2f_sL}{3}\left\{\left[\frac{i_L^3(t_1)-i_L^3(t_0)}{V_1}\right]+\left[\frac{i_L^3(t_2)-i_L^3(t_1)}{V_1+nV_2}\right]+\left[\frac{i_L^3(t_3)-i_L^3(t_2)}{nV_2}\right]\right\}\right]\right\}}$ $Q_{5'}=v_{rms5'}\times i_{irms5'}$	$v_{rms6}=\sqrt{\left[V_1^2D_1+n^2V_2^2D_2+2nV_1V_2(D_2+2D_3-D_1-1)\right]}$ $i_{rms6}=\sqrt{\left[\frac{2f_sL}{3}\left\{\left[\frac{i_L^3(t_1)-i_L^3(t_0)}{V_1+nV_2}\right]+\left[\frac{i_L^3(t_2)-i_L^3(t_1)}{V_1}\right]+\left[\frac{i_L^3(t_3)-i_L^3(t_2)}{V_1-nV_2}\right]+\left[\frac{i_L^3(t_0)+i_L^3(t_3)}{nV_2}\right]\right\}\right]}$ $Q_6=v_{rms6}\times i_{rms6}$	$v_{rms6'}=\sqrt{\left[V_1^2D_1+n^2V_2^2D_2+2nV_1V_2(D_1-D_2-2D_3+1)\right]}$ $i_{rms6'}=\sqrt{\left[\frac{2f_sL}{3}\left\{\left[\frac{i_L^3(t_1)-i_L^3(t_0)}{V_1-nV_2}\right]+\left[\frac{i_L^3(t_2)-i_L^3(t_1)}{V_1}\right]+\left[\frac{i_L^3(t_3)-i_L^3(t_2)}{V_1+nV_2}\right]-\left[\frac{i_L^3(t_0)+i_L^3(t_3)}{nV_2}\right]\right\}\right]}$ $Q_{6'}=v_{rms6'}\times i_{rms6'}$

3. Generalization of TPS control scheme

From the analysis presented in previous sections, TPS control can be generalised for all known phase shift modulation techniques. To illustrate this, the following examples are considered by applying the mode operational constraints defined in previous section.

i. **Conventional phase shift (CPS):** This is defined by D_1=1, D_2=1. Applying this definition to modes 6 and 6′ yields $0 \le D_3 \le 1$. CPS is therefore fully achieved with these two modes.

ii. **Dual phase shift (DPS):** This is characterized by $D_1=D_2=D$. Applying this definition to modes 6 and 6′ yields $D \ge 0.5$ and $1-D \le D_3 \le D$. This does not represent the complete control range for D. Considering modes 3 and 3′, if $D_1=D_2=D$, therefore $D \le 0.5$ and $D \le D_3 \le 1-D$. Consequently, modes 3, 3′, 6 and 6′ can cover the whole operating range for DPS.

iii. **Extended phase shift (EPS):** This is defined by either bridge voltage being a full square wave with the other bridge voltage controlled to be a quasi-square wave. Considering modes 6 and 6′, if

- D_1=1, therefore $D_2 \ge 0$ and $1-D_2 \le D_3 \le 1$
- D_2=1, therefore $D_1 \ge 0$ and $0 \le D_3 \le D_1$

EPS can therefore partially be achieved with modes 6 and 6′. Modes 1, 1′, 2 and 2′ cover the remaining EPS range of operation.

For Modes 1 and 1′, if:

- D_1=1, therefore $D_2 \le 1$ and $0 \le D_3 \le 1-D_2$

For Modes 2 and 2′, if:

- D_2=1, therefore $D_1 \le 1$ and $D_1 \le D_3 \le 1$

4. Optimization example using reactive power minimization algorithm

The following section outlines the implementation of generic per unit system TPS algorithm, that aims to reduce the converter reactive power flow, considering the complete operating range of -1 pu to 1 pu. Circulating RMS current can also be used if desired to minimize, rather than reactive power. Detailed algorithm features to overcome reactive power losses are discussed, while extensive theoretical and experimental evaluation are also performed. In TPS control, phase shift parameters D_1, D_2 and D_3 are varied to achieve the required output power transfer, with the objective of enhancing regulation flexibility of the converter, compared to CPS, EPS and DPS schemes. This leads to several TPS modes meeting the same reference power requirement as illustrated in Figure 9, but rather, with different reactive power loss values. To exemplify the task required, in order to determine optimum mode, consider an active reference power requirement for 0.3 p.u as an example for a given DC link voltages. According to Figure 9, modes 1, 1′, 2, 2′, 3, 4, 5 and 6, meet the required power to be transferred. Hence, a multi-step optimization procedure eliminates modes which cause unnecessarily high circulating reactive power through selection of optimum TPS mode, from all possible operating modes fulfilling the required reference power. Once the optimum mode is determined, the corresponding TPS phase shift combination satisfying minimum reactive power generated are listed.

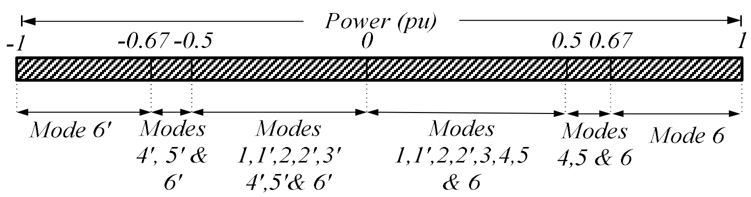

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Figure 9. Map of TPS modes vs output power ranges in *pu*.

In this reactive power optimization algorithm, The first step is to convert all modes derived peak current, RMS currents, RMS voltages, active and reactive powers into *pu* system. These base values are defined as follows:

$$\begin{aligned} V_{base} &= V_{DC1} = V_{DC1(pu)} \\ Z_{base} &= 8 f_s L_{tot} \\ I_{base} &= \frac{V_{DC1}}{8 f_s L_{tot}} \\ P_{base} &= \frac{V^2{}_{DC1}}{8 f_s L_{tot}} \\ Q_{base} &= \frac{V^2{}_{DC1}}{8 f_s L_{tot}} \end{aligned} \tag{55}$$

The resulting *pu* expressions are independent of L_{tot} and f_s, as an example of instantaneous inductor current and power equations of (56), (57) and (58) for mode 1 shows below

$$\begin{aligned} i_L(t_0)_{(pu)} &= -\left[2V_{DC1(pu)}D_1 - 2nV_{DC2_{(pu)}}D_2\right] \\ i_L(t_1)_{(pu)} &= \left[4V_{DC1_{(pu)}}D_3 - 2V_{DC1_{(pu)}}D_1 + 2nV_{DC2_{(pu)}}D_2\right] \\ i_L(t_2)_{(pu)} &= \left[4V_{DC1(pu)}D_2 + 4V_{DC1(pu)}D_3 - 2V_{DC1_{(pu)}}D_1 + 2nV_{DC2_{(pu)}}D_2\right] \\ i_L(t_3)_{(pu)} &= \left[2V_{DC1_{(pu)}}D_1 - 2nV_{DC2_{(pu)}}D_{DC2}\right] \end{aligned} \tag{56}$$

$$P_{model(pu)} = \frac{nV_{DC2(pu)}\left[D_2^{\,2} - D_1D_2 + 2D_2D_3\right]}{V_{DC1(pu)}} \tag{57}$$

$$Q_{model(pu)} = \left(\left[\left(V_{DC1(pu)}{}^2 D_1 + (nV_{DC2})_{(pu)}{}^2 D_2 - 2nV_{DC1(pu)}V_{DC2(pu)}D_2\right)\right] \times \left(\left[i_{L(pu)}{}^2(t_3)(1-D_1)\right] + \left[\frac{1}{12} \left\{ \left[\frac{i_{L(pu)}{}^3(t_1) - i_{L(pu)}{}^3(t_0)}{V_{DC1(pu)}}\right] + \left[\frac{i_{L(pu)}{}^3(t_2) - i_{L(pu)}{}^3(t_1)}{V_{DC1(pu)} - nV_{DC2(pu)}}\right] + \left[\frac{i_{L(pu)}{}^3(t_3) - i_{L(pu)}{}^3(t_2)}{V_{DC1(pu)}}\right] \right\} \right] \right) \right)^{1/2} \tag{58}$$

The next step involves, implementation of the algorithm, which is described through a flow chart diagram of Figure 0 and can be summarised as follows,

- The algorithm determines mode(s) that meet the required reference output power ($P_{ref(pu)}$).
- Once the correct mode(s) is/are computed, the algorithm responds by calculating key metrics such active and reactive power values for each mode(s).
- By using set of nested for loops, minimum reactive power search is performed, considering of all possible modes and results are listed.
- From this list, the mode that generates minimum reactive power is selected.
- Finally, the algorithm generates respective values of D_1, D_2 & D_3 for the optimum mode (D_{1opt}, D_{2opt} & D_{3opt}).

The algorithm can be extended to include applications that involve variable input and output DC link voltages. Instead of assuming fixed DC link voltages, it can be updated to also include $V_{DC1(pu)}$ and $nV_{DC2(pu)}$ as an input parameter in addition to $P_{ref(pu)}$.

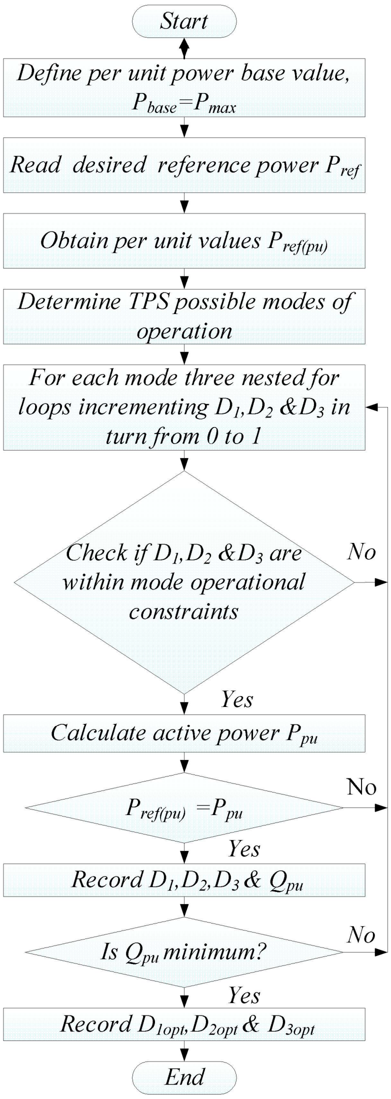

Figure 10. Flow chart of the TPS iterative optimization algorithm.

5. Results

In this section simulation and experimental verification are presented. To differentiate from the transformer voltage conversion ratio, an effective method is to perform analysis across the whole conversion ratio and power levels for each conversion ratio i.e,

$$R_V = \frac{nV_{DC2}}{V_{DC1}} \tag{59}$$

Therefore, considering converter operating range of 0 *pu* to 1 *pu* reference powers and for R_V=2, that is illustrated in Table 5, the advantages using triple phase shift algorithm to minimize the converter losses is evident. In the example of R_v=2, for partial power operation *of* p_{ref}*=0.5 pu and* p_{ref}*=0.25 pu.* This test shows modes that can meet the reference power, possible minimum reactive power for each mode and corresponding TPS values. Note that, each mode that can achieve the reference power output, the resulting reactive power is the minimum possible within

Table 5. TPS Mode selection performance of the algorithm for R_V=2 at pref=0.25 *pu* and pref=0.5 *pu*.

P_{ref}= 0.5 pu

Mode	*1*	*1′*	*2*	*2′*	*3*	*4*	*5*	*6*
$P_{ref}(pu)$	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Q(pu)	0.5771	2.8865	3.7519	1.4425	1.1430	1.1430	0.5771	0.5771
D_1	1.0000	1.0000	0.5000	0.5000	0.5000	0.5000	1.0000	1.0000
D_2	0.5000	0.5000	1.0000	1.0000	0.5000	0.5000	0.5000	0.5000
D_3	0.5000	-1.0000	0.5000	0.0000	0.5000	0.5000	0.5000	0.5000

P_{ref}= 0.25 *pu*

Mode	*1*	*1′*	*2*	*2′*	*3*	*4*	*5*	*6*
$P_{ref}(pu)$	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
Q(pu)	0.3423	1.5043	2.5335	0.8659	0.6123	0.8355	0.2990	0.6318
D_1	0.7500	0.7500	0.2500	0.5000	0.5000	0.6600	0.6700	0.9800
D_2	0.5000	0.2500	0.7500	0.7500	0.2500	0.1900	0.3300	0.9000
D_3	0.2500	-1.0000	0.5000	0.000	0.5000	0.8300	0.3600	0.1100

that mode, irrespective of its magnitude. During partial loading of 0.5 *pu* and 0.25 *pu*, eight different modes achieve the active power requirement as depicted in Table 5. Taking the case of $P_{ref(pu)}$= 0.5 *pu*, a minimum reactive power (Q_{min}) flow of 0.57 *pu* for modes *1, 5 and 6* is generated, while modes 2 outputs the maximum reactive power (Q_{max}) loss of 3.75 *pu;* a difference of 3.18 *pu* for the same active power requirement. The corresponding optimum TPS values leading to Q_{min} are, D_{1opt}=1, D_{2opt} =0.5 and D_{3opt} =0.5. This is EPS modulation scheme discussed in section 2 and further shows the importance of the TPS in generalising all known phase shift control schemes.

Similarly, at partial loading of $P_{ref(pu)}$=0.25 *pu*, the advantages of the TPS algorithm is even more noticeable for R_v=2. Q_{min} output of mode 5 is 1.16 *pu*, whilst mode 2, leads to a Q_{max}=3.75 *pu*, a difference of 4.74 *pu*. Therefore, these minimum reactive power values are the optimum which the controller selects for D_{1opt} =1, $D_{2\ opt}$ =0.5 and D_{3opt} =0.5. Table 6 presents the response of the algorithm when R_V ratio is further increased to 4. Using the same reference power of 0.5 *pu* and 0.25 *pu*, as in previous case, eight different modes operate at the required active power. When 0.5 *pu* is required, mode 6 generates a Q_{min} of 1.16 *pu*, while mode 2 leads to a corresponding, Q_{max} of 5.92 *pu*. Reducing $P_{ref\ (pu)}$ to 0.25 *pu*, a Q_{min} of 0.51 *pu* and Q_{max} of 4.31 *pu* is generated by modes 5 and 2. The optimum TPS parameters that lead to minimum reactive power when P_{ref}= 0.5 *pu* are, D_{1opt} =0.85, $D_{2\ opt}$ =0.40 and D_{3opt} =0.55. While for P_{ref}= 0.25 *pu*, D_{1opt} =0.81, $D_{2\ opt}$ =0.19 and D_{3opt} =0.64. Again, as with these two cases, the algorithm as expected was capable to determine and select Q_{min}.

Table 6. TPS Mode selection performance of the algorithm for R_V=4 at p_{ref}=0.25 *pu* and p_{ref}=0.5 *pu*.

P_{ref}= 0.5 *pu*

Mode	*1*	*1′*	*2*	*2′*	*3*	*4*	*5*	*6*
$P_{ref}(pu)$	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Q(pu)	1.4425	3.7519	5.9160	3.6066	2.4528	2.1802	1.2941	1.1579

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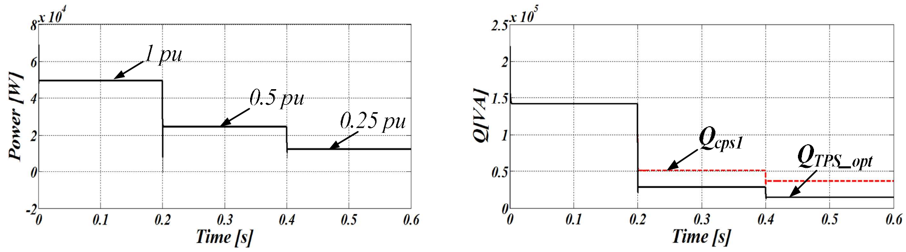
D_1	1.0000	1.0000	0.5000	0.5000	0.5000	0.6500	0.8500	0.9800
D_2	0.5000	0.5000	1.0000	1.0000	0.5000	0.4000	0.4000	0.3600
D_3	0.5000	-1.0000	0.5000	0.0000	0.5000	0.7000	0.5500	0.6600

P_{ref}= 0.25 pu

Mode	1	1′	2	2′	3	4	5	6
P_{ref}(pu)	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
Q(pu)	0 .5556	1.7335	4.3103	2.5582	0.9182	0.8208	0.5074	0.5579
D_1	0.7500	0.7500	0.2500	0.5000	0.5000	0.8500	0.8100	0.9800
D_2	0.2500	0.2500	0.7500	0.7500	0.2500	0.1500	0.1900	0.1400
D_3	0.5000	-1.000	0.5000	0.000	0.5000	0.9000	0.6400	0.8700

To further validate the importance of TPS algorithm, a 100 kW, 1kV/4kV converter is simulated using Matlab/Simulink using 2 kHz switching frequency and L_{tot} of 0.62 *mH* for HVDC application. Simulation results of Figure 11 and Figure 12, highlight effect of operating the converter at non-unity R_V. The results of Figure 11 illustrate the converter operating at R_V ratio of 2. Figure 11 (a) depicts the corresponding active power output 1.0 *pu* from time *t=0 to t= 0.2s, 0.5 pu* from *t=0.2s* to *t=0.4s* and *0.25 pu* from *t=0.4s* to *t=0.6s*. The superimposed reactive power plots of the TPS algorithm and conventional phase shift (CPS) is displayed in Figure 11 (b). As in previous case, regardless of the voltage conversion ratio, at 1.0 *pu* output power, the reactive power is uncontrollable. But however, observe the significant difference of reactive power at low power levels of 0.5 *pu* and 0.25 *pu,* where DAB converter losses are significant. For 0.5 *pu,* between *t=0.2s* to *t=0.4s,* the dash red line represents a reactive power value of *Q=1.05 pu*, while, for the TPS optimisation algorithm shown by the solid black line, *Q=0.56 pu*. This is a significant improvement, which will translate to conduction and copper losses reduction.

Similarly, for output power of 0.25 *pu*, the reactive power loss gap widens further between CPS and proposed control scheme, a difference of *Q*=0.44 *pu*. Figure 11 parts (c) to (f) depict the transformer AC voltages and currents at 2 kHz. Waveforms of Figure 11 parts (c) to (d) show AC voltages TPS and under CPS. In Figure 11 (c), v_{ac1} and v_{ac2}, waveforms are full square waves, for all



(a) (b)

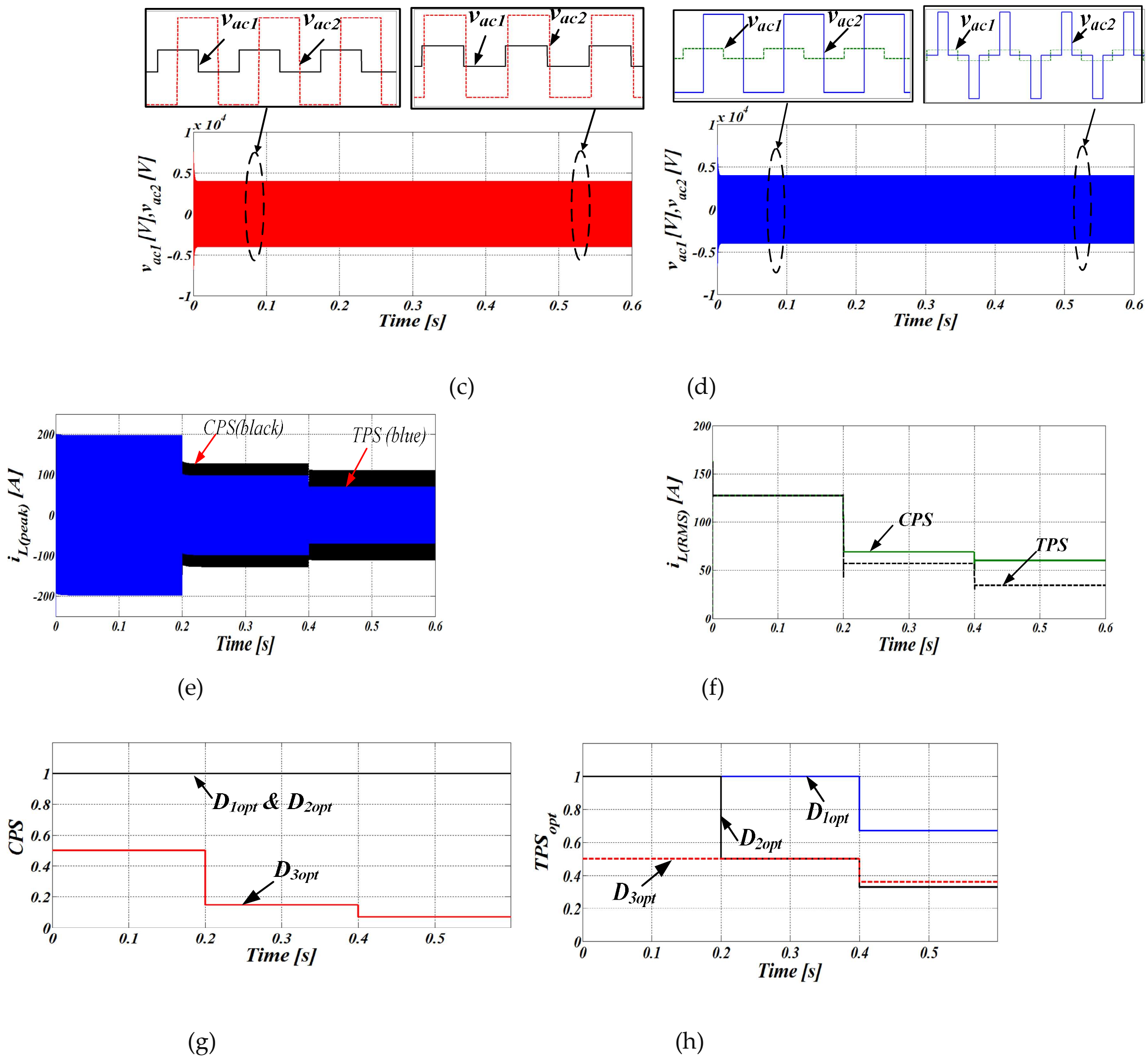


Figure 11. Simulation results for Rv=2 (a) active power (b) reactive power, (c) CPS AC voltage waveforms for bridges A and B, (d) TPS AC voltage waveforms (e) Peak inductor currents, (f) RMS currents, (g) CPS control variable (h) optimum TPS control variables.

power levels, and the corresponding D_1, D_2 and D_3 values are shown in Figure 11 (g). In Figure 11 (d), the quasi square wave pattern for low power level of 0.5 *pu* and 0.25 *pu* respectively can be seen. The TPS control parameters, that leads to this low reactive power is depicted by Figure 11 (g). Peak and RMS inductor currents, waveforms are shown in Figure 11 parts (e) and (f). During low power transmission of 0.5 *pu* and 0.25 *pu* the improvement of the switching algorithm over CPS scheme can be seen.

Experimental test rig of a down scaled 568W 24V/100V DAB converter prototype, was also performed to show the TPS algorithm response under wide Rv. The converter parameters are indicated in Table 7 and the circuit layout, including a photo of the test rig, are shown in Figure 4.12. The entire TPS controller was implemented using Texas instruments TMS320F2335 Microcontroller mounted on eZDSP evaluation board. Several test setups are performed that include the following:

Table 7. Converter Parameters.

Input DC voltage	V_{DC1}	*24 V*
Output DC voltage	V_{DC2}	*100 V*

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Total inductance	L_{tot}	*63.36 uH*
Switching frequency	f_s	*2 kHz*
Transformer turns ratio	n	*100/24*
Input DC capacitor	C_{DC1}	*1200 µF*
Output DC capacitor	C_{DC2}	*2700 µF*

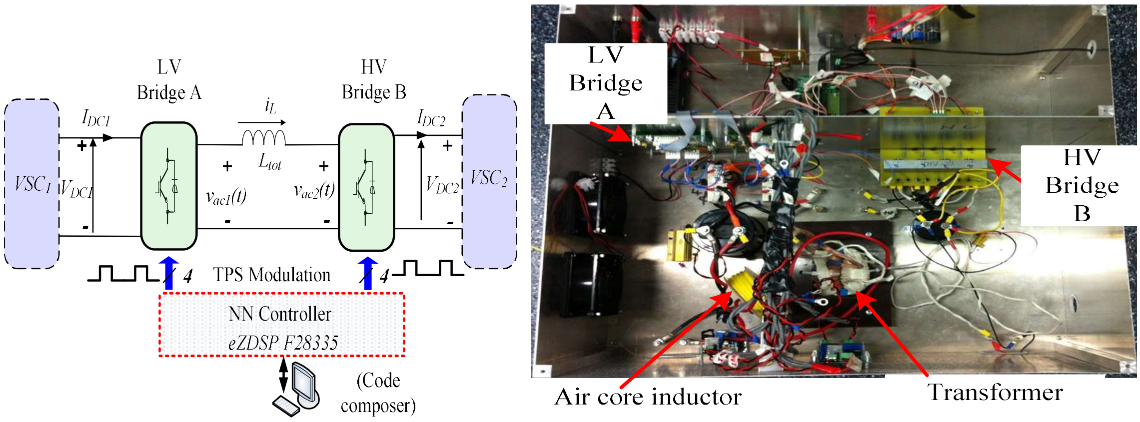

Figure 12. (a) Block diagram of test system (b) Test set up.

The hardware test sub-systems consist of the following,

- Low (LV) bridge and high voltage (HV) bridge single phase dual active converter bridges which are implemented using four active insulated gate bipolar transistor (IGBT) switches, with associated gate driver circuits for galvanic isolation between the switches common points and microcontroller common ground.
- Texas instruments F28335 Microcontroller.
- 2 kHz nano-crystalline core transformer and external air core inductor.
- DC filters capacitors.
- DC power supplies powering sensor circuits, gate drivers, microcontroller, and cooling fans.

This test is designed to study the response of the TPS contoller when the converter is required to source/sink while operating at full/partial loading scenarios at R_V=1. Results of Figure 13 (a) shows when the converter is operating at full rated power of -1 *pu* (power flow from HV Bridge B to LV Bridge A) initially. Before power reversal is performed, bridge B is sourcing while bridge A is sinking, which is evident from the DC currents I_{DC1}, I_{DC2} directions and the full square waveforms of the transformer AC voltages v_{ac1} and v_{ac2} at *2 kHz*. After short duration, a full power reversal of *1 pu* is commanded. Observe that, the directions of the DC currents reverse fast as expected with virtually no noticeable transient's overshoot. Similarly, the full square wave transformer ac voltages v_{ac1} and v_{ac2} phase shift reversal can be seen, where v_{ac1} now leads v_{ac2} by 90^0. The inductor current i_L,

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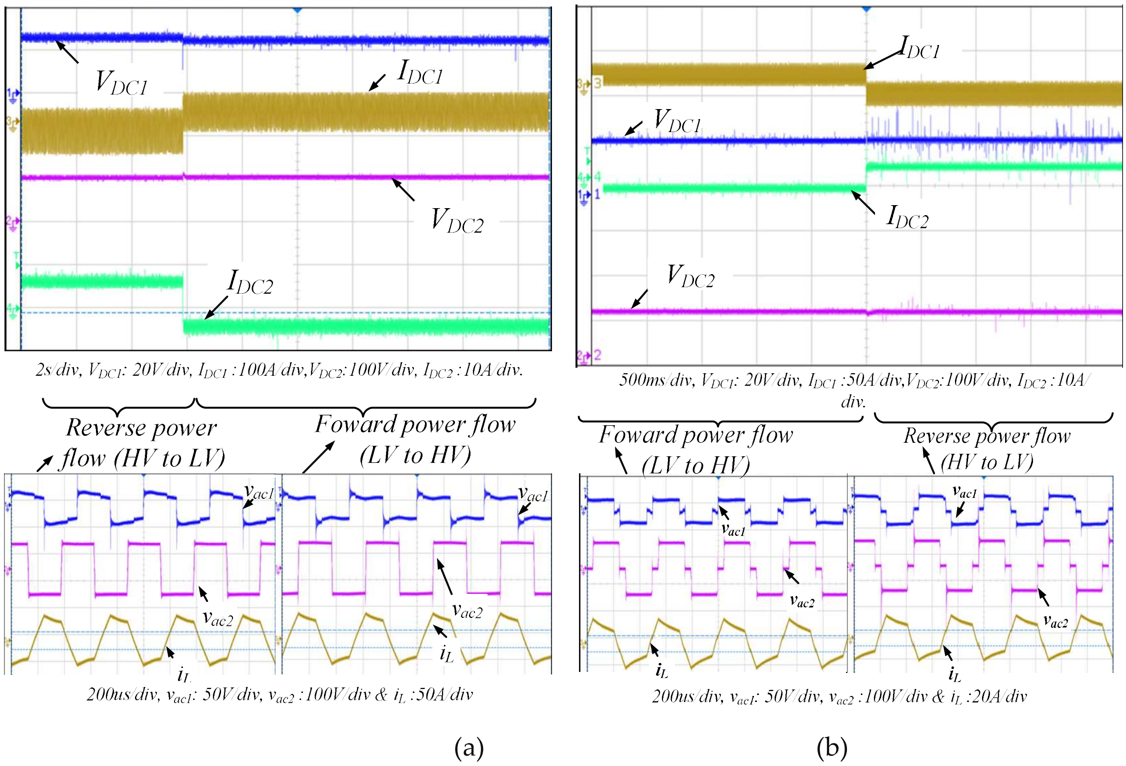

Figure 13. Measured voltage and current waveforms showing power reversal capability TPS algorithm.

to the TPS controller. The quasi-square wave ac voltages at ±0.5 *pu* active power are illustrated at the bottom of the Figure 13(b).

direction change is also illustrated in the figure. In Figure 13 (b), the algorithm response to ±0.5 pu partial power operation is also demonstrated. A fast partial power reversal of 0.5 *pu* to -0.5 *pu* , is achieved.

Similarly, to validate the algorithm in terms of selecting minimum reactive power flow, out of all possible modes for active power reference of *0.5 p.u* and *0.25 pu* , individual test was further performed, at voltage conversion ratio of *Rv*=2. Figure 14 shows post processed results representing clusters of bar graphs of the modes reactive power and efficiency for partial power levels of *0.5 p.u* and *0.25 p.u* respectively. The corresponding practical AC and DC waveforms of the results of Figure 14 (a) is presented in Figure 15.

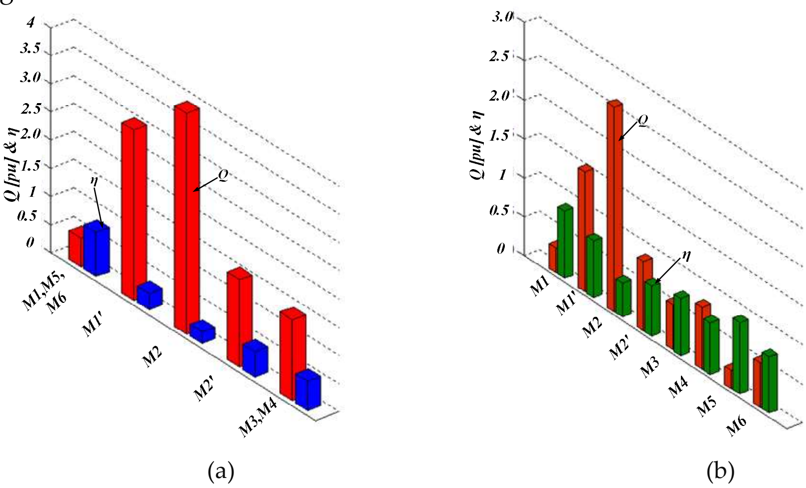

Figure 14. Experimental values of reactive power and efficiency for active power operations of (a) 0.5 *pu* (b) 0.25 *pu* when R_v=2.

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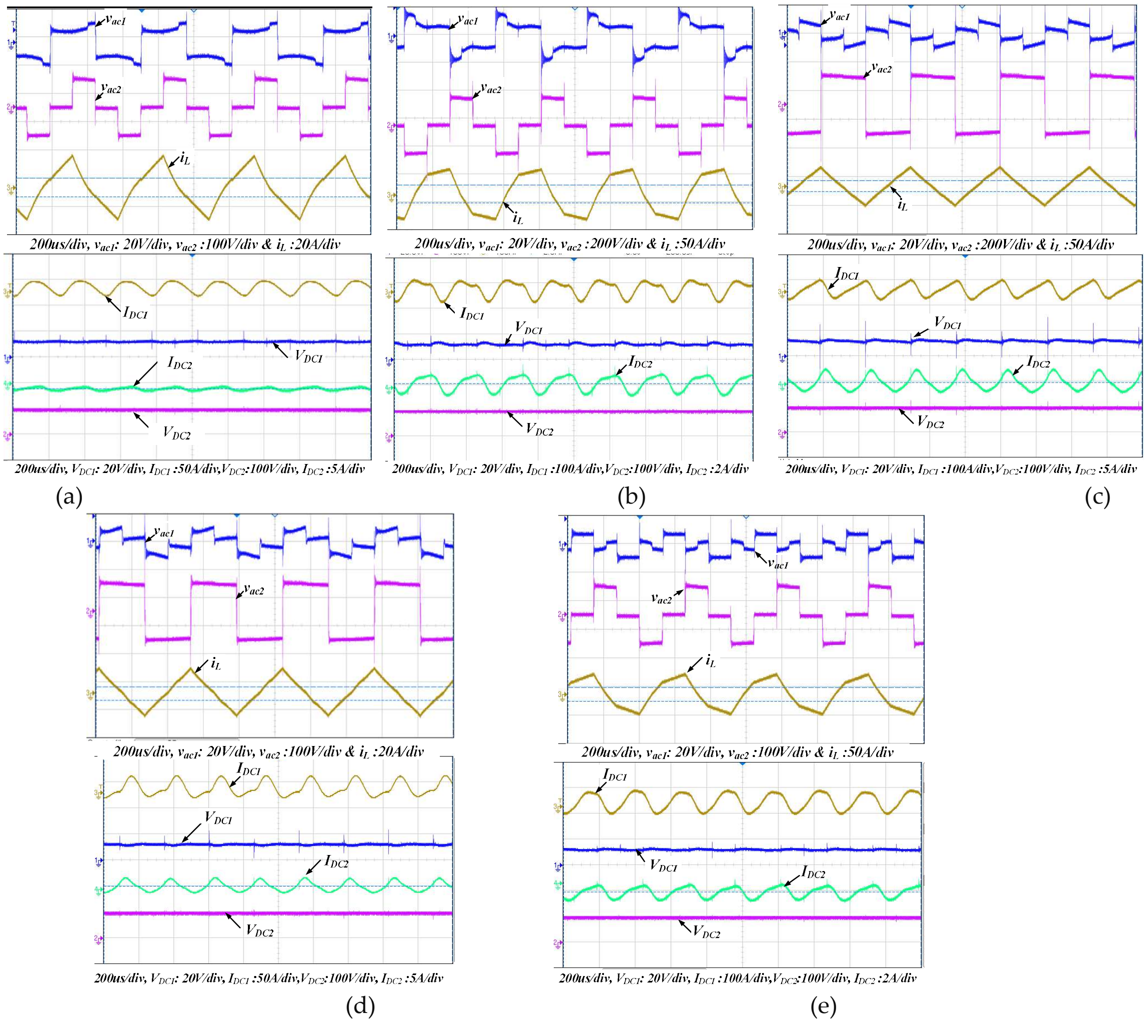

Figure 15. 0.5 *pu* measured AC and DC waveforms for optimum mode selection when R_v=2 (a) Modes 1,5 and 6 (b) Mode 1′ (c) Mode 2 (d) Mode 2′ (e) Modes 3 and 4.

This agrees with the result of Table 5, whereby modes M1, M2, M2′, M3, M4, M5 and M6 were able to transmit the required active power. Similarly, performance of the algorithm was further evaluated at low output power level of *0.25 pu* as demonstrated in Figure 4.14 (b). According to Table 5, Modes M1, M2, M2′, M3, M4, M5 and M6 were able to transmit the required active power *0.25 pu*. M5 is the most efficient mode, with Q_{min}=0.23 *pu*, while the M2 is the worst with corresponding reactive power circulation of Q_{min}=2.63 *pu*, a significant difference of 2.4 *pu* (680 Var). Typical oscilloscope waveforms recorded for the least and the most efficient mode M2 and M5 is illustrated by Figure 16 parts (a) and (b).

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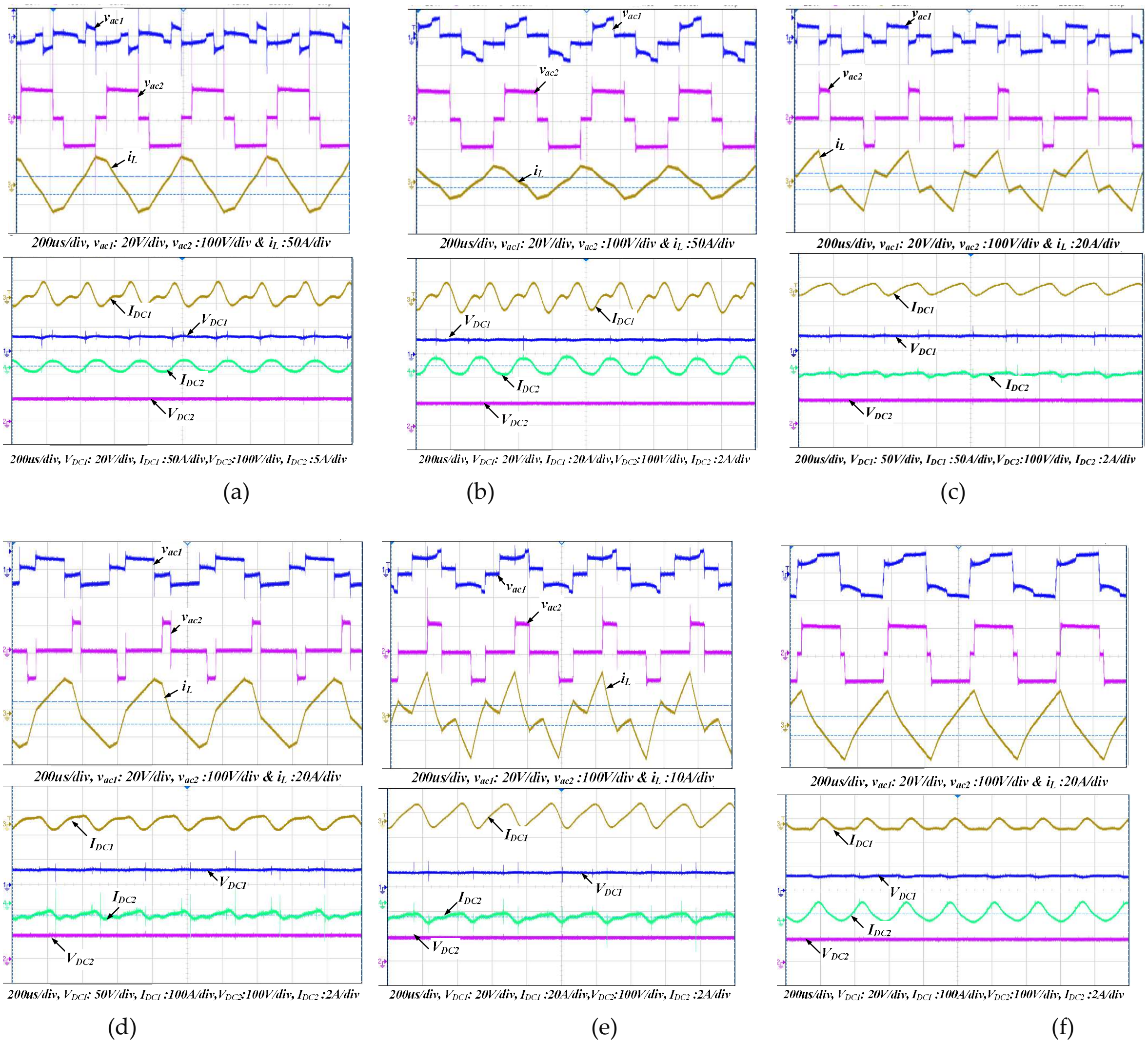


Figure 16. 0.25 *pu* reference power, AC and DC waveforms when R_v=2 (a) Mode 1 (b) Mode 1′ (c) Mode 2 (d) Mode 2′ (e) Modes 3 (f) Mode 4 (g) Mode 5 (h) Mode 6.

6. Conclusions

A steady state analysis of single-phase DAB converter using TPS was presented in this paper. It has been shown that Single phase shift, Extended phase shift and Dual phase shift modulation schemes are special cases of triple phase shift (TPS) modulation control. Six switching modes and their complements for reverse power flow have been identified using TPS control. Rather than using fundamental component approximation to determine average power transmitted, detailed analytical investigation was performed on all the switching modes. Moreover, based on the mode operating constraint, the power transfer range for each mode was derived. Inductor current which is crucial in the determination of DAB performances indices was calculated for all the modes at each time intervals. In complementary modes, bridge 2 waveform is shifted by 180^0 from original mode, hence resulting in equal but negative power transfer. From the analysis, it was observed that modes 6 and 6′ are the only modes that cover the whole converter operating power range. Modes 1, 1′, 2 and 2′are capable of charging and discharging operation, but only for half the power range. Modes 3, 4, 5 and 6 with their complements only provide unidirectional power transfer capability each. Finally, it is worth noting that, in mode 3 and 3′ power transfer is independent of D_3, meaning that it can be solely controlled by controlling bridge voltages. In addition, this article has shown that the presented TPS analysis can be generalized to include all phase shift modulation techniques such as CPS, EPS and DPS.

Contrary to recently reported in literature, this manuscript has simplified TPS modulation scheme and thus with the intent to standardize all known modulation schemes for single phase shift DAB converter. a novel generic per unit reactive power optimization algorithm based TPS modulation. The algorithm iteratively searched for TPS control variables D_{1opt}, D_{2opt} and D_{3opt} which satisfied desired active power, while selecting the mode with minimum reactive power flow. The algorithm robustness was verified analytically, through MATLAB/Simulink simulations and experimentally.

Author Contributions: Conceptualization, Y.H.; methodology, Y.H; software, Y.H.; validation, H.M and A.A.; formal analysis, Y.H.; investigation, Y.H; resources, H.M; data curation, A.A.; writing—original draft preparation, Y.H.; writing—review and editing, H.M. and AA.; visualization, Y.H. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Data is unavailable.

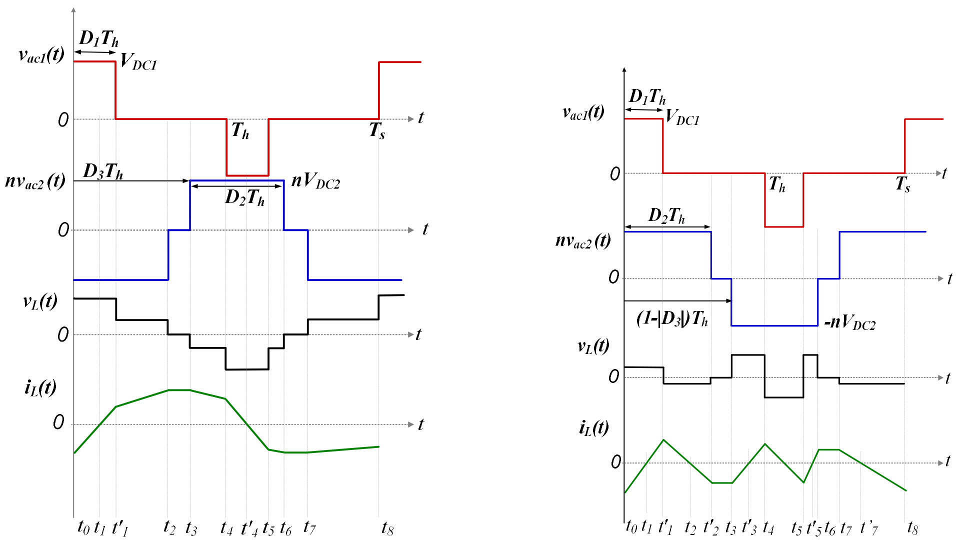
Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

A1: Remaining TPS modes of operation 2 to 6 including its complements.

a) **Modes 2 and 2′**

The voltage/current waveforms for these modes of operation are depicted in Figure 3.7. Mode 2, operational waveforms portrayed in Figure 3.2 (a) is characterised by full overlap of positive and negative transformer voltages. Similarly, for mode 2′, full overlap v_{ac1} and v_{ac2} of both voltage waveforms feature distinguishes the mode as Figure 3.7 (b) demonstrates. In addition, the inductor current (i_L) at each instantaneous current interval and average input/output current are also indicated.



(a) (b)

Figure A.1. Ideal steady state transformer voltages/inductor current (a) Mode 2 (b) Mode 2′.

i. Mode 2

Mode boundary is determined by ensuring full overlap of positive v_{ac1} and negative v_{ac2} transformer voltages. Through, observation of voltage waveform features of Figure A.1 (a), the following constraint is defined for the mode.

$$D_2 \geq D_1$$
$$1 + D_1 - D_2 \leq D_3 \leq 1 \tag{A.1}$$

Analysis of various switching instant of the inductor current, during first half switching cycle is explained below.

Interval ***t_0 - t_1:*** During this sequence, the initial inductor current is negative; hence, the current flows through reverse recovery diodes D_{S1} and D_{S4}, for bridge A. While in bridge B anti-parallel diodes D_{Q2} and D_{Q3}, carry the current. Figure A.2 (a) shows the resulting equivalent circuit. The inductor voltage can be expressed as, $V_{DC1}+nV_{DC2}$. Therefore, i_L, is

$$i_L(t) = \frac{V_{DC1} + nV_{DC2}}{L_{tot}}(t - t_0) + i_L(t_0) \tag{A.2}$$

Interval ***t_1 - t_1':*** The current polarity reverses during this segment and the equivalent circuit of Figure A.2 (b) demonstrates the new current path. In bridge A, switches S_1 and S_4 start to conduct, whilst in bridge B the current flows through switches Q_2 and Q_3 respectively. The instantaneous inductor current for this sub-period remains unchanged. Thereby, the inductor voltage also remains coupled at $V_{DC1}+nV_{DC2}$ value.

Interval ***t_1'- t_2:*** Current continues to increase steadily and flows in the direction shown by the equivalent circuit diagram of Figure A.2 (c). It flows through D_{S2} and S_4, of primary bridge A, while for bridge B, Q_2 and Q_3 are still conducting. The voltage impressed across the inductor is nV_{DC2} and the thus, inductor current can be deduced by

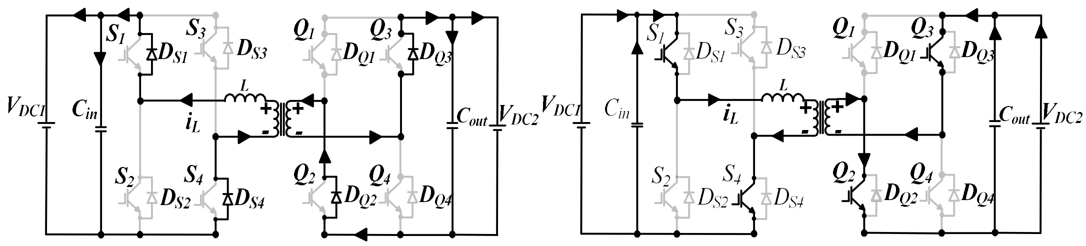
$$i_L(t) = \frac{nV_{DC2}}{L_{tot}}(t - t_1) + i_L(t_1) \tag{A.3}$$

Interval ***t_2 – t_3:*** The time sequence begins upon switch Q_2 turn off. Both AC transformer voltages are zero and hence, the voltage across the inductor equates to zero. The current continues to freewheel in D_{S2} and through S_4, in bridge A, while in bridge B, D_{Q1} and Q_3, conduct the current as portrayed in Figure A.2 (d). The current is retained at same level as in previous interval.

Interval ***t_3 – t_4:*** Figure A.2 (e), shows the schematic diagram demonstrating the current path during this sub-period that completes one half cycle. In bridge A, the current continues in similar path as in previous interval for bridge A. For bridge B, current flows through D_{Q1} and D_{Q4}. The voltage across the inductor is $-nV_{DC2}$. The inductor current is expressed as,

$$i_L(t) = -\frac{nV_{DC2}}{L_{tot}}(t - t_3) + i_L(t_3) \tag{A.4}$$

According to Figure A.1 (a), t_n values are determined by assuming $t_0=0$, then $t_1= D_1T_h$, $t_2=(D_2+D_3-1)T_h$, $t_3=D_3T_h$ and $t_4=T_h$,. By therefore inserting t_n values in expressions (A.2) to (A.4) respectively, the inductor current at various switching interval that facilitate the derivation of key performance indicators for mode 2, which is computed and listed in Table 3.2. According to derivations in Table 3.2, the peak current is achieved by $i_L(t_3)$. The result obtained for the mode per unit power range is ±0.5 *pu*, which is similar to previous two modes and the TPS modulation parameters that result in these limits are given. Finally, mode can operate the converter switching devices under soft switching if the ZVS limits outlined at the bottom of Table 3.2 are adhered to.



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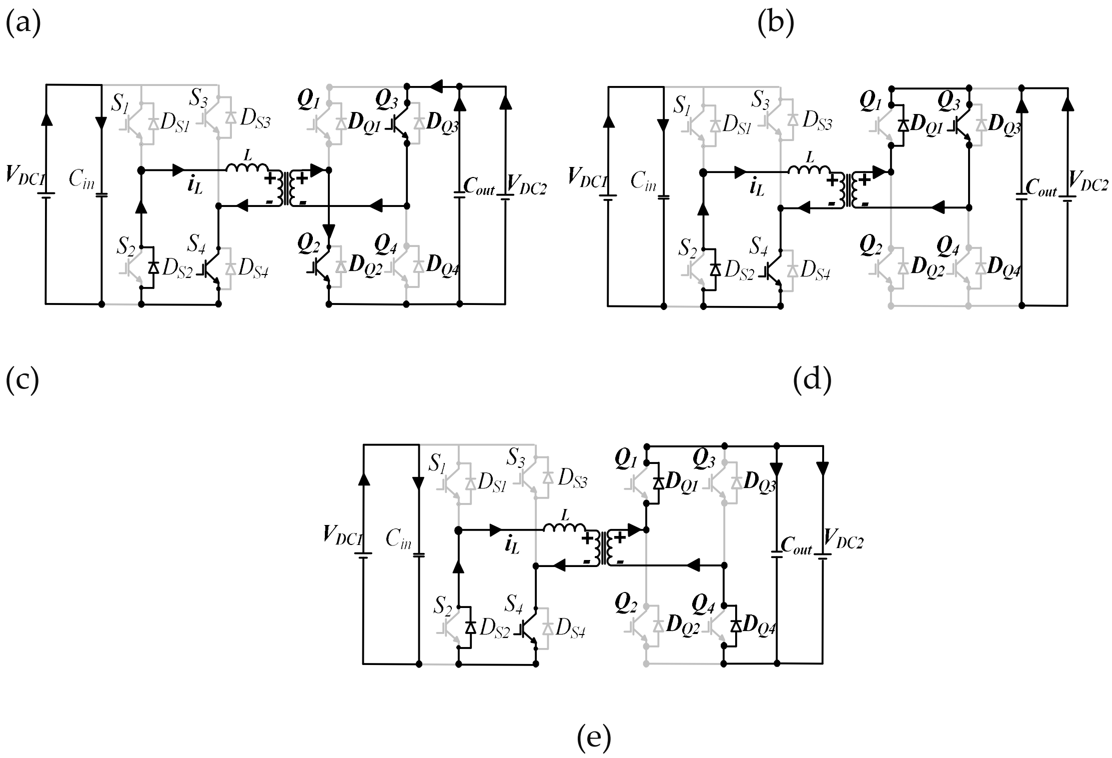

Figure A.2. Mode 2 detailed equivalent circuit diagrams (a) t_0-t_1 (b) t_1-t'_1(c) t'_1 -t_2 (d) t_2- t_3 (e) t_3- t_4. .

ii. Mode 2′

To visualise complimentary mode 2′ boundaries, its paramount that overlap of negative v_{ac1} and positive v_{ac2} transformer voltages are maintained throughout as Figure A.1 (b) demonstrates. Following similar procedure as in complimentary mode 1′ and by extending waveforms of Figure A.1 (b) to the negative half plane, the following mode boundary is derived.

$$\begin{aligned} &D_2 \geq D_1 \\ &D_1 - D_2 \leq D_3 \leq 0 \end{aligned} \tag{A.5}$$

Evaluation of steady state inductor current for the first half switching cycle is performed as follows.

Interval t_0 - t_1: This switching duration is illustrated by equivalent circuit diagram of Figure A.3 (a). At t_0, the inductor current is freewheeling through diode D_{S1} and D_{S4} in H-bridge A. Switches, Q_1 and Q_4 of H-bridge B, conduct. The voltage impressed across L_{tot}, is V_{DC1}-nV_{DC2}. Current i_L which continues to increment is given by

Table A.1. Mode 2 derivations.

Variable	
Currents at each switching instants	$i_L(t_0) = -\left[\dfrac{V_{DC1}D_1 + nV_{DC2}D_2 - 2nV_{DC2} + 2nV_{DC2}D_3}{4f_sL_{tot}}\right]$
	$i_L(t_1) = \left[\dfrac{V_1 D_{DC1} + 2nV_{DC2}D_1 - nV_{DC2}D_2 + 2nV_{DC2} - 2nV_{DC2}D_3}{4f_sL_{tot}}\right]$

	$i_L(t_2)=\left[\dfrac{V_{DC1}D_1+nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_3)=i_L(t_2)$
	$i_L(t_4)=\left[\dfrac{V_{DC1}D_1+nV_{DC2}D_2-2nV_{DC2}+2nV_{DC2}D_3}{4f_sL_{tot}}\right]$
RMS current	$I_{rms(\mathrm{mode}2)}=\left(\left[i_L^2(t_2)(1-D_2)\right]+\left[\dfrac{2f_sL_{tot}}{3}\left\{\left[\dfrac{i_L^3(t_1)-i_L^3(t_0)}{V_{DC1}+nV_{DC2}}\right]+\left[\dfrac{i_L^3(t_2)-i_L^3(t_1)}{nV_{DC2}}\right]+\left[\dfrac{i_L^3(t_0)+i_L^3(t_3)}{nV_{DC2}}\right]\right\}\right]\right)^{1/2}$
RMS voltage	$V_{Lrms(\mathrm{mode}2)}=\left(V_{DC1}^2D_1+\left(nV_{DC2}\right)^2D_2+2nV_{DC1}V_{DC2}D_1\right)^{1/2}$
Average power & range	$P_{(\mathrm{mode}2)}=-\dfrac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}\left[D_1^2-D_1D_2+2D_1-2D_1D_3\right]$ ***Range:*** ➡ $\begin{cases}P_{\max}=0.5pu & (D_1=0.5,D_2=1,D_3=0.5)\\ P_{\min}=-0.5pu & (D_1=0.5,D_2=1,D_3=1)\end{cases}$
Reactive power	$Q_{\mathrm{mode}2}=v_{rms(\mathrm{mode}2)}\times i_{rms(\mathrm{mode}2)}$
ZVS	*Achievable for all switches* ***Constraints:*** $i_L(t_0)<0, i_L(t_1)>0 \& i_L(t_2)>0$

N

$$i_L(t)=\frac{V_{DC1}-nV_{DC2}}{L_{tot}}(t-t_0)+i_L(t_0) \tag{A.6}$$

Interval t_1 - t_1': The current during this segment changes polarity and the path it flows through is depicted in Figure A.3 (b). As can be seen, for the bridge A, switches S_1 and S_4 are turned on, whilst reverse recovery diodes D_{Q1} and D_{Q4}, of bridge-B carry the current. The inductor voltage is clamped at $V_{DC1}+nV_{DC2}$ and the instantaneous current transferred at this segment remains unchanged.

Interval t_1'- t_2: Figure A.3 (c) shows the equivalent circuit for this sub-period. In bridge A, the current flows through D_{S2} and S_4, while for bridge B anti-parallel diodes D_{Q1} and D_{Q4} conduct. The inductor voltage during this duration is $-nV_{DC2}$ and the current can be expressed as,

$$i_L(t)=\frac{nV_{DC2}}{L_{tot}}(t-t_1)+i_L(t_1) \tag{A.7}$$

Interval t_2 - t'_2: During this time instant shown by Figure A.3 (d), the inductor changes from positive to negative, its D_{S2} and S_4 of primary bridge A and D_{Q1} and Q_3 of bridge B that conduct current respectively. The voltage impressed across the inductor remains at $-nV_{DC2}$ and thus, the current is,

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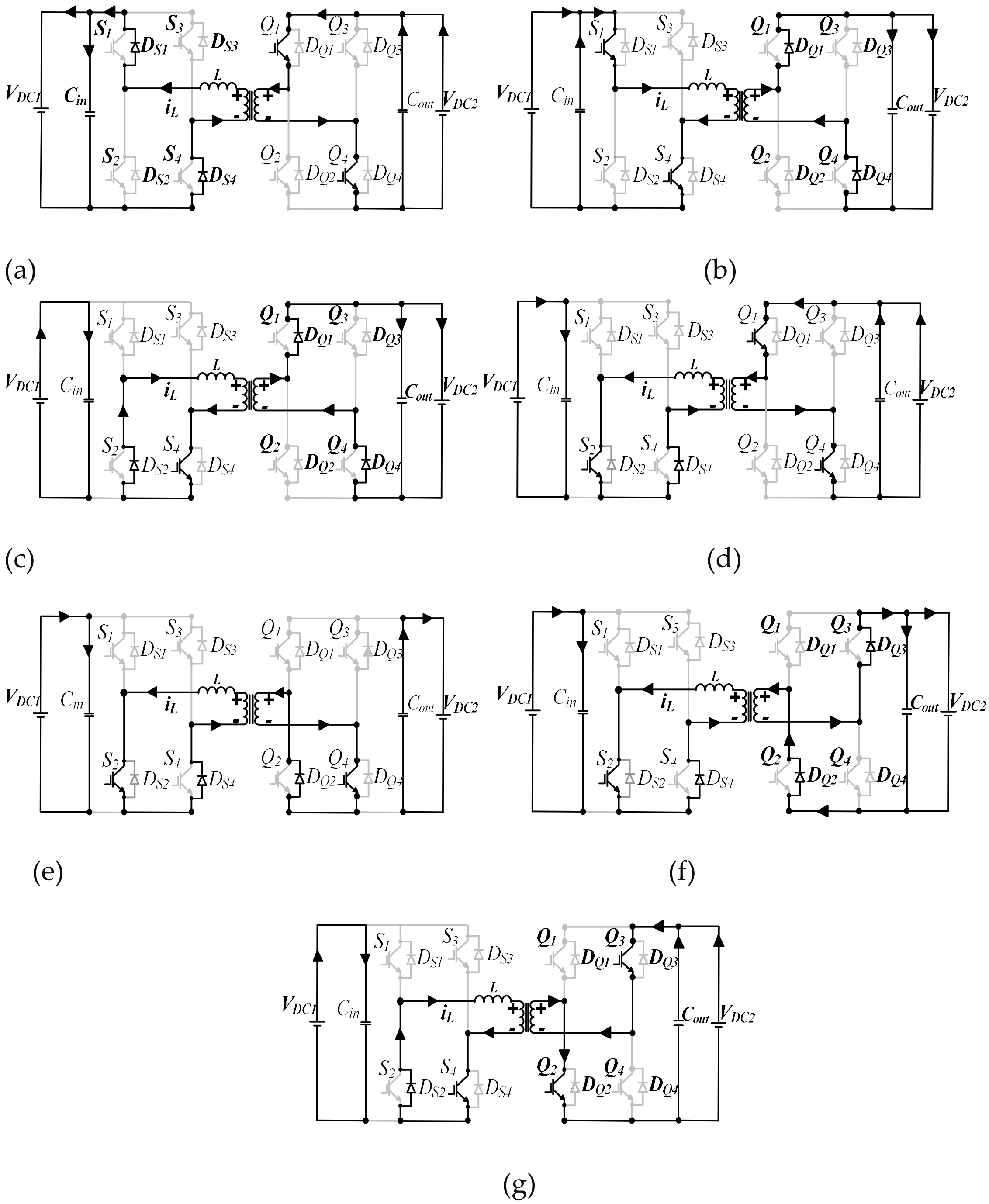

Figure A.3. Equivalent schematic diagram of Mode 2′ (a) t_0-t_1 (b) t_1-t'_1 (c) t'_1-t_2 (d) t_2- t'_2 (e) t'_2 -t_3 (f) t'_3 -t_3 (g) t_3 –t_4.

$$i_L(t) = -\frac{nV_{DC2}}{L_{tot}}(t-t_2) + i_L(t_2) \tag{A.8}$$

Interval t'_2- t_3: The current is same as in expression (A.8), with zero gradients as shown by Figure A.1 (b). The equivalent circuit diagram of Figure A.3 (e), shows that D_{S2} and S_4 continue to conduct the current for bridge A and it is the freewheeling diode D_{Q2} and power switch Q_4 that the current flows through for H-bridge B. The inductor voltage is zero during this time sequence.

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Interval t_3 - t'_3: Inductor current increases linearly and the voltage across the inductor is nV_{DC2}. For bridge A, S_2 and D_{S4} conduct, while in bridge B the current freewheels in D_{Q2} and D_{Q3} as depicted in Figure A.3 (f). The inductor voltage is nV_{DC2}, which causes the current to increment gradually.

$$i_L(t)=\frac{nV_{DC2}}{L_{tot}}(t-t_3)+i_L(t_3) \tag{A.9}$$

Interval t'_3- t_4: At t'_3, the current change polarity. D_{S2} and S_4 are conducting in bridge A, while Q_2 and Q_3 are turned on. Current magnitude and inductor voltage are retained at same value as previous in previous switching instant. This is displayed in Figure A.3 (g).

Therefore, from equations (A.6) to (A.9), the instantaneous inductor current at each switching interval, can be determined by assuming $t_0=0$, $t_1= D_1T_{h,}$, $t_2=(D_2-|D_3|)T_h$, $t_3=(1-|D_3|)T_{h,}$, $t_4=T_{h,}$. These expressions are listed in Table A.2, together with the derivation of other important mode parameters. The maximum current is given by $|i_L(t_4)|$ and the resulting power range for this complimentary mode is also evaluated to be ±0.5 *pu*. Moreover, ZVS is achievable for all switches and the boundaries for soft switching are given by the inequalities tabulated.

Table A.2. Mode 2'steady state expressions.

Variable	
Currents at each switching instants	$i_L(t_0)=-\left[\frac{V_{DC1}D_1-nV_{DC2}D_2+2nV_{DC2}\lvert D_3\rvert}{4f_sL_{tot}}\right]$
	$i_L(t_1)=\left[\frac{V_{DC1}D_1-2nV_{DC2}D_1+nV_{DC2}D_2-2nV_{DC2}\lvert D_3\rvert}{4f_sL_{tot}}\right]$
	$i_L(t_2)=\left[\frac{V_{DC1}D_1-nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_3)=i_L(t_2)$
	$i_L(t_4)=\left[\frac{V_{DC1}D_1-nV_{DC2}D_2+2nV_{DC2}\lvert D_3\rvert}{4f_sL_{tot}}\right]$
RMS current	$I_{rms(mode2')}=\left(\left[i_L^2(t_2)(1-D_2)\right]+\left[\frac{2f_sL_{tot}}{3}\left\{\left[\frac{i_L^3(t_1)-i_L^3(t_0)}{V_{DC1}-nV_{DC2}}\right]-\left[\frac{i_L^3(t_2)-i_L^3(t_1)}{nV_{DC2}}\right]-\left[\frac{i_L^3(t_0)+i_L^3(t_3)}{nV_{DC2}}\right]\right\}\right]\right)^{1/2}$
RMS voltage	$V_{Lrms(mode2')}=\left(V_{DC1}^2D_1+(nV_{DC2})^2D_2-2nV_{DC1}V_{DC2}D_1\right)^{1/2}$
Average power & range	$P_{(mode2')}=-\frac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}\left[D_1^2-D_1D_2+2D_1\lvert D_3\rvert\right]$ *Range:* ➡ $\begin{cases}P_{max}=0.5pu & (D_1=0.5, D_2=1.0, D_3=-0.5)\\ P_{min}=-0.5pu & (D_1=0.5, D_2=1.0, D_3=0.0)\end{cases}$
Reactive power	$Q_{mode2'}=v_{rms(mode2)}\times i_{rms(mode2)}$

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ZVS	*Achievable for all switches* *Constraints:* $i_L(t_0)<0, i_L(t_1)>0 \,\&\, i_L(t_2)<0$

b) Modes 3 and 3′

Mode 3 converter waveforms which is shown in Figure A.4 (a), is characterised by non-overlapping primary and secondary transformer voltages (v_{ac1} and v_{ac2}). The corresponding voltage and inductor current waveforms for complimentary mode 3′ are indicated in Figure A.4 (b).

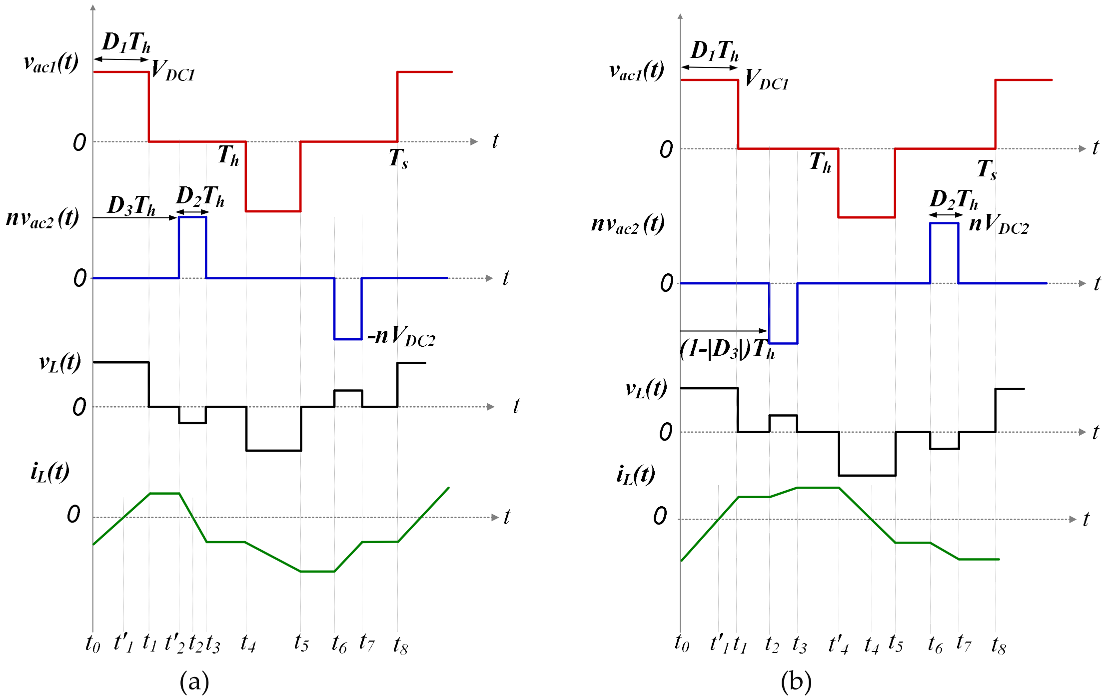

Figure A.4. Modes steady state voltages and current (a) Mode 3 (b) Mode 3′.

i. Mode 3

By following previous steps to determine mode constraint, inequalities defining the mode 3 boundary from the voltage sequence of Figure A.4 (a), is determined as

$$\begin{aligned} D_2 &\le 1 - D_1 \\ D_1 \le D_3 &\le 1 - D_2 \end{aligned} \tag{A.10}$$

Similarly, from Figure A.4 (a), the piecewise linear inductor current, during different sub-periods is determined over a half cycle as follows,

Interval t_0 **-** t'_1**:** Figure A.5 (a) shows the equivalent circuit. The inductor current is in negative, for bridge A , the current flows through reverse recovery diodes D_{S1} and D_{S4}. Q_1 and D_{Q3} of secondary Bridge-B provide path for the current. The voltage impressed across L_{tot} is V_{DC1}. Thus, i_L can be written as,

$$i_L(t) = \frac{V_{DC1}}{L_{tot}}(t - t_0) + i_L(t_0) \tag{A.11}$$

Interval t'_1 **-** t_1**:** At t'_1, the current changes polarity and becomes positive. Switches S_1 and S_4 of bridge A are turned on, while D_{Q1} and Q_3 of the secondary bridge-B are in the conduction path as shown in Figure A.5 (b). Inductor voltage during this interval is retained at V_{DC1} and the magnitude of inductor current remains unchanged, which is given by expression (A.11).

Interval t_1 **–** t'_2**:** During this segment both v_{ac1} and v_{ac2} AC voltages are zero. The i_L, remains at same value according to previous segment, while flowing through D_{S2}, S_4, D_{Q1} and Q_3 of both H-bridges respectively, as Figure A.5 (c) demonstrates.

Interval t'_2 **-** t_2**:** Figure A.5 (d) shows resulting circuit structure during this sequence. Anti-parallel diode D_{S2} and switch S_4 continue to conduct. For bridge B D_{Q1} and D_{Q4} begin to freewheel. The voltage impressed across the inductor is $-nV_{DC2}$. Therefore, the current through L_{tot} is

$$i_L(t) = -\frac{nV_{DC2}}{L_{tot}}(t - t_2) + i_L(t_2) \quad \text{(A.3)}$$

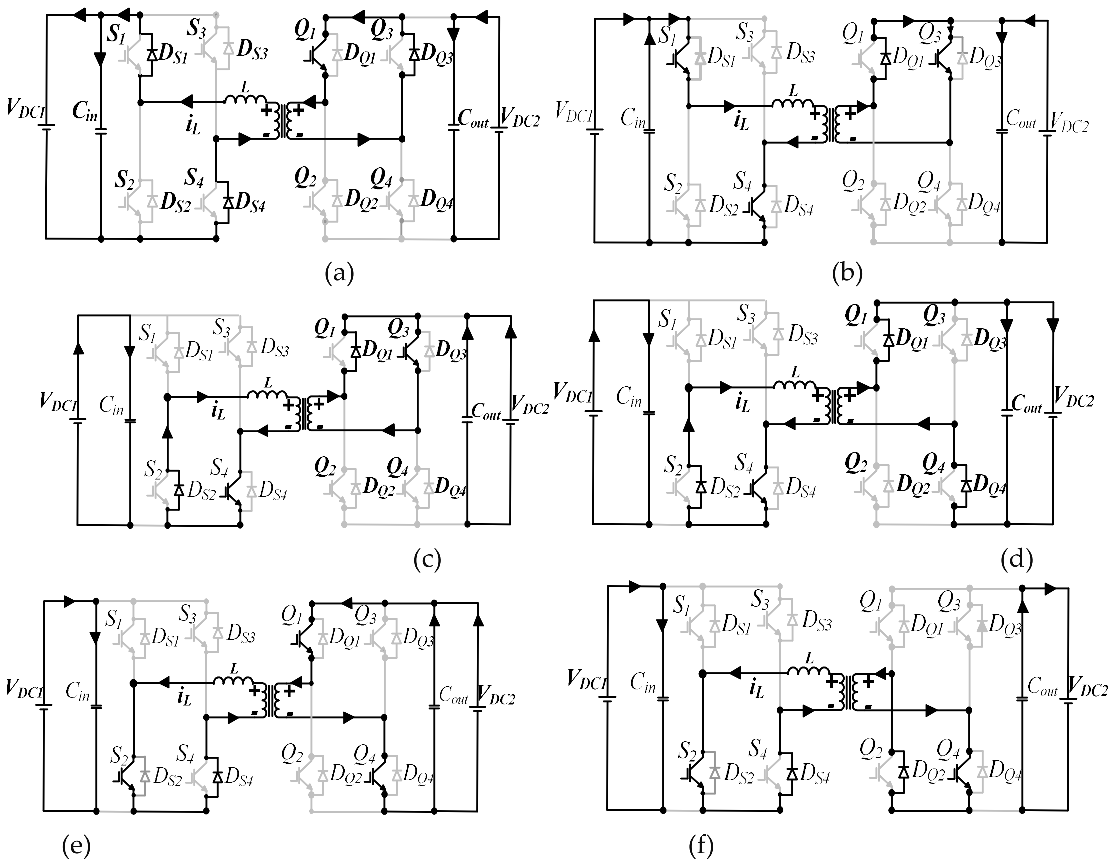

Figure A. 5. Mode 3 equivalent circuits for first half cycle (a) t_o-t'_1 (b) t'_1-t_1(c) t_1-t'_2 (d) t'_2- t_2 (e) t_2 -t_3 (f) t_3 –t_4.

Interval t_2 **-** t_3**:** At t_2, i_L, polarity change from positive to negative occurs. S_2 and D_{S4} start to conduct and in bridge B the current flows through switches Q_1 and Q_3 as shown by Figure A.5 (e). The inductor voltage is clamped at $-nV_{DC2}$ with the current remaining unchanged for the duration.

Interval t_3 **-** t_4**:** Figure A.5(f) shows the equivalent circuit for this sequence. S_2 and D_{S4} of Bridge A continue to conduct, D_{Q2} and Q_4 in H bridge-B begin to conduct. Since the difference between AC voltages, v_{ac1} and v_{ac2} is zero, this causes the voltage across the inductor to be zero. The inductor current remains unchanged.

Therefore, according to the analysis above and by assuming t_0=0, t_1= D_1T_h, t_2= D_3T_h, t_3= $(D_2+D_3)T_h$ and t_4=T_h, the inductor current for the first half cycle is computed and listed in Table A.1. Mode's equations that comprise average current, RMS current, active power, reactive power and ZVS possibility are outlined by performing step by step analysis. The result of this derivation is also tabulated in Table A.1. The peak current is given by $i_L(t_1)$ for this mode. By observing the active power expression, active power transfer is independent of D_3, meaning that it can be solely controlled by controlling bridge voltages. The power range for this mode is evaluated to be maximum of $0.5\ pu$ and minimum of $0\ pu$. This shows that the mode is only capable of unidirectional power transfer. ZVS for all switches is not possible, but rather, the mode partially achieves soft switching for some of the switches.

Table A.3. Mode 3 Mathematical expressions.

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Variable	
Currents at each switching instants	$i_L(t_0) = -\left[\frac{V_{DC1}D_1 - nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_1) = \left[\frac{V_{DC1}D_1 + nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_2) = i_L(t_1)$
	$i_L(t_3) = \left[\frac{V_{DC1}D_1 - nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_4) = i_L(t_3)$
RMS current	$I_{rms(\text{mode}3)} = \left(\left\{\left[\left[i_L^2(t_1)(D_3 - D_1)\right] + \left[i_L^2(t_3)(1 - D_2 - D_3)\right]\right] + \left[\frac{2f_sL_{tot}}{3}\left\{\left[\frac{i_L^3(t_1) - i_L^3(t_0)}{V_1}\right] - \left[\frac{i_L^3(t_3) - i_L^3(t_2)}{nV_2}\right]\right\}\right]\right\}\right)^{1/2}$
RMS voltage	$V_{Lrms(\text{mod}\,e3)} = \left(V_{DC1}^{\ 2}D_1 + (nV_{DC2})^2 D_2\right)^{1/2}$
Average power & range	$P_{(\text{mod}\,e3)} = \frac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}[D_1D_2]$ *Range:* ➡ $\begin{cases} P_{\max} = 0.5pu \ (D_1 = 0.5, D_2 = 0.5, D_3 = 0.5) \\ P_{\min} = 0pu \ (D_1 = 0, D_2 = 0, D_3 = 0) \end{cases}$
Reactive power	$Q_{\text{mod}\,e3} = v_{rms(\text{mod}\,e3)} \times i_{rms(\text{mod}\,e3)}$
ZVS	*Not achievable for all switches* ***Constraints:*** none

ii. Mode 3′

According to the operating waveforms of Figure A.4 (b), the following two constraints are evaluated for mode 3′.

$$\begin{aligned} D_2 &\le 1 - D_1 \\ D_1 - 1 \le D_3 &\le -D_2 \end{aligned} \quad \text{(A.12)}$$

Steady state analysis for first half switching cycle of mode 3′ current waveform of Figure A.4 (b) is explained below.

Interval t_0 - t'_1: The inductor current starts from negative value, D_{S1} and D_{S4} are both conducting for Bridge A. For bridge B its D_{Q2} and switch Q_4 that carry the current. The equivalent circuit for this sub-period is shown in Figure A.6 (a). The inductor voltage is V_{DC1} and current is equivalent to

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$$i_L(t)=\frac{V_{DC1}}{L_{tot}}(t-t_0)+i_L(t_0) \tag{A.13}$$

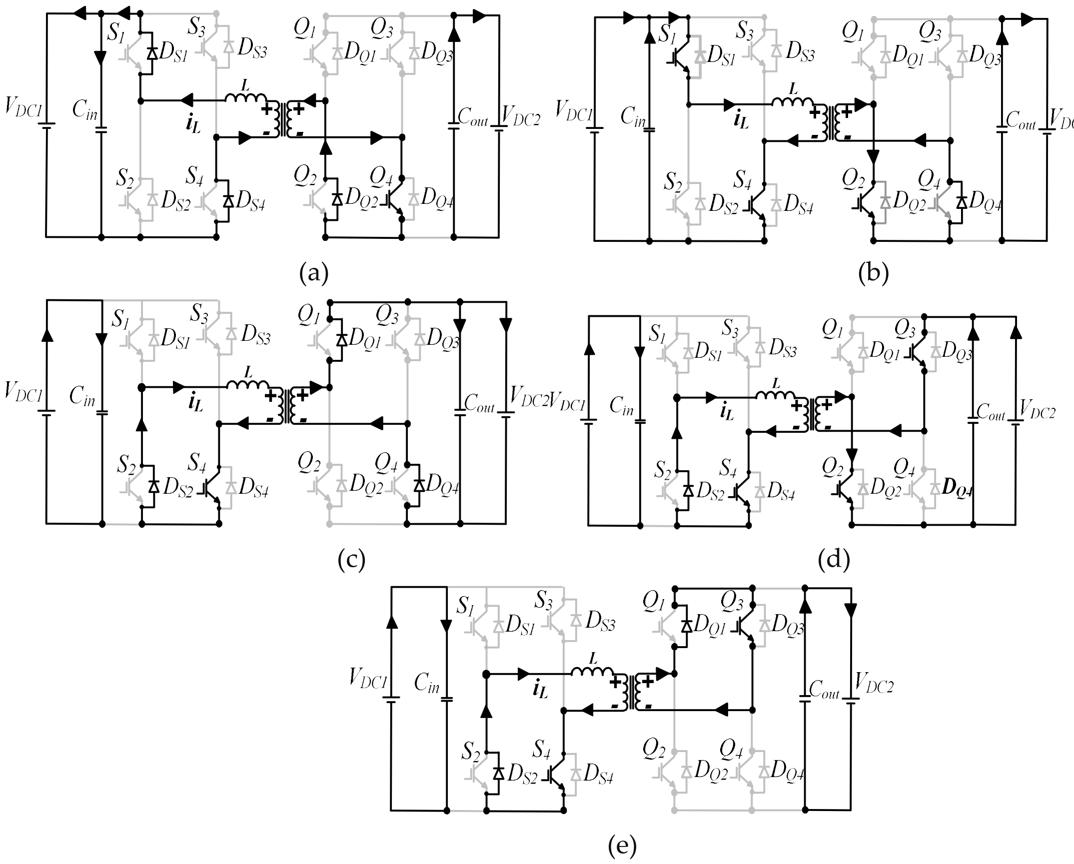

Figure A.6. Mode 3' equivalent circuit diagrams (a) t_0-t'_1 (b) t'_1-t_1 (c) t_1-t_2 (d) t_2- t_3(e) t_3 –t'_4.

Interval t'_1 ***-*** t_1***:*** Figure A.4 (b) depicts the current path during this instant. At t'_1, a polarity reversal of the current occurs. Its switches S_1 and S_4 of bridge A that carry the current, whilst the current flows through Q_2 and D_{Q4} in the second bridge. The inductor voltage continues to be clamped at V_{DC1}, and i_L magnitude remains unchanged.

Interval t_1 ***–*** t_2***:*** The slope of the current is zero, due to zero inductor voltage. For bridge A, the current circulates between D_{S2} and S_4 as Figure A.6 (c) shows. For the second H-bridge, the current flows through switches D_{Q1} and D_{Q4}.The inductor current remains unchanged for the entire segment.

Interval t_2 ***–*** t_3***:*** The current gradually ramps up during this sequence. Figure A.6 (d) shows the resulting equivalent circuit highlighting the current path. Its, D_{S2} and S_4 of bridge A , that are still conducting and for the second H-bridge, the current flows through switches Q_2 and Q_3. The interval ends when Q_2 is turned off. The voltage across the coupling inductor is nV_{DC2} and the current is

$$i_L(t)=\frac{nV_{DC2}}{L_{tot}}(t-t_2)+i_L(t_2) \tag{A.14}$$

Interval t_3 ***–*** t'_4***:*** Equivalent schematic circuit is illustrated in Figure A.6 (e) for this time instant. Since both transformer terminal voltages also for this sub-period equate to zero, the current will remain the same as segment t_2 – t_3 with zero slope. The current flows through S_2 and D_{S4} of bridge A, while D_{Q1} and Q_3 of bridge-B provide path for the current to flow through.

By substituting t_n values of t_0=0, t_1= D_1T_h,,t_2=(1-|D_3|)T_h,t_3=(1-|D_3|+D_2)T_h and t_4=T_h, in expressions (A.13) and (A.14), the inductor current at each switching interval can be evaluated. Table A.2, provides the result of the derivation. The peak current for this mode is given by $i_L(t_4)$. By following similar step by step procedure of mode 1, mode steady state equations for average current, RMS current, active, and reactive power are derived and listed in the Table A.4.

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Also observe that, the derived active power expression for mode 3′, similarly shows D_3 independence. Mode upper and lower power range capability is 0 *pu* and -0.5 *pu* respectively, providing only unidirectional transfer. ZVS for Mode 3′ is unachievable for the entire range for all the switches at the same time.

c) Modes 4 and 4′

Mode 4 waveforms which are graphically depicted in Figure A.7 (a), can be described by partial overlap of positive v_{ac1} and negative v_{ac2} during the first half cycle and during the second half cycle, partial overlap of positive v_{ac2} and negative v_{ac1} occurs. Similarly, complimentary mode 4′ is characterised by partial overlap of positive/negative v_{ac1} and v_{ac2} voltage waveforms for first and second half cycles as Figure A.7 (b) illustrates.

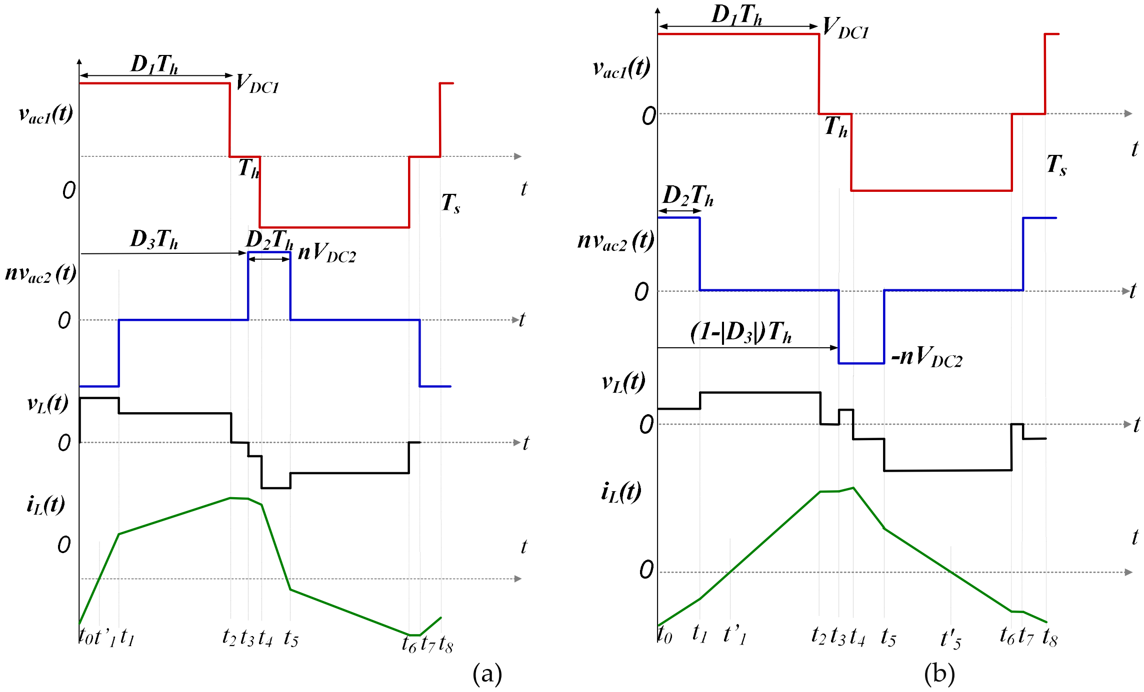


Figure A.7. (a) Mode 4 (b) Mode 4′, ideal steady state waveforms.

i. Mode 4

Considering the waveform features of Figure A.7 (a), mode 4 boundaries can be described as

$$1-D_3 \le D_2 \le 1-D_3+D_1$$
$$D_1 \le D_3 \le 1 \tag{A.15}$$

Half cycle inductor current of Figure A.4 (a) segments are analysed and explained below.

Interval t_0 **-** t'_1**:** Schematic diagram of Figure A.8 (a) shows the current path during this instant. D_{S1}, D_{S4}, D_{Q2} and D_{Q3} of DAB converter are conducting. The coupling inductor voltage is clamped at $V_{DC1}+nV_{DC2}$. Therefore, i_L is

$$i_L(t)=\frac{V_{DC1}+nV_{DC2}}{L_{tot}}(t-t_0)+i_L(t_0) \tag{A.16}$$

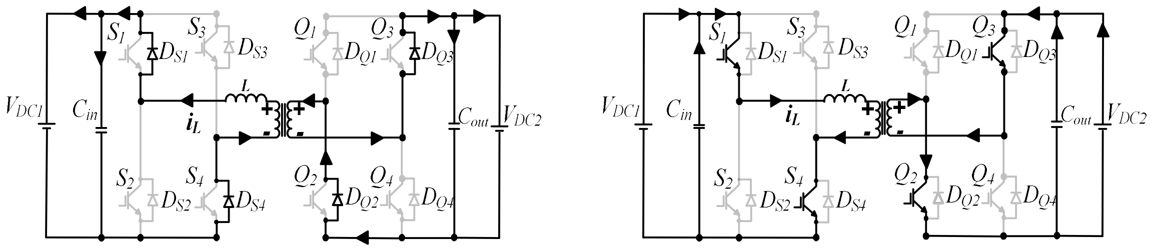
Table A.4. Derived analytical expressions Mode 3′.

Variable	
Currents at each switchin	$i_L(t_0)=-\left[\frac{V_{DC1}D_1+nV_{DC2}D_2}{4f_sL_{tot}}\right]$

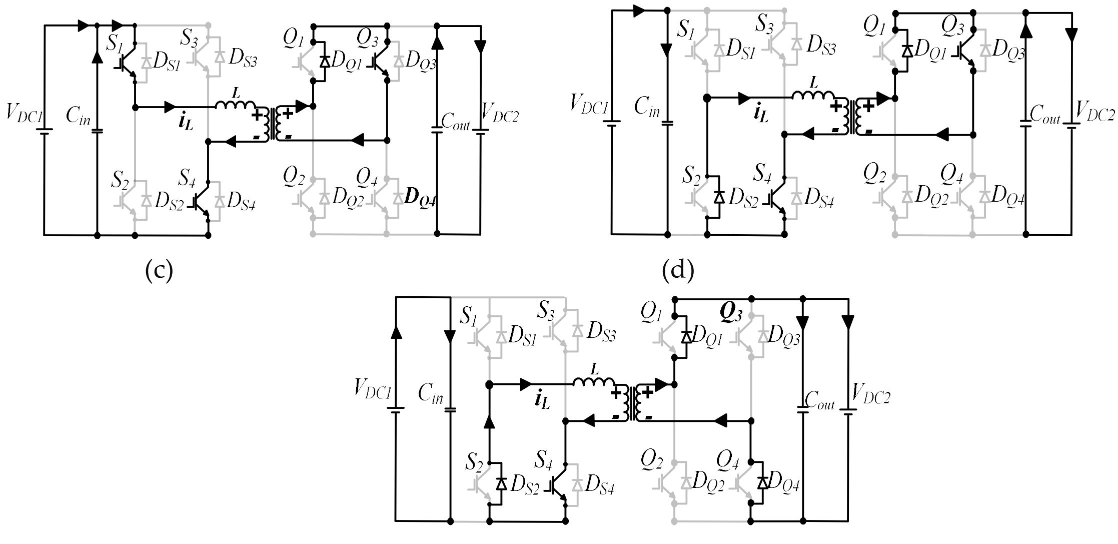
g instants	$i_L(t_1) = \left[\dfrac{V_{DC1}D_1 - nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_2) = i_L(t_1)$
	$i_L(t_3) = \left[\dfrac{V_{DC1}D_1 - nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_4) = i_L(t_3)$
RMS current	$I_{rms(mode3')} = \left(\left\{\left[i_L^2(t_1)(D_3 - D_1)\right] + \left[i_L^2(t_3)(1 - D_2 - D_3)\right] + \left[\dfrac{2f_sL_{tot}}{3}\left\{\left[\dfrac{i_L^3(t_1) - i_L^3(t_0)}{V_{DC1}}\right] + \left[\dfrac{i_L^3(t_3) - i_L^3(t_2)}{nV_{DC2}}\right]\right\}\right]\right\}\right)^{1/2}$
RMS voltage	$V_{Lrms(mode3')} = \left(V_{DC1}{}^2 D_1 + \left(nV_{DC2}\right)^2 D_2\right)^{1/2}$
Average power & range	$P_{(mode3')} = -\dfrac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}\left[D_1D_2\right]$ ***Range:*** ➡ $\begin{cases} P_{max} = 0.0\,pu \ \left(D_1 = 0, D_2 = 1, D_3 = -1\right) \\ P_{min} = -0.5\,pu \ \left(D_1 = 0.5, D_2 = 0.5, D_3 = -0.5\right) \end{cases}$
Reactive power	$Q_{mode3'} = v_{rms(mode3')} \times i_{rms(mode3')}$
ZVS	*Not achievable for all switches* ***Constraints:*** none

Interval t′₁ - t₁: At t'_1, inductor current polarity reversal occurs. Switches S_1 and S_4 of Bridge A switches Q_2 and Q_3, of bridge B are turned on. The inductor voltage is continuously clamped on at $V_{DC1}+nV_{DC2}$, with no increment in the inductor current value. This is illustrated by schematic of Figure A.8 (b).

Interval t_1 – t_2: During this interval, shown in Figure A.8 (c), the inductor current continues to increase with bridge A status remaining similar to the previous sub-period. But for bridge B, Q_2 is switched off and the current flows through D_{Q1} and Q_3 respectively. The voltage across the coupling inductor is $V_{DC1}+nV_{DC2}$.



(a) (b)



(c) (d) (e)

Figure A.8. First half cycle equivalent circuit diagrams of Mode 4 (a) t_0-t'_1 (b) t'_1-t_1 (c) t_1-t_2 (d) t_2- t_3 (e) t_3- t_4.

Interval $t_2 - t_3$***:*** The equivalent circuit diagram is illustrated by Figure A.8 (d), whereby, the current path in Bridge-B remains unchanged, while in bridge A, it circulates in D_{S2} and S_4. The inductor current is retained at the same magnitude as in previous time sequence.

Interval $t_3 - t_4$***:*** Figure A.8 (e) shows the resulting equivalent circuit of this segment. Bridge A , D_{S2} and S_4 are still conducting, but for bridge B reverse recovery diodes, D_{Q1} and D_{Q4}, provide path for the current to flow through. The voltage impressed across L_{tot} is $-nV_{DC2}$. During this instant, the current is,

$$i_L(t) = \frac{-nV_2}{L}(t - t_3) + i_L(t_3) \tag{A.17}$$

Currents at each switching interval for mode 4, can be deduced from expressions (A.16) and (A.17), by substituting t_n values of, $t_0=0$, $t_1=(D_2+D_3-1)T_h$, $t_2=D_1T_h$, $t_3=D_3T_h$ and $t_4=T_h$. These are given in Table A.5. Magnitude of $i_L(t_2)$ results in mode peak current. The corresponding expressions for steady state RMS current, average current, active and reactive powers equations are indicated in Table A.5. However, it can be seen that, maximum and minimum power limits are evaluated as 0.67 *pu* and 0 *pu* respectively. This only represents positive unidirectional power transfer capability. Finally, soft switching is realisable for all switches under this mode of operation and the corresponding constraints are also listed in Table A.5.

Table A.5. Mathematical expressions for Mode 4.

Variable	
Currents at each switching instants	$i_L(t_0) = -\left[\frac{V_{DC1}D_1 - 2nV_{DC2} + nV_{DC2}D_2 + 2nV_{DC2}D_3}{4f_sL_{tot}}\right]$
	$i_L(t_1) = \left[\frac{-V_{DC1}D_1 + 2V_{DC1}D_3 - 2V_{DC1} + 2V_{DC1}D_2 + nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_2) = \left[\frac{V_{DC1}D_1 + nV_{DC2}D_2}{4f_sL_{tot}}\right]$

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	$i_L(t_3)=i_L(t_2)$
	$i_L(t_4)=\left[\dfrac{V_{DC1}D_1-2nV_{DC2}+nV_{DC2}D_2+2nV_{DC2}D_3}{4f_sL_{tot}}\right]$
RMS current	$I_{rms(mode4)}=\left(\left\{\left[i_L^2(t_3)\left(D_3-D_1\right)\right]+\left[\dfrac{2f_sL_{tot}}{3}\left\{\left[\dfrac{i_L^3(t_1)-i_L^3(t_0)}{V_{DC1}+nV_{DC2}}\right]+\left[\dfrac{i_L^3(t_2)-i_L^3(t_1)}{V_{DC1}}\right]+\left[\dfrac{i_L^3(t_3)+i_L^3(t_0)}{nV_{DC2}}\right]\right\}\right]\right\}\right)^{1/2}$
RMS voltage	$V_{Lrms(mode4)}=\left(V_{DC1}{}^2D_1+\left(nV_{DC2}\right)^2D_2+2nV_{DC1}V_{DC2}(D_2+D_3-1)\right)^{1/2}$
Average power & range	$P_{(mode4)}=\dfrac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}\left[-D_2^2-D_3^2+2D_2+2D_3-2D_2D_3+D_1D_2-1\right]$ *Range:* ➡ $\begin{cases}P_{max}=0.667\,pu & (D_1=0.67, D_2=0.67, D_3=0.67)\\ P_{min}=0\,pu & (D_1=0.0, D_2=0.54, D_3=0.46)\end{cases}$
Reactive power	$Q_{mode4}=v_{rms(mode4)}\times i_{rms(mode4)}$
ZVS	*Achievable for all switches* ***Constraints:*** $i_L(t_0)<0, i_L(t_1)>0 \,\&\, i_L(t_2)>0$

iii. Mode 4′

Similarly, mode 4′ constraint has to ensure partial overlap of positive/negative v_{ac1} and v_{ac2} voltage waveforms for first and second half switching cycles. Thus, from Figure A.7 (b), mode 4′ boundary is given by

$$\begin{aligned}|D_3|\le D_2\le D_1+|D_3|\\ D_1-1\le D_3\le 0\end{aligned} \tag{A.18}$$

The current expression of each segment for the first half cycle of Figure A.7 (b) is analysed below,

Interval t_0 **-** t_1**:** Figure A.9 (a) shows the equivalent circuit diagram. The current flow path for bridge A is through D_{S1} and D_{S4}, while for bridge B switches Q_1 and Q_4 conduct. The voltage impressed across the inductor is V_{DC1}-nV_{DC2}. The segment ends when Q_1 is turned off. The inductor current can be written as,

$$i_L(t)=\frac{V_{DC1}-nV_{DC2}}{L_{tot}}(t-t_0)+i_L(t_0) \tag{A.19}$$

Interval t_1 **–** t'_1**:** The current continues to be negative and circulates between D_{S1} and D_{S4} of bridge A. For bridge B, D_{Q2} start to freewheel and switch Q_4 is still turned on. Voltage across L_{tot} is V_{DC1}. The equivalent schematic showing the converter during this duration is depicted in Figure A.9 (b). The current during is

$$i_L(t)=\frac{V_{DC1}}{L_{tot}}(t-t_1)+i_L(t_1) \tag{A.20}$$

Interval t'_1 **–** t_2**:** During this duration that is portrayed in Figure A.9(c), at t'_1, the current changes polarity, and therefore, switches S_1 and S_4 of bridge A start to conduct, while Q_2 and D_{Q4} of second bridge-B carry the current. The inductor voltage is still clamped at V_{DC1}. Current i_L remains same as in previous interval. The segment ends when S_1 is turned off.

Interval $t_2 - t_3$***:*** The value of the current during this sub-period also remains unchanged and both transformer terminal voltages are confined to zero state, resulting in zero inductor voltage. The equivalent circuit of Figure A.9 (d) illustrates the current path, with D_{S2}, S_4, Q_2 and D_{Q4} playing the pivotal role of conducting for both DAB H-bridges.

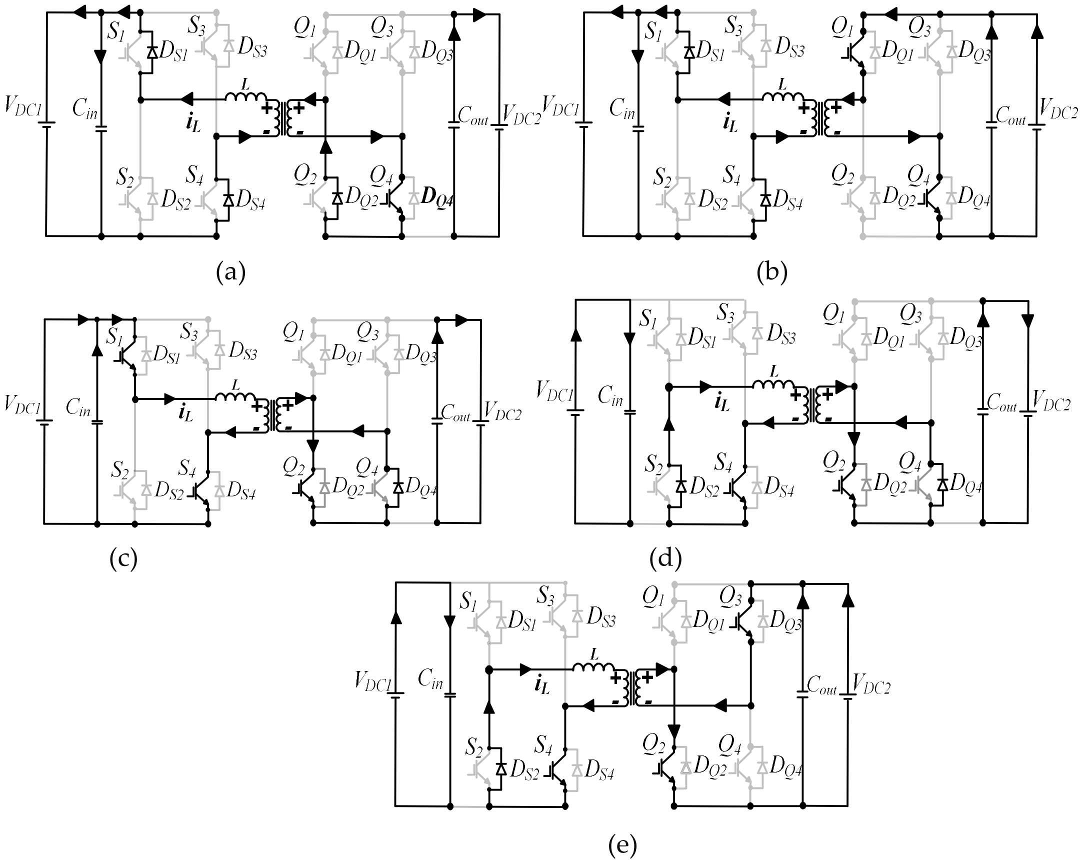


Figure A.9. Mode 4′ equivalent circuit diagrams for the first half cycle (a) t_o-t_1 (b) t_1-t'_1 (c) t'_1- t_2 (d) t_2 - t_3 (e) t_3- t_4 .

Interval $t_3 - t_4$***:*** Figure A.9 (e) shows the equivalent schematic diagram during this switching instant. In bridge A conducting devices remain unchanged, but for bridge B switches Q_2 and Q_3 start to provide path for the current path. The voltage across the coupling inductor is nV_{DC2}. Therefore, i_L which is linearly increasing is deduced as,

$$i_L(t) = \frac{nV_{DC2}}{L_{tot}}(t - t_3) + i_L(t_3) \tag{A.21}$$

Based on the above analysis, the inductor current at each switching segments is evaluated by assuming, $t_0=0, t_1=(D_2-|D_3|)T_h, t_2=D_1T_h, t_3=(1-|D_3|)T_h$ and $t_4=T_h$. The resulting values of the current at each switching instant are shown in Table A.4. Using these current values, other vital parameters of complimentary mode 4′ are similarly derived and summarised in Table A.4. Peak inductor current is given by equation $i_L(t_4)$. As can be observed also, the mode permits only unidirectional reverse power flow with the upper and lower active power limits given by 0.0 *pu* and -0.67 *pu* respectively. The corresponding TPS modulations parameters also listed. In addition, it's worth mentioning that ZVS for this mode is not realisable for the entire switches.

d) Modes 5 and 5′

Figure A.10 shows modes 5 and 5′ operating waveforms. As indicated, Mode 5 of Figure A.10 (a) is characterised by partial overlap of positive v_{ac1} and positive v_{ac2} for the first half cycle and vice versa during the second half cycle. Complimentary mode 5′, waveforms, which are plotted in Figure A.10 (b), is described by partial overlap of positive v_{ac1} and negative v_{ac2} during the first half cycle.

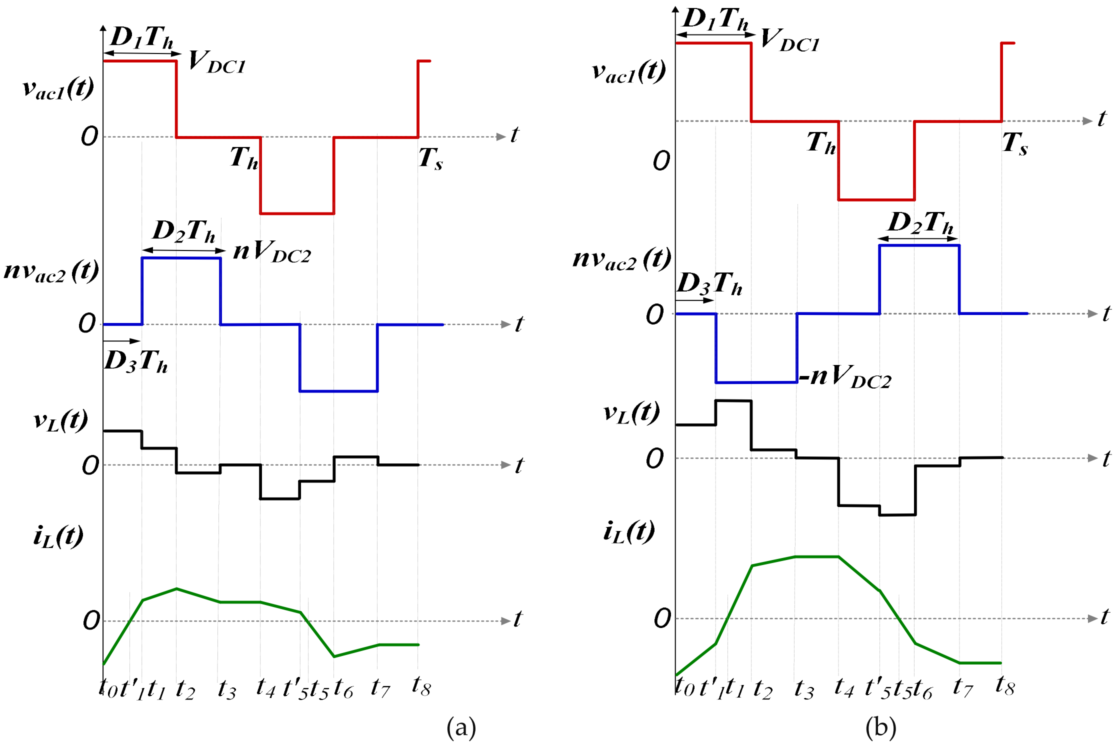


Figure A.10. Steady state transformer voltages and inductor current (a) Mode 5 (b) Mode 5′.

i. Mode 5

The mode constraint according to Figure A.10 (a) is

$$\begin{gathered} D_1 - D_3 \le D_2 \le 1 - D_3 \\ 0 \le D_3 \le D_1 \end{gathered} \tag{A.22}$$

Table A.6. Derived analytical expressions representing mode 4′.

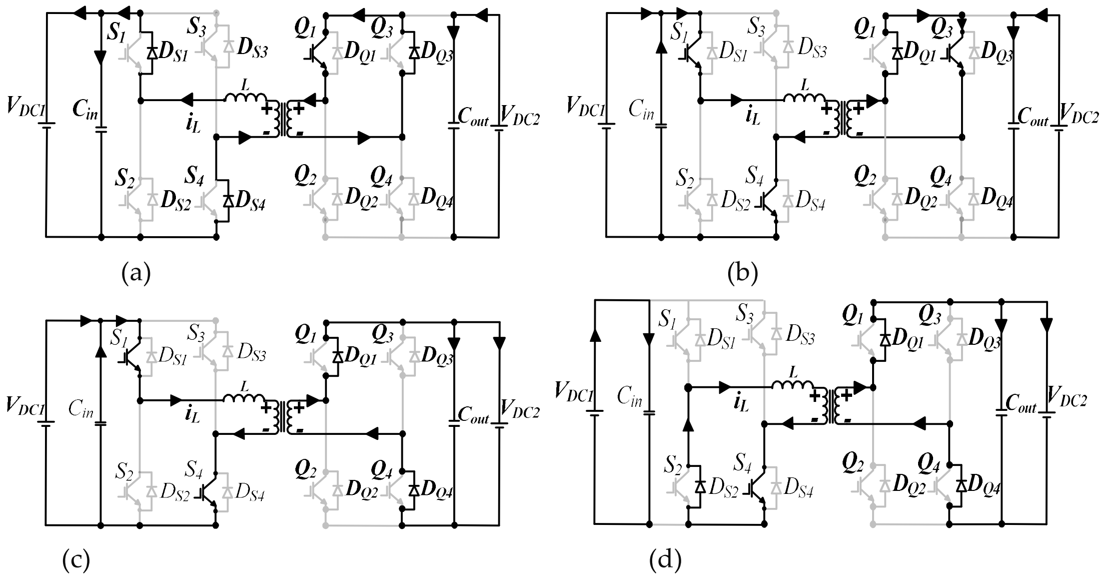
Variable	
Currents at each switching instants	$i_L(t_0) = -\left[\dfrac{V_{DC1}D_1 - nV_{DC2}D_2 + 2nV_{DC2}\lvert D_3\rvert}{4f_sL_{tot}}\right]$
	$i_L(t_1) = \left[\dfrac{-V_1D_{DC1} + 2V_1D_{DC2} - 2V_{DC1}\lvert D_3\rvert - nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_2) = \left[\dfrac{V_{DC1}D_1 - nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_3) = i_L(t_2)$
	$i_L(t_4) = \left[\dfrac{V_{DC1}D_1 - nV_{DC2}D_2 + 2nV_{DC2}\lvert D_3\rvert}{4f_sL_{tot}}\right]$

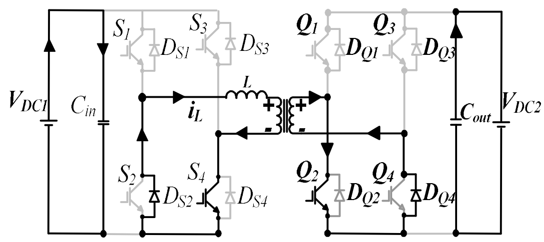
RMS current	$I_{rms(mode4')} = \left(\left\{\left[i_L^{\,2}(t_3)\left(1-\lvert D_3\rvert - D_1\right)\right] + \left[\frac{2f_s L_{tot}}{3}\left\{\left[\frac{i_L^{\,3}(t_1)-i_L^{\,3}(t_0)}{V_{DC1}-nV_{DC2}}\right] + \left[\frac{i_L^{\,3}(t_2)-i_L^{\,3}(t_1)}{V_{DC1}}\right] - \left[\frac{i_L^{\,3}(t_3)+i_L^{\,3}(t_0)}{nV_{DC2}}\right]\right\}\right]\right\}\right)^{1/2}$
RMS voltage	$V_{Lrms(mode4')} = \left(\left[V_{DC1}{}^{2} D_1 + \left(nV_{DC2}\right)^2 D_2 - 2nV_{DC1}V_{DC2}(D_2 - \lvert D_3 \rvert)\right]\right)^{1/2}$
Average power & range	$P_{(mode4')} = \frac{nV_{DC1}V_{DC2}}{4f_s L_{tot}}\left[D_2^2 + \lvert D_3\rvert^2 - 2D_2\lvert D_3\rvert - D_1 D_2\right]$ *Range:* ➡ $\begin{cases} P_{max} = 0pu \ \ (D_1 = 0.0, D_2 = 0.0, D_3 = 0.0) \\ P_{min} = -0.67pu\left(D_1 = 0.65, D_2 = 0.67, D_3 = -0.35\right) \end{cases}$
Reactive power	$Q_{mode4'} = v_{rms(mode4')} \times i_{rms(mode4')}$
ZVS	*Not achievable for all switches* ***Constraints:*** none

The mode half switching intervals of Figure A.10 (a) can be divided into five segments which are analysed as follows.

Interval $t_0 - t'_1$: During this interval, the current circulates between reverse recovery diodes D_{S1} and D_{S4} of bridge A, while in bridge B its Q_1 and D_{Q3} that provide path for the current to flow through. This is illustrated in the equivalent circuit of Figure A.11(a). The voltage across the inductor is V_{DC1} and thus, the inductor current is given by

$$i_L(t) = \frac{V_{DC1}}{L_{tot}}(t - t_0) + i_L(t_0) \tag{A.23}$$





(e)

Figure A.11. Equivalent circuits of Mode 5 (a) t_o-t'_1 (b) t'_1-t_1 (c) t_1- t_2 (d) t_2 - t_3 (e) t_3- t_4 .

Interval ***$t'_1 - t_1$:*** Figure A.11 (b), shows the equivalent diagram. As a result of current polarity reversal, switches S_1 and S_4, of H bridge A conduct, while in bridge B the current is carried by D_{Q1} and Q_3. The voltage across the inductor continues to be clamped at V_{DC1} and the current during this instant remains constant.

Interval ***$t_1 - t_2$:*** The time instant starts upon turn off of switch Q_3. The current continues to slowly increment, bridge A switching pattern is similar to previous segment, but for bridge B, the current starts to flow through D_{Q1} and D_{Q4}. This is illustrated by Figure A.11 (c). Inductor voltage is V_{DC1}-nV_{DC2} and current i_L during this duration is expressed as

$$i_L(t) = \frac{V_{DC1} - nV_{DC2}}{L_{tot}}(t - t_1) + i_L(t_1) \tag{A.23}$$

Interval ***$t_2 - t_3$:*** Figure A.11 (d), shows the equivalent circuit. The same current path exists for bridge B but for H bridge A, D_{S2} and S_4 provide path for the current to pass through. The inductor voltage is given by -nV_{DC2}. Thus, i_L for this instant can analytically be represented as,

$$i_L(t) = \frac{-nV_{DC2}}{L_{tot}}(t - t_2) + i_L(t_2) \tag{A.24}$$

Interval ***$t_3 - t_4$:*** Transformer terminal voltages are zero during this duration. The current remains constant with a value given by expression (A.24) and thus, no instantaneous power transferred. Figure A.11 (e) shows the equivalent circuit diagram. In bridge A, D_{S2} and S_4 conduct the current and in the second H-bridge, Q_2 and D_{Q4}.

According to equations (A.22) - (A.24), the values of the inductor current at each sub-period, is evaluated by assuming $t_0=0$, $t_1=D_3T_h$, $t_2=D_1T_h$, $t_3=(D_2+D_3)T_h$ and $t_4=T_h$. As shown in Table A.7, the final mathematical equations for inductor current at each instant, average current, RMS current, average power and reactive power are obtained for mode 5. Based on this analysis, it can be concluded that $i_L(t_2)$ gives the peak inductor current. The mode achieves only unidirectional power flow, with corresponding upper and lower power transfer limits of 0.67 *pu* and 0.0 *pu* respectively. Finally, soft switching for all switches is unattainable for this mode, but rather, ZVS is only partially obtainable for some of the switches.

Table A.7. Mode 5 key performance indicators.

Variable	
Currents at each switching instants	$i_L(t_0) = -\left[\frac{V_{DC1}D_1 - nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_1) = \left[\frac{-V_{DC1}D_1 + 2V_{DC2}D_3 + nV_{DC2}D_2}{4f_sL_{tot}}\right]$

	$i_L(t_2)=\left[\dfrac{V_{DC1}D_1-2nV_{DC2}D_1+nV_{DC2}D_2+2nV_{DC2}D_3}{4f_sL_{tot}}\right]$
	$i_L(t_3)=\left[\dfrac{V_{DC1}D_1-nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_4)=i_L(t_3)$
RMS current	$I_{rms(\text{mode}5)}=\left(\left\{\left[i_L^2(t_3)(D_3-D_2)\right]+\left[\dfrac{2f_sL_{tot}}{3}\left\{\left[\dfrac{i_L^3(t_1)-i_L^3(t_0)}{V_1}\right]+\left[\dfrac{i_L^3(t_2)-i_L^3(t_1)}{V_1-nV_2}\right]-\left[\dfrac{i_L^3(t_3)-i_L^3(t_2)}{nV_2}\right]\right\}\right]\right\}\right)^{1/2}$
RMS voltage	$V_{Lrms(\text{mod}\,e5)}=\left(\left[V_1^2D_1+(nV_{DC2})^2D_2+2nV_1V_2(D_3-D_1)\right]\right)^{1/2}$
Average power & range	$P_{(\text{mod}\,e5)}=\dfrac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}\left[-D_1^2-D_3^2+2D_1D_3+D_2D_1\right]$ ***Range :*** ➡ $\begin{cases}P_{\max}=0.667\,pu & (D_1=0.67, D_2=0.65, D_3=0.35)\\ P_{\min}=0\,pu & (D_1=0, D_2=0, D_3=0)\end{cases}$
Reactive power	$Q_{\text{mod}\,e5}=v_{rms(\text{mod}\,e5)}\times i_{rms(\text{mod}\,e5)}$
ZVS	*Not achievable for all switches* ***Constraints:*** none

ii. Mode 5′

By shifting the waveforms of Figure A.10 (b), to the negative half plane, mode 5′ constraint can be expressed as,

$$\begin{aligned}&D_1+|D_3|-1\le D_2\le |D_3|\\&-1\le D_3\le D_1-1\end{aligned} \tag{A.25}$$

Five segments emerge for the first half switching cycle, based on the waveforms of Figure A.10 (b), which are briefly described below.

Interval t_0– t'_1: As shown in circuit structure of Figure A.12 (a), anti-parallel diodes D_{S1} and D_{S4} of bridge A conduct, while for the second bridge, current flows through diode D_{Q2} and switch Q_3. The inductor voltage is clamped at V_{DC1} and the current continues to ramp up and is expressed as,

$$i_L(t)=\frac{V_{DC1}}{L_{tot}}(t-t_0)+i_L(t_0) \tag{A.26}$$

Interval t'_1– t_1: Diodes D_{S1} and D_{S4} are still conducting for bridge A, however for bridge B, D_{Q3} and diode D_{Q2} start to freewheel as shown in Figure A.12 (b). The coupling inductor voltage is $V_{DC1}+nV_{DC2}$. The current continues to increment, and its value is deduced as

$$i_L(t)=\frac{V_{DC1}+nV_{DC2}}{L_{tot}}(t-t_1)+i_L(t_1) \tag{A.27}$$

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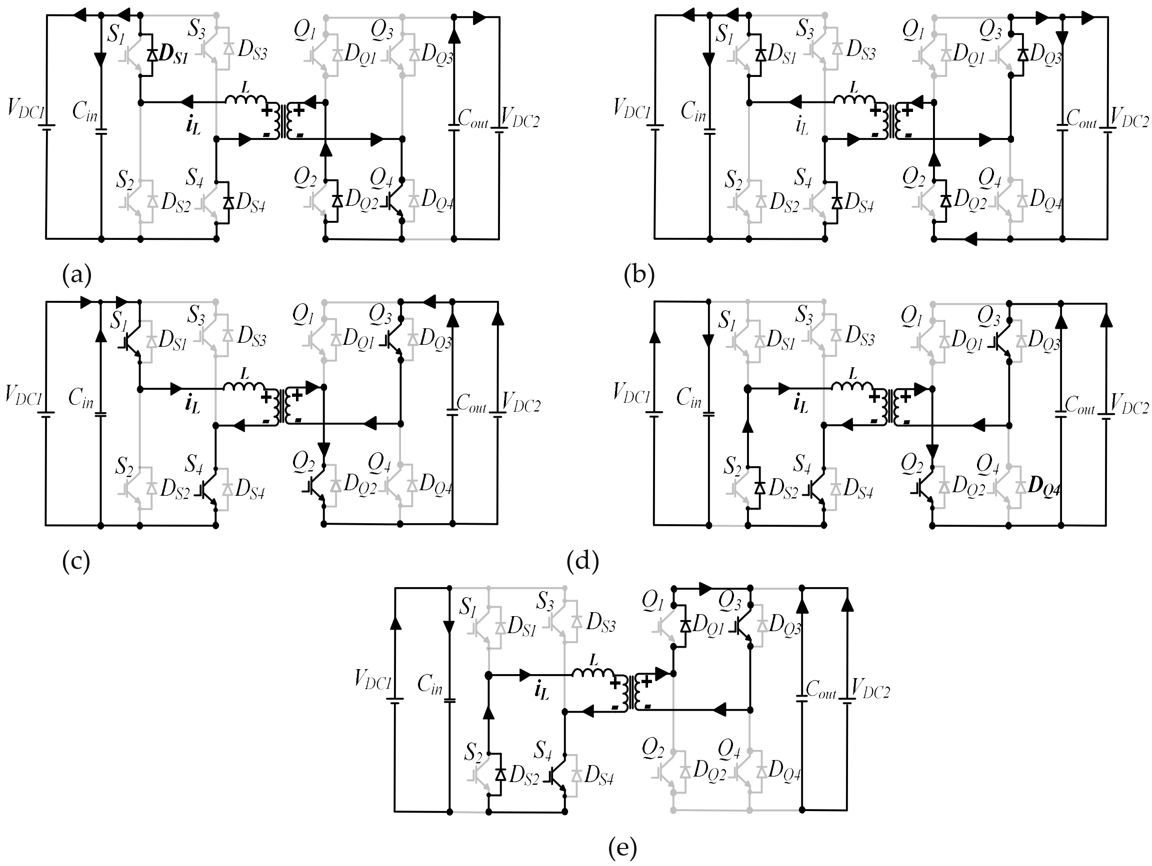

Figure A.12. Mode 5′ detailed equivalent circuits for first half cycle sequence (a) t_o-t'_1 (b) t'_1-t_1 (c) t_1 -t_2 (d) t_2- t_3 (e) t_3- t_4 .

Interval t_1***–*** t_2***:*** At t'_1, the current changes polarity, with switches S_1, S_4, Q_3 and Q_4 of both bridges providing current path as illustrated in Figure A.12(c). The magnitude of the current remains similar to previous segment and inductor voltage is clamped at $V_{DC1}+nV_{DC2}$.

Interval t_2***–*** t_3***:*** Switches Q_3 and Q_4 are still conducting for bridge B while D_{S2} and S_4 of bridge A provide path for the current to flow through as depicted in Figure A.12(d). The inductor voltage is given by nV_{DC2}. Therefore, i_L slope can be written as

$$i_L(t)=\frac{nV_{DC2}}{L_{tot}}(t-t_1)+i_L(t_1) \tag{A.28}$$

Interval t_3***–*** t_4***:*** Sub-period starts when Q_2 is switched off. Both transformer AC voltages are zero. The equivalent circuit is plotted in Figure A.12(e). Current path for bridge A , still remains unchanged and for bridge B anti-parallel diode D_{Q1} and switch Q_3 conduct the current. i_L is unchanged for this duration.

Based on the analysis above, analytical expressions for the mode currents and other key indices are calculated by assuming t_n values of, $t_0=0$,t_1= $(1-|D_3|)T_h$,t_2= D_1T_h,t_3=$(1-|D_3|+ D_2)T_h$ and t_4=T_h. The resulting values of the derivations for mode 5′ are tabulated in Table A.6. The maximum current obtained is $i_L(t_3)$= $i_L(t_4)$. The mode is capable of only unidirectional power range of 0.0 *pu* and -0.67 *pu*. Moreover, ZVS is achievable across all switches and the resulting inequalities that define the soft switching boundary are also given in Table A.8.

e) Modes 6 and 6′

Figure A.13 illustrates modes 6 and 6′ operational waveforms. Mode 6 displayed by Figure A.13 (a) is characterised by partial overlap of positive v_{ac2} with positive and negative of v_{ac1}. Complimentary mode 6′ waveforms of Figure A.13 (b), portrays inverse features of mode 6′

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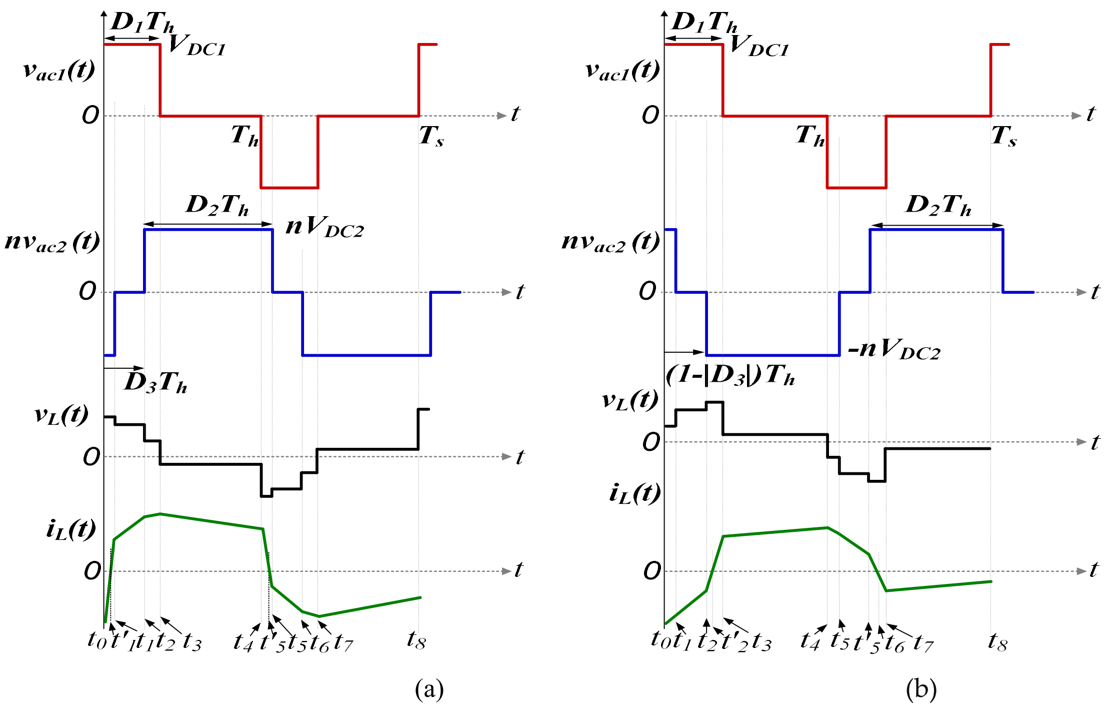

Figure A.13. Ideal voltage/current waveforms of (a) Mode 6 (b) Mode 6′.

Table A.8. Key derivations for Mode 5′.

Variable	
Currents at each switching instants	$i_L(t_0)=-\left[\dfrac{V_{DC1}D_1+nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_1)=\left[\dfrac{-V_{DC1}D_1-2V_{DC1}\lvert D_3\rvert+2V_{DC1}-nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_2)=\left[\dfrac{V_{DC1}D_1+2nV_{DC2}D_1+2nV_{DC2}\lvert D_3\rvert-2nV_{DC2}-nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_3)=\left[\dfrac{V_{DC1}D_1+nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_4)=i_L(t_3)$
RMS current	$I_{rms(mode5')}=\left(\left\{\left[i_L^2(t_3)\left(\lvert D_3\rvert-D_2\right)\right]+\left[\dfrac{2f_sL_{tot}}{3}\left\{\left[\dfrac{i_L^3(t_1)-i_L^3(t_0)}{V_1}\right]+\left[\dfrac{i_L^3(t_2)-i_L^3(t_1)}{V_1+nV_2}\right]+\left[\dfrac{i_L^3(t_3)-i_L^3(t_2)}{nV_2}\right]\right\}\right]\right\}\right)^{1/2}$
RMS voltage	$V_{Lrms(mode5')}=\left(\left[V_{DC1}^2D_1+\left(nV_{DC2}\right)^2D_2+2nV_{DC1}V_{DC2}\left(D_1+\left(\lvert D_3\rvert-1\right)\right)\right]\right)^{1/2}$

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Average power & range	$P_{(mode5')} = \frac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}\left[D_1^2+\lvert D_3\rvert^2-2D_1-2\lvert D_3\rvert+2D_1\lvert D_3\rvert-D_1D_2+1\right]$ *Range:* ➡ $\begin{cases} P_{max}=0\,pu \ (D_1=0.19, D_2=0, D_3=-0.81) \\ P_{min}=-0.667\,pu \ (D_1=0.66, D_2=0.67, D_3=-0.67) \end{cases}$
Reactive power	$Q_{mode5}=v_{rms(mode5')}\times i_{rms(mode5')}$
ZVS	*Achievable for all switches* ***Constraints:*** $i_L(t_0)<0, i_L(t_1)<0 \& i_L(t_2)>0$

i. Mode 6

Mode constraint is determined by observing voltage waveforms of Figure A.13 (a) and ensuring that the waveform features are not violated. This is given by,

$$\begin{gathered} 1-D_2 \le D_1 \\ 1-D_2 \le D_3 \le D_1 \end{gathered} \tag{A.29}$$

Mode half cycle interval for each sequence of Figure A.10 (a) is described below.

Interval t_0 – t'_1: The inductor current is negative, hence, D_{S1} and D_{S4} of bridge A are freewheeling, whilst for bridge B, the current similarly flows through anti-parallel diodes D_{Q2} and D_{Q3}, as shown in circuit structure of Figure A.14 (a). At the end of the segment, the current falls to zero and the inductor voltage is clamped at $V_{DC1}+nV_{DC2}$. i_L can be deduced from

$$i_L(t)=\frac{V_{DC1}+nV_{DC2}}{L_{tot}}(t-t_0)+i_L(t_0) \tag{A.30}$$

Interval t'_1– t_1: Polarity change for i_L occurs at t'_1. Figure A.14 (b) shows resulting equivalent circuit showing switches S_1, S_4, Q_2 and Q_3 providing path for the current to flow through. The current value remains unchanged during this segment and is given by expression (A.30). Similarly, the voltage impressed across the coupling inductor is retained at $V_{DC1}+nV_{DC2}$.

Interval t_1– t_2: Plot of Figure A.14 (c) shows the schematic diagram illustrating current path during this sub-period. The operation of bridge A remains unchanged, while D_{Q1} and Q_3 of bridge-B conduct. The inductor voltage is V_{DC1}. The current starts to ramp up and can be expressed according to

$$i_L(t)=\frac{V_{DC1}}{L_{tot}}(t-t_1)+i_L(t_1) \tag{A.31}$$

Interval t_2– t_3: As can be seen on Figure A.14 (d), during this time instant, switches S_1 and S_4, are still conducting, while for bridge B reverse recovery diodes, D_{Q1} and D_{Q4} carry the current. The inductor voltage is V_{DC1}-nV_{DC2} and i_L continues to rise steeply with a slope given by,

$$i_L(t)=\frac{V_{DC1}-nV_{DC2}}{L_{tot}}(t-t_2)+i_L(t_2) \tag{A.32}$$

Interval t_3– t_4: During this segment, D_{Q1} and D_{Q4} of H-bridge B still provide path for the current to flow through and for H bridge A, the current starts to circulate between DS_2 and S_4. The equivalent circuit is shown in Figure A.14 (e). The voltage across the inductor been given -nV_{DC2} and the current slightly decrease, and is derived as

$$i_L(t)=\frac{-nV_{DC2}}{L_{tot}}(t-t_3)+i_L(t_3) \tag{A.33}$$

Applying similar step by step procedures to mode 6 and by assuming $t_0=0$, $t_1=(D_3+D_2-1)T_h$, $t_2=D_3T_h$, $t_3=D_1T_h$ and $t_4=T_h$. Solutions for mode currents, active power, reactive power and ZVS boundaries are obtained and given in Table A.9. The mode peak current is achieved by $i_L(t_3)$. It can be observed from the results of Table A.9, the mode can operate at maximum power of 1 *pu* and minimum 0.0 *pu* range. Finally, soft switching is attainable for this mode and the corresponding inequalities that define the ZVS range are listed.

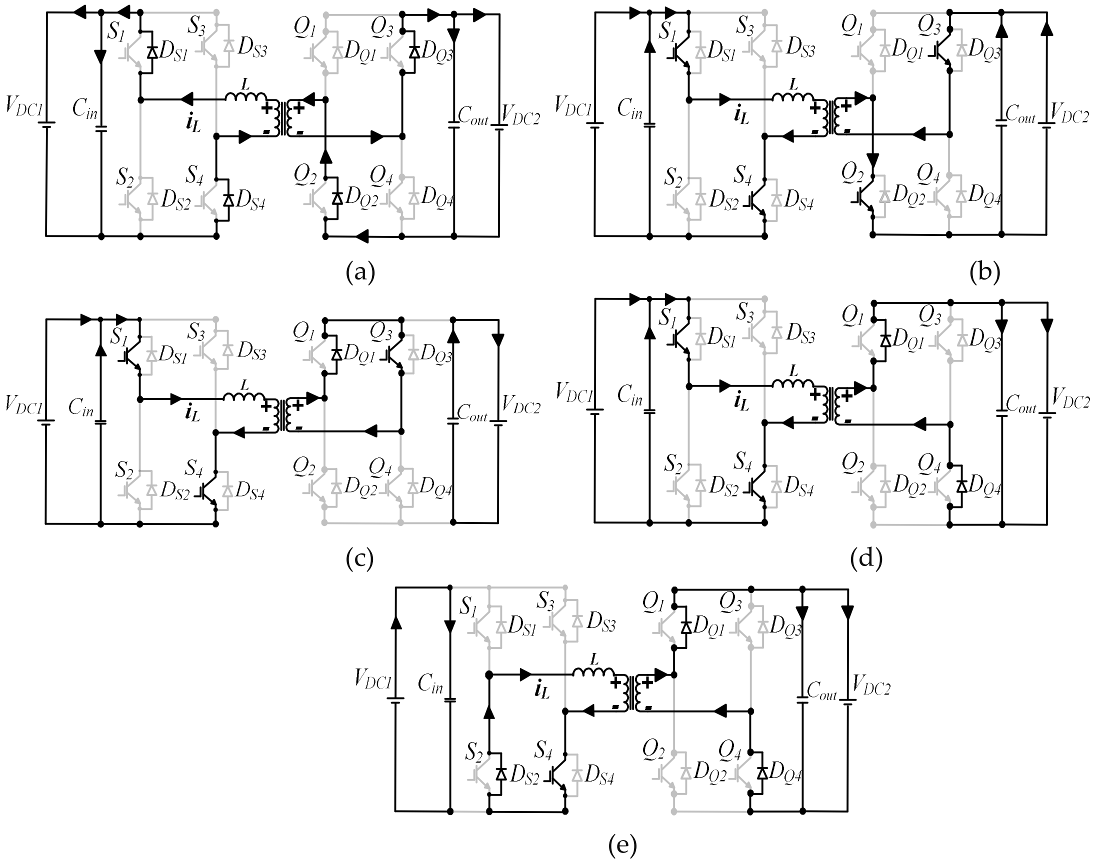

Figure A.14. Equivalent circuit diagrams for mode 6 first half cycle (a) t_0-t'_1 (b) t'_1-t_1 (c) t_1-t_2 (d) t_2- t_3 (e) t_3- t_4 .

i. Mode 6′

Mode constraints can be determined by observing the theoretical waveforms of Figure A.10 (b) and by shifting it to negative half plane. The inequalities describing the mode boundary should ensure partial overlap of positive v_{ac1}(t) with positive & negative of $v_{ac2}(t)$ and is given by

$$\begin{aligned} 1-D_2 &\le D_1 \\ -D_2 \le D_3 &\le -1+D_1 \end{aligned} \quad \text{(A.34)}$$

Analysis of various switching instant of Figure A.10 (b) waveforms for the first half cycle interval is discussed below and are plotted in detailed equivalent diagrams of Figure A.12.

Interval t_0– t_1: Figure A.15 (a) shows the current path. For bridge A and B, D_{S1}, D_{S4}, D_{Q1} and D_{Q4} allow current to pass through. The voltage across the inductor is clamped at V_{DC1}-nV_{DC2} and the current through L_{tot} is given by

$$i_L(t)=\frac{V_{DC1}-nV_{DC2}}{L_{tot}}(t-t_0)+i_L(t_0) \quad \text{(A.35)}$$

Interval t_1– t_2: The current continues to circulate between D_{S1} and D_{S4} anti-parallel diodes. In bridge B, switch Q_2 and reverse recovery diode D_{Q4} allow to current to flow through as can be seen in Figure A.15 (b). The inductor voltage is V_{DC1} and thus i_L is

$$i_L(t)=\frac{V_{DC1}}{L_{tot}}(t-t_1)+i_L(t_1) \tag{A.36}$$

Interval t₂– t′₂: Figure A.15 (c) demonstrates the equivalent circuit during this switching instant. The operation of bridge A remains unchanged, as the current is still negative, D_{S1} and D_{S4} remain in the conduction path. Meanwhile, in bridge B, current flows through diodes D_{Q2} and D_{Q3} until it decreases to zero. The voltage across the inductor is V_{DC1}-nV_{DC2}. And the current is given by

Table A.9. Mode 6 expressions.

Variable	
Currents at each switching instants	$i_L(t_0)=-\left[\frac{V_{DC1}D_1+nV_{DC2}D_2+2nV_{DC2}D_3-2nV_{DC2}}{4f_sL_{tot}}\right]$
	$i_L(t_1)=\left[\frac{-V_{DC1}D_1+2V_{DC1}D_2+2V_{DC1}D_3-2V_{DC1}+nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_2)=\left[\frac{-V_{DC1}D_1+2V_{DC1}D_3+nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_3)=\left[\frac{V_{DC1}D_1-2nV_{DC2}D_1+nV_{DC2}D_2+2nV_{DC2}D_3}{4f_sL_{tot}}\right]$
	$i_L(t_4)=\left[\frac{V_{DC1}D_1+nV_{DC2}D_2+2nV_{DC2}D_3-2nV_{DC2}}{4f_sL_{tot}}\right]$
RMS current	$I_{rms(mode6)}=\left(\left\{\left[\frac{2f_sL_{tot}}{3}\left\{\left[\frac{i_L^3(t_1)-i_L^3(t_0)}{V_{DC1}+nV_{DC2}}\right]+\left[\frac{i_L^3(t_2)-i_L^3(t_1)}{V_{DC1}}\right]+\left[\frac{i_L^3(t_3)-i_L^3(t_2)}{V_{DC1}-nV_{DC2}}\right]+\left[\frac{i_L^3(t_0)+i_L^3(t_3)}{nV_{DC2}}\right]\right\}\right]\right\}\right)^{1/2}$
RMS voltage	$V_{Lrms(mode6)}=\left(\left[V_{DC1}{}^2D_1+(nV_{DC2})^2D_2+2nV_{DC1}V_{DC2}(D_2+2D_3-D_1-1)\right]\right)^{1/2}$
Average power & range	$P_{(mode6)}=\frac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}\left[-D_1^2-D_2^2-2D_3^2+2D_3-2D_2D_3+D_1D_2+2D_1D_3+2D_2-1\right]$ *Range:* ➡ $\begin{cases}P_{max}=1\,pu & (D_1=1,D_2=1,D_3=0.5)\\P_{min}=0\,pu & (D_1=0,D_2=1,D_3=0)\end{cases}$
Reactive power	$Q_{mode6}=v_{rms(mode6)}\times i_{rms(mode6)}$

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ZVS	*Achievable for all switches* ***Constraints:*** $i_L(t_0)<0, i_L(t_1)>0, i_L(t_2)>0 \& i_L(t_3)>0$

$$i_L(t)=\frac{V_{DC1}+nV_{DC2}}{L_{tot}}(t-t_2)+i_L(t_2) \tag{A.37}$$

Interval t'_2***–*** t_3***:*** At t'_2, the current changes to positive. Figure A.15 (d) displays the current path during this sub-period. Switches, S_1, S_4, Q_2 and Q_3 are turned on respectively. V_{DC1}-nV_{DC2}, is continually been impressed across the inductor voltage and i_L magnitude is unchanged.

Interval t_3***–*** t_4***:*** The current continues to ramp up gradually and the equivalent circuit structure is shown in Figure A.15 (e). In bridge B the current continues to flow through switches Q_2 and Q_3, but due to zero state of voltage v_{ac1}, D_{S2} and S_4 of bridge A conduct. The voltage across the inductor is nV_{DC2} and the slope of i_L can be deduced from

$$i_L(t)=\frac{nV_{DC2}}{L_{tot}}(t-t_3)+i_L(t_3) \tag{A.38}$$

According to aforementioned analysis, the inductor current at each intervals discussed above is computed by assuming $t_0=0$, $t_1=(D_2-|D_3|)T_h$, $t_2=(1-|D_3|)T_h$, $t_3=D_1T_h$ and $t_4=T_h$. This are provided in Table 3.11 below, in addition other mode's important parameters are computed. Observe that the peak inductor current is obtained through $i_L(t_4)$. The derived mode active power output and range is tabulated in Table 10, with a corresponding unidirectional upper and lower transfer limit of 0.0 *pu* and -1.0 *pu* respectively. The converter switches can operate under ZVS with the boundary defined by the instantaneous current inequalities.

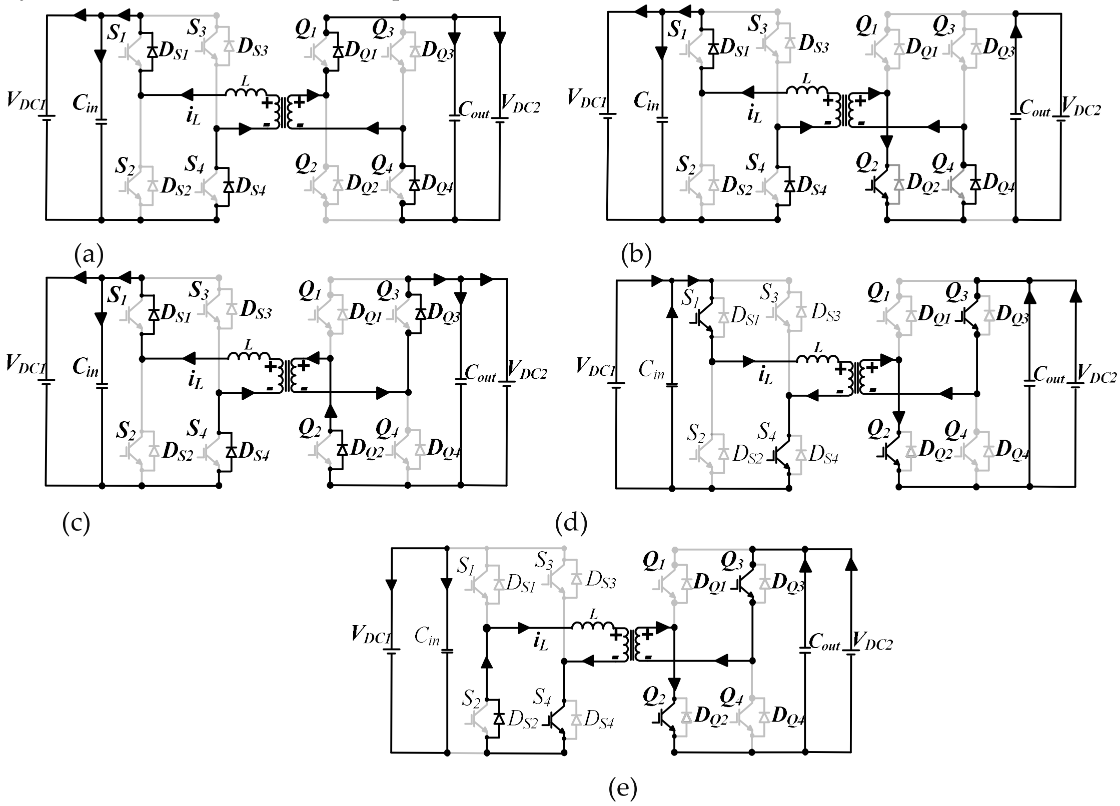

Figure A.15. Detailed equivalent circuits of Mode 6′ (a) t_0-t_1 (b) t_1- t_2 (c) t_2-t'_2 (d) t'_2 - t_3 (e) t_3- t_4.

Table A.10. Mode 6′ parameters.

Variable	
Currents at each switching instants	$i_L(t_0) = -\left[\dfrac{V_{DC1}D_1 - nV_{DC2}D_2 + 2nV_{DC2}\lvert D_3\rvert}{4f_sL_{tot}}\right]$
	$i_L(t_1) = \left[\dfrac{-V_{DC1}D_1 + 2V_{DC1}D_2 - 2V_{DC1}\lvert D_3\rvert - nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_2) = \left[\dfrac{-V_{DC1}D_1 - 2V_{DC1}\lvert D_3\rvert + 2V_{DC1} - nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_3) = \left[\dfrac{V_{DC1}D_1 + 2nV_{DC2}D_1 + 2nV_{DC2}\lvert D_3\rvert - 2nV_{DC2} - nV_{DC2}D_2}{4f_sL_{tot}}\right]$
	$i_L(t_4) = \left[\dfrac{V_{DC1}D_1 - nV_{DC2}D_2 + 2nV_{DC2}\lvert D_3\rvert}{4f_sL_{tot}}\right]$
RMS current	$I_{rms(mode6')} = \left(\left[\dfrac{2f_sL_{tot}}{3}\left\{\left[\dfrac{i_L^3(t_1)-i_L^3(t_0)}{V_{DC1}-nV_{DC2}}\right]+\left[\dfrac{i_L^3(t_2)-i_L^3(t_1)}{V_{DC1}}\right]+\left[\dfrac{i_L^3(t_3)-i_L^3(t_2)}{V_{DC1}+nV_{DC2}}\right]-\left[\dfrac{i_L^3(t_0)+i_L^3(t_3)}{nV_{DC2}}\right]\right\}\right]\right)^{1/2}$
RMS voltage	$V_{Lrms(mode6')} = \left(\left[V_{DC1}^2D_1 + (nV_{DC2})^2 D_2 + 2nV_{DC1}V_{DC2}(D_1 - D_2) + 2\lvert D_3\rvert - 1\right]\right)^{1/2}$
Average power & range	$P_{(mode6')} = \dfrac{nV_{DC1}V_{DC2}}{4f_sL_{tot}}\left[D_1^2 + D_2^2 + 2\lvert D_3\rvert^2 - 2D_1 - 2\lvert D_3\rvert + 2D_1\lvert D_3\rvert - 2D_2\lvert D_3\rvert - D_1D_2 + 1\right]$ *Range:* ➡ $\begin{cases} P_{max} = 1pu & (D_1 = 1, D_2 = 1, D_3 = 0.5) \\ P_{min} = 0pu & (D_1 = 0, D_2 = 1, D_3 = 0) \end{cases}$
Reactive power	$Q_{mode6'} = v_{rms(mode6')} \times i_{rms(mode6')}$
ZVS	*Achievable for all switches* **Constraints:** $i_L(t_0)<0, i_L(t_1)<0, i_L(t_2)<0 \,\&\, i_L(t_3)>0$

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