Investigation on the Power Consumption of Digital-Based Analog Amplifiers

Anna Richelli *, Paolo Faustini , Andrea Rosa , Luigi Colalongo

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Article

Investigation on the Power Consumption of Digital-Based Analog Amplifiers

Anna Richelli, Paolo Faustini, Andrea Rosa, Luigi Colalongo [1,‡*]

[1] University of Brescia; name.surname@unibs.it

* Correspondence: anna.richelli@unibs.it; Tel.: +39-030-371-5501

‡ These authors contributed equally to this work.

Abstract: Digital-based differential amplifiers (DDA) are particularly suitable to low voltage digital integrated circuit technologies. This paper presents an exhaustive analysis of the digital-based analog amplifiers to take advantage of today's high-performance digital technologies and of computer-aided design (CAD) commonly employed to design integrated circuits. The operating principle and the main mathematical relations of the digital-based differential amplifiers are discussed along with an exhaustive explanation of its operating regions and of the corresponding power consumption. Finally, a detailed description of the design procedure of in UMC 180nm standard CMOS technology is shown. *Index Terms*—Digital-based amplifiers, analog integrated circuits, amplifiers, ultra-low voltage, ultra-low power.

Keywords: digital-based amplifiers; ultra low power; CMOS integrated circuits

1. Introduction

Ubiquitous electronic requires compact ultra-low power devices and fast prototypization. Technology scaling favors digital circuits thanks to their high speed and low power dissipation. In this context, it is rising the trend of implementing low-voltage inverter-based analog circuits. The elementary inverter-based amplifier is a couple of CMOS digital inverters that operates in an analog fashion due to the common-mode (CM) voltage that keeps both the NMOS and PMOS transistors in the saturation region. The resulting amplifiers have high differential gain, large transconductance, high output resistance, and high gain bandwidth (GBW). The gain of the simple inverter is the ratio of the small signal transconductances and output conductances: $A_v = (g_{mN} + g_{mP})/(g_{dsN} + g_{dsP})$, where g_m is the transconductance and g_{ds} the output conductance. Unfortunately, operating the inverter as an analog amplifier, leads to large variation with temperature and fabrication process of the DC gain and GBW. Furthermore, the higher is the voltage gain, the narrower is the range of the CM. To face these issues several techniques were proposed in the literature, mostly based on common mode feedback (CMFB) circuits, that sense the output CM to control the bias current of the inverter. Indeed, g_{mN}, g_{mP}, and g_{dsN}, g_{dsP} depend on the drain and source voltages and, in turn, on the CM. Therefore, the DC gain can be regulated by changing the CM. In principle, only two resistors are required to extract the CM. The CMFB can be also implemented without resistors as in the Nauta operational transconductance amplifier and its most recent derivations [1]-[5]. Nevertheless, they remain analog circuits in which both the NMOS and PMOS are in saturation, the current flows continuously, and the static power consumption is large. Several approaches, based on current-starved topologies, were suggested in the literature to reduce the power consumption: they are fully differential circuits that need an output common mode voltage feedback to stabilize the small signal performances.
Another approach is to radically re-think analog functions in digital terms to use only digital circuits as, by the way of example, the class D amplifier [6]. VCO-based amplifiers [7], voltage to time converters [8], digital.-to-analog converters [9], hybrid analog-digital amplifiers [10] and digital-based amplifiers [11] - [19] are reported in the literature. In [11]-[19] a differential amplifier, composed of logic gates only, is shown. It has several appealing features: low power consumption, small area, easy design, and fast prototyping. It is an interesting approach and a deep understanding of the possible topologies,

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design, features, and limits is important for analog-background designers that, habitually, use different design methodologies. This paper is focused on the understanding of the DDA both from a circuital and mathematical standpoint with particular emphasis on the power consumption that is one of its main appealing features. In section II, the operating principles, the transistors operating conditions, and the main mathematical relations to design the DDA are devised. In section III, the full design of the amplifier in 180nm CMOS standard is shown, along with a comprehensive explanation of the operating regions and power consumption. In section IV, some conclusions are drawn.

2. Operating Principle of the DDA

In Figure 1 the building blocks of the DDA are shown [11]. The output of the digital buffers ($OUT+, OUT-$) is high (H) when the input voltages v_{i+}, v_{i-} are larger than the threshold voltage (V_M) and low (L) when are lower than V_M. The CMFB (green box) adjusts the CM voltage v_{CM} in order to emulate the input stage of a differential amplifier. Hence, ($OUT+, OUT-$) are related to the differential voltage $v_D = v_{i+} - v_{i-}$. A detailed description of the DDA, along with the basic mathematical relations, are reported in [11]. For the sake of clarity, here we recall: $v_{CM} = (v_{i+} + v_{i-})/2$, $v_{i\pm} = v_{CM} \pm v_D/2$ and, using a balanced resistor network, $v'_{i\pm} = (v_{i\pm} + v_{CM})/2$.

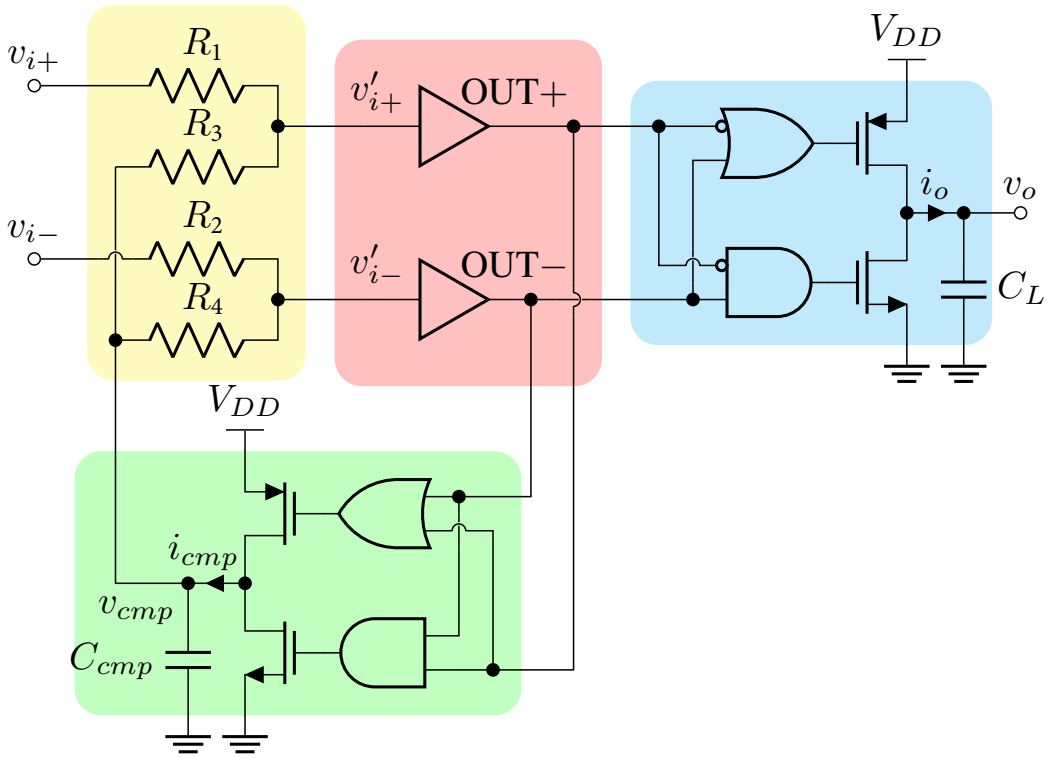

Figure 1. Digital-based amplifier [11], resistor network (yellow box), digital buffers (pink box), blue box (output stage), CMFB (green box). $R_1 = R_2 = R_3 = R_4 = R$

Since the logic gates are assumed to switch much faster than the input signals of the DDA, the output and CMFB voltages v_o e v_{cmp} are well approximated by the following first order differential equations:

$$\frac{dv_o(t)}{dt} = \frac{i_o(t)}{C_L}, \quad \frac{dv_{cmp}(t)}{dt} = \frac{i_{cmp}(t)}{C_{cmp}} \tag{1}$$

where $i_o(t) = \{\, i_o^{pmos}$ if $[v'_{i+}(t_1) > V_M] \wedge [v'_{i-}(t_1) < V_M]$, $-i_o^{nmos}$ if $[v'_{i+}(t_1) < V_M] \wedge [v'_{i-}(t_1) > V_M]$, 0 elsewhere $\}$, $i_{cmp} = \{\, i_{cmp}^{pmos}$ if $[v'_{i+}(t_2) < V_M] \wedge [v'_{i-}(t_2) < V_M]$, $-i_{cmp}^{nmos}$ if $[v'_{i+}(t_2) > V_M] \wedge [v'_{i-}(t_2) > V_M]$, 0 elsewhere $\}$, $t_1 = t - t_{D,o}$, $t_2 = t - t_{D,cmp}$ and $t_{D,o}$ and $t_{D,cmp}$ represent the propagation time through the logic gates. Furthermore, for the sake of simplicity, the logic gates are assumed ideal with

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the same propagation time $t_D = t_{D,o} = t_{D,cmp}$, and $i_o^{pmos} = i_o^{nmos} = I_o$, $i_{cmp}^{pmos} = i_{cmp}^{nmos} = I_{cmp}$ constant and not depending on v_o and v_{cmp}. Under those assumptions, in the following, the two possible operating conditions $v_D = 0$ and $v_D \neq 0$, will be discussed.
In Figure 2, the waveforms when $v_D = 0$ are shown. When $v_D = 0$, $OUT+$, $OUT-$ are the same, the output inverter is in high impedance, v_o is constant and the load capacitor C_L holds its charge. Nevertheless, the compensation voltage v_{cmp} oscillates, in fact:

- At $t = 0$ both v'_{i+} and v'_{i-} cross V_M, and $OUT+$, $OUT-$ switch from L to H. It takes a certain amount of time t_D for the signal to propagate through the CMFB.
- Before t_D, although $OUT+$, $OUT-$ are high, the CM compensation inverter has not yet changed its state, and C_{cmp} is still charging with I_{cmp} as when $t = 0$.
- At $t = t_D$, the CMFB changes its state: the pull-down switches on, and the capacitor C_{cmp} is discharged with a constant current $-I_{cmp}$.
- From t_D to $2t_D$, while C_{cmp} is discharging, both v'_{i+} and v'_{i-} fall below the threshold V_M.
- At $2t_D$, $OUT+$, $OUT-$ switch from H to L;
- Before $3t_D$ the CM compensation inverter has not yet changed its state and C_{cmp} is still discharging.
- At $3t_D$ the CM compensation inverter changes state, the pull-up switches on, and the capacitor C_{cmp} is charged with the current I_{cmp}.
- This cycle is repeated every $T_{cmp} = 4t_D$.

Hence, the delay introduced by the compensation network t_D induces a triangular wave oscillation on v_{cmp} of period $4t_D$ and peak-to-peak amplitude $v_{cmp,pp} = 2t_D\, I_{cmp}/C_{cmp}$.

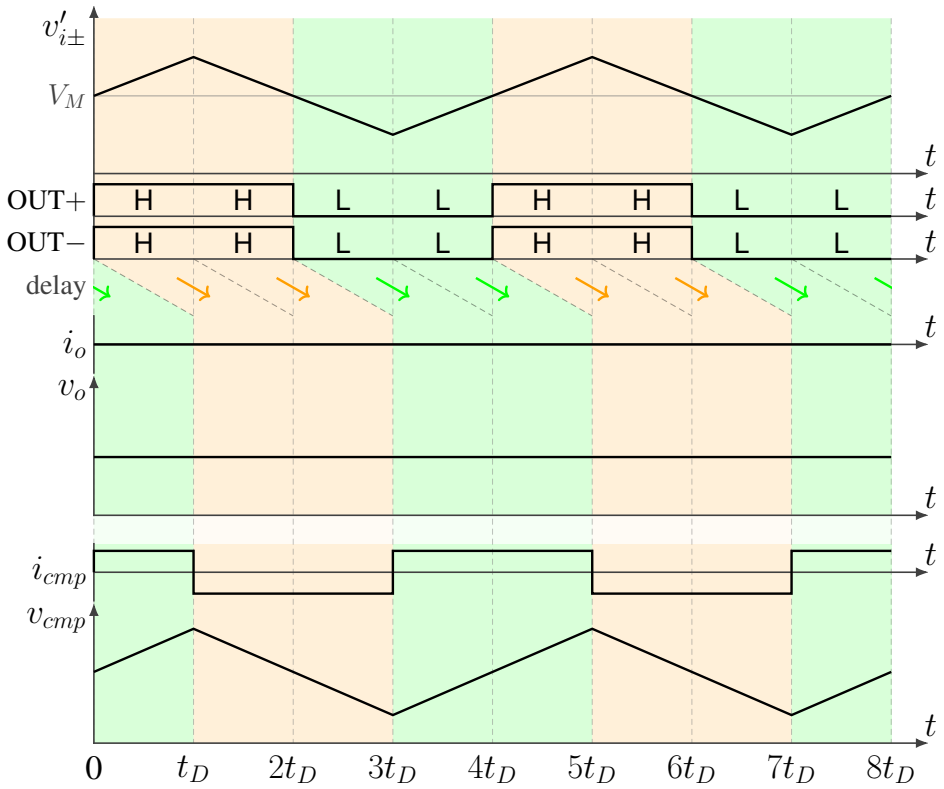

Figure 2. Waveforms of the DDA at $v_D = 0$.

In Figure 3, the waveforms when $v_D > 0$ are shown, similar considerations hold when $v_D < 0$.

- The differential voltage v_D corresponds to a small mismatch between v'_{i+} and v'_{i-} that, in turn, causes v'_{i-} to cross the threshold voltage V_M with a small delay Δt_C; during Δt_C, the differential

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voltage is positive, $v'_{i+} > v'_{i-}$, and the outputs $(OUT+, OUT-) = (1, 0)$. After $2t_D$, it is v'_{i+}, that crosses the threshold voltage V_M with a small delay Δt_C respect to v'_{i-}.

- v_{cmp} is a triangular wave with the same period $T_{cmp} = 4t_D$, as in Figure 2 but, during the interval Δt_C, the voltage is clamped since the buffer is in the high impedance region.
- During the interval Δt_C, the output buffer charges C_L and v_o steps up of $I_o\,\Delta t_C/C_L$.
- The charge on C_L is incremented by $I_o\,\Delta t_C$, twice every $T_{cmp} = 4t_D$.

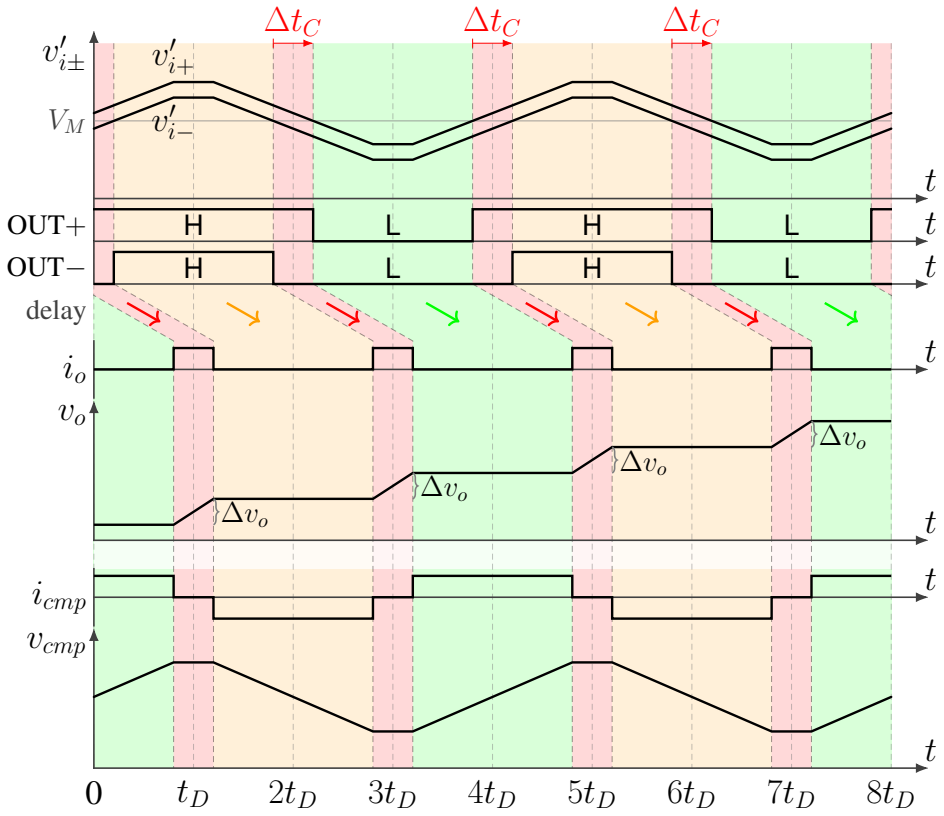

Figure 3. Waveforms of the DDA at $v_D > 0$.

In other words, the DDA operates as a double conversion from voltage to time and back from time to voltage again. The first conversion is v_D to Δt_C, thanks to the oscillation on v_{cmp}. Indeed, the mismatch on v'_{i+} and v'_{i-} is converted into a delay Δt_C, i.e. a time. Then, the output buffer converts the delay Δt_C back into a voltage $\Delta v_o = I_o \Delta t_C / C_L$. The voltage gain of the DDA in the frequency domain, assuming only the capacitive load C_L, reads:

$$A_D(f) = \frac{G_D(f)}{j2\pi f C_L} = \frac{\alpha}{j2\pi f\, 2t_D}\, e^{-j2\pi f t_D} \tag{2}$$

where $\alpha = I_o/C_L$,

$$G_D(f) = \frac{I_o(f)}{V_D(f)} \approx \frac{I_o}{2t_D}\,\frac{C_{cmp}}{I_{cmp}}\, e^{-j2\pi f t_D} \tag{3}$$

and $e^{-j2\pi f t_D}$ is the phase shift due to the propagation delay t_D. Furthermore, when $f \ll f_c/2$, eq. (2) can be simplified as $A_D(f) \approx \alpha/(j2\pi f\, 2t_D)$. Thus, the transfer function is equivalent to an integrator with a unity gain frequency of $f_u = \alpha/(4\pi t_D)$. The digital-based analog amplifier can be used, almost as conventional analog amplifiers, in feedback loops. Nevertheless, the classical assumptions of infinite

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input impedance ($Z_i \to \infty$) and negligible output impedance ($Z_o \to 0$) are not properly verified. The transfer function can be approximated as:

$$G(f) = \frac{V_o(f)}{V_i(f)} = \frac{1/\beta}{1 + j2\pi f/(\beta f_u)} \tag{4}$$

where β is the gain of the feedback network set by the resistors' ratio. In other words, the DDA operates as a first order system.

3. Design and Simulations of the DDA

The digital-based amplifier discussed in the previous section has been designed in the standard 180nm UMC (United Microelectronic Corporation) CMOS process and extensively simulated in different operating conditions. It is worth noting that the final schematic is slightly modified with respect to the base circuit of Figure 1 to equalize the propagation time of $OUT+$ and $OUT-$.The circuit is extremely simple, composed only of resistors and logic gates. The supply voltage is standard for this technology (1.8V) at the aim of investigate the DDA in normal operating conditions. Several simulations worked out at lower supply voltages show that the DDA operates correctly at supply as low as 400mV.

3.1. Sizing of the DDA in UMC 180 nm CMOS Process

The first step is to dimension the CMOS inverter with a logic threshold V_M half of V_{DD}. Considering the different transistor's threshold $V_{Tn,Tp}$ and mobility $\mu_{n,p}$, the ratio of the PMOS and NMOS, to maximize the symmetry of the inverter, results of 4.725. Minimum transistors are chosen to minimize the gate capacitance: $L_{n,p} = 180$nm, $W_n = 240$nm and $W_p = 1134$nm. The NOR logic gate is composed of two PMOS connected in series and two NMOS in parallel. To have a symmetric behavior both the transistors of the pull-up and pull-down read: $L_{n,p} = 180$nm, $W_n = 240$nm and $W_p = 2268$nm. Dual considerations hold for the NAND that comprises two PMOS in parallel and two NMOS in series: $L_{n,p} = 180$nm, $W_n = 480$nm and $W_p = 1134$nm. The input resistors R1-R4, on the one hand, should be large to have a high input impedance, on the other hand should be not too large to limit the area consumption and the thermal noise. Although same resistances of 145kΩ were chosen to have an input differential impedance of 580kΩ, in the layout $R_1 - R_4$ were slightly modified to have true rail-to-rail common mode: $R_{1,2}$ = 140kΩ and $R_{3,4}$ = 150kΩ. The output and the CMFB are dimensioned to balance the propagation delay between the logic gates. The dimensions of the output stage are: $L_{n,p} = 180$nm, $W_n = 5\mu$m and $W_p = 10\mu$m. And for the inverter of the CMFB is: $L_{n,p} = 180$nm, $W_n = 240$nm and $W_p = 720$nm. All the dimensions are in agreement to the technology minimum grid.

3.2. Simulation Results

The DDA can hardly be simulated by means of the classical small-signal AC analysis tools since the core of its operating principle is digital and is related to the oscillation of v_{cmp}. Time-expensive transient analysis are required to design and characterize the amplifier. The DDA was simulated in two different configurations: open loop as a comparator, and closed loop as a feedback amplifier.

3.2.1. Open Loop

The amplifier is operated as a comparator. In the simulations, to generate a modulated differential voltage v_D that emphasizes all the different operating regions of the amplifier, we used two input sinusoidal signals v_{i+} and v_{i-} of amplitude V_{DD} with different frequencies: v_{i+} 10kHz, v_{i-} 30kHz. The transient simulation time is 100μs. The waveforms of the most relevant voltages of the internal nodes are shown in Figure 4: the bottom x-axis represents the simulation time, the top x-axis the operating

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regions, the y-axis the voltages at the nodes. In Figure 5, one can see that the DDA has five distinct behaviors and power consumption that we call operating regions 1-5:

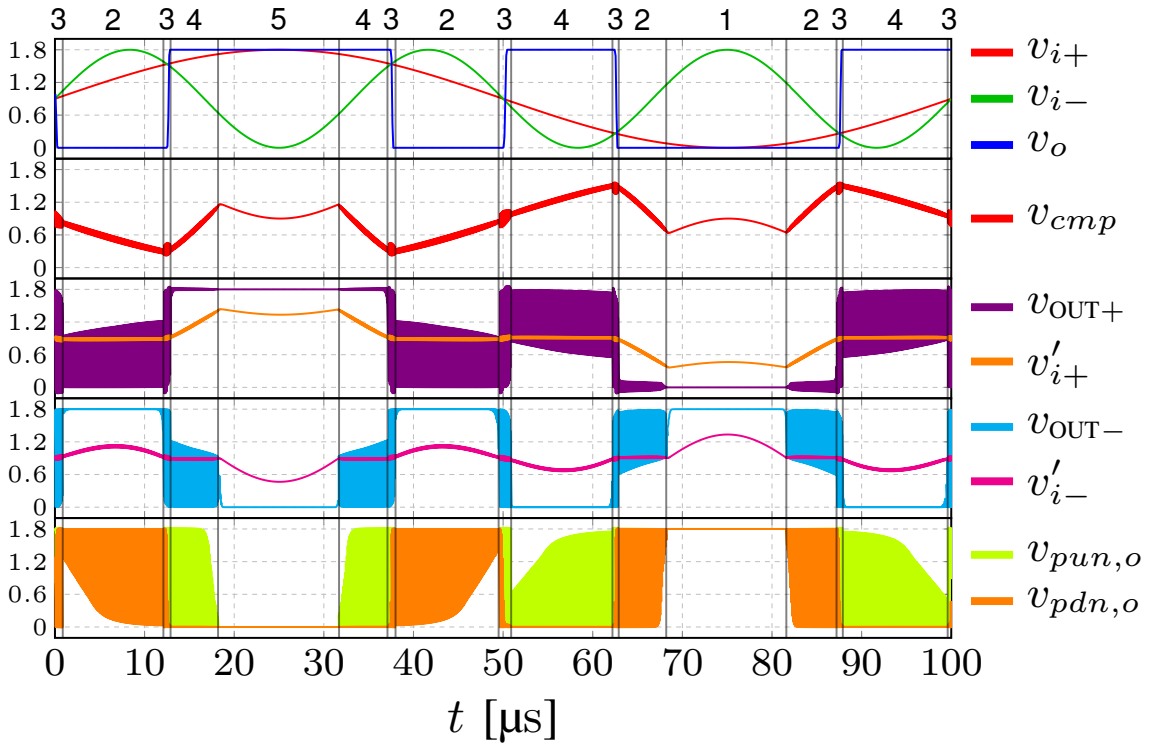

Figure 4. Open loop: input/output waveforms and intermediate node voltages

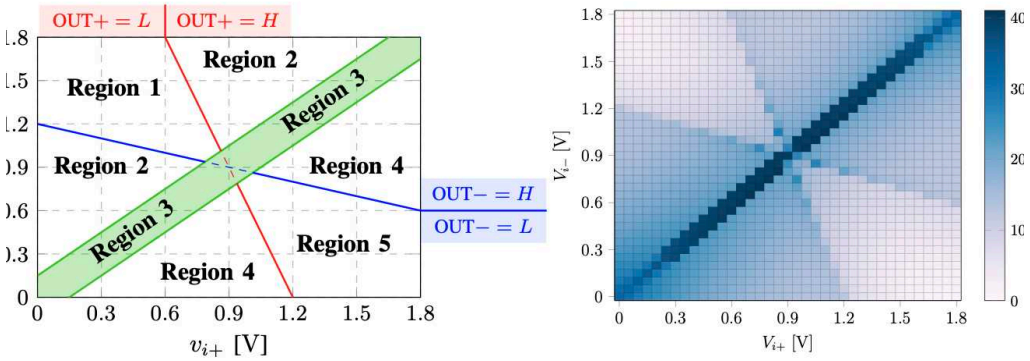

Figure 5. Open loop: operating regions vs. $v_{i\pm}$ and power consumption

- In the regions 1 and 5, the differential voltage v_D is large, $v_{i\pm}$ are well separated and opposite with respect to the logic threshold V_M. In these regions the output voltage saturates to V_{DD} or 0, the common-mode compensation network is not active and only the pull-up or the pull-down of output inverter turns on. In Figure 4, $v_{pun,o}$, $v_{pdn,o}$ are the gate voltages of the pull-up and pull-down respectively. In Figure 5, the regions 1 and 5 are limited by the equations $|v'_{i+}| < V_M$ and $|v'_{i-}| > V_M$:

$$v'_{i+} = \frac{v_{i+}\,R_3 + v_{cmp}\,R_1}{R_1 + R_3} \tag{5}$$

$$v'_{i-} = \frac{v_{i-}\,R_4 + v_{cmp}\,R_2}{R_2 + R_4} \tag{6}$$

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Furthermore, since the CMFB is not active $v_{cmp} = v_{CM}$, i.e. $(v_{i+} + v_{i-})/2$, the regions 1 and 5 reads:

$$v'_{i+} = \frac{v_{i+} + v_{CM}}{2} = \frac{3}{4} v_{i+} + \frac{1}{4} v_{i-} \tag{7}$$

$$v'_{i-} = \frac{v_{i-} + v_{CM}}{2} = \frac{1}{4} v_{i+} + \frac{3}{4} v_{i-} \tag{8}$$

- In the region 3, the differential voltage v_D is small enough to activate the CMFB. The compensation voltage v_{cmp} oscillates and the digital outputs $OUT+$ and $OUT-$ commute between L and H. Both the pull-up and the pull-down of the output inverter are active: if v_D is positive, v_o steps up, if v_D is negative, v_o steps down. This region is defined by the condition $\Delta t_C < t_D$ i.e. $v_D < I_{cmp}/C_{cmp}\, t_D$
- In the regions 2 and 4, the differential voltage v_D is small, but not as small as in the region 3. In the region 2 $v_D < 0$, $OUT+$ holds the low logic state, while $OUT-$ quickly commutes from H to L due to the CMFB. The pull-down of the output stage switches on. In the region 4 $v_D > 0$, $OUT-$ holds the low logic state, while $OUT+$ quickly commutes from H to L due to the CMFB. The pull-up of the output stage switches on. Hence, the pull-up or the pull-down switches on, but are not always active as in region 1 and 5.

The power consumption of the DDA is mostly dynamic and is due to the switching of the gates (P_{gates}), to the charging and discharging of C_{cmp} (P_{cmp}) and C_L (P_o). It strongly depends on the operating regions of the amplifier as shown in Figure 5: the dissipated power, as a function of the differential voltage, is represented as a shade of blue from light (lower power consumption) to dark (higher power consumption). The x- and the y-axis are the input voltages $v_{i\pm}$, ranging from 0 to V_{DD} in steps of 50mV. It is worth adding, that the simulations are worked out at 1.8V (standard for this technology): if the voltage supply is reduced, the power consumption gets remarkably smaller, [13]-[16]. This is due both to the dependence of the dynamic power on V_{DD} and to the reduction of the switching frequencies of the CMFB and of the output stage. In the regions 1 and 5, the power dissipation is lower than in the region 2, 3, 4, since the common mode compensation network is always switched off, only the pull-up or pull-down is conducting, and the output voltage saturates to V_{DD} or 0. In the regions 2 and 4 the power dissipation is higher since the CMFB is active. Finally in the region 3 the power consumption reaches its maximum since the differential voltage is small and v_{cmp} oscillates continuously.

3.2.2. Closed Loop

The DDA can be used in feedback connection as an analog amplifier. In the simulations of the closed loop connection a sinusoidal rail-to-rail input signal of 20kHz is applied to the non-inverting input v_{i+}. The simulation time is 100μs. The Fast Fourier Transform (FFT) of the buffer connection with unitary loop gain (G) is 0.992, the phase delay (φ) 0.08^o, and a total harmonic distortion (THD) 0.23%. Figure 6 show that, when the DDA is used as a buffer, the differential voltage v_D is very small and always operates in the region 3. Hence, despite the rather good overall performances, the power consumption reaches its maximum.

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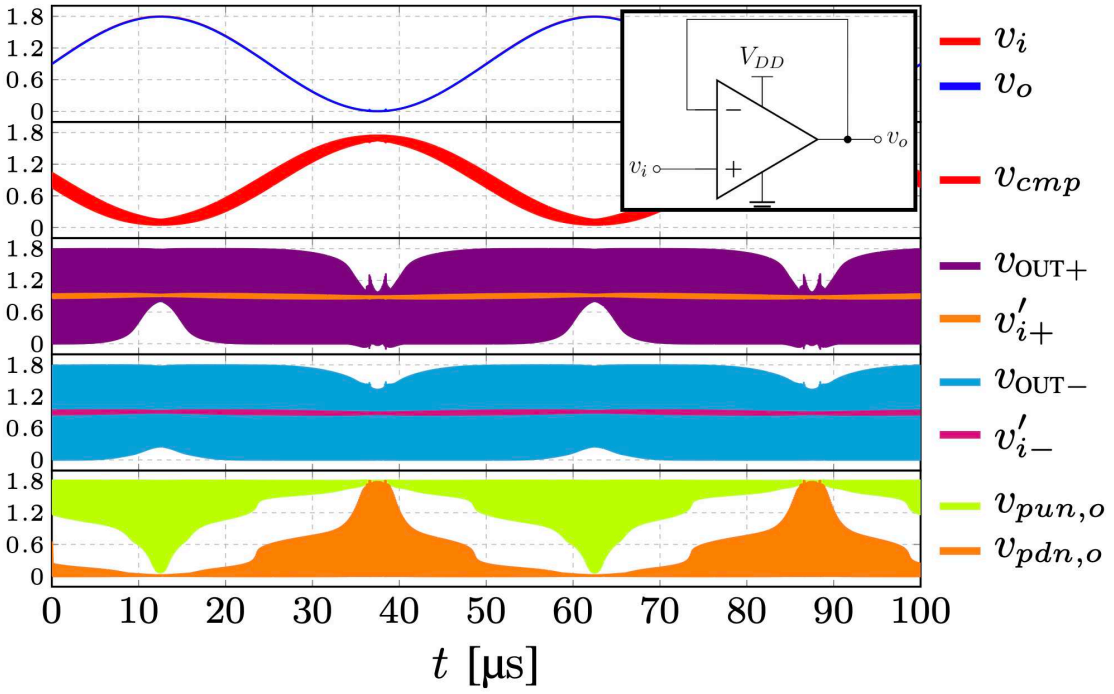

Figure 6. Buffer: input/output waveforms and internal node voltages

Furthermore, the closed loop configuration was simulated in several other configurations. Figure 7 shows the simulations in three different configurations: buffer (G=0.987, φ=0.14^o, THD=0.31%), inverter (G=-0.938, φ=0.06^o, THD=1.58%), and gain two (G=2.007, φ=0.06^o, THD=0.99%). The results are shown in Figure 7. Simulations are worked out with an input signal of 400mVp and a frequency of 20kHz. The voltage gain G and the output voltage v_o are close to the ideal ones while the largest THD is smaller than 1.6%, the phase delay is below 0.14^o, and the larger offset 33.7 mV only.

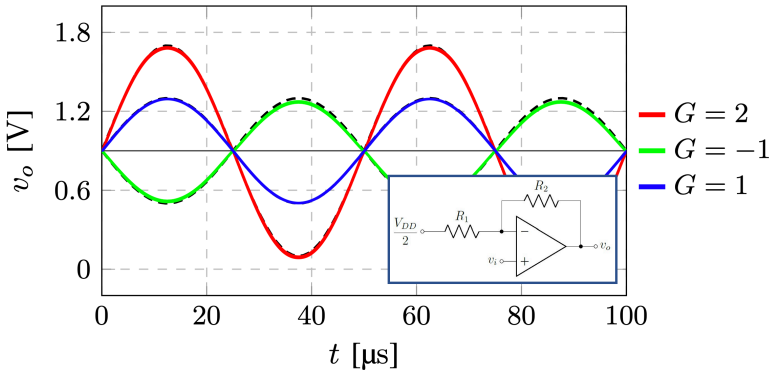

Figure 7. Closed loop simulations

Finally, the closed loop amplifier is simulated with rail-to-rail input voltages at several frequencies. In Figure 8 (A) the FFT in the range of 100kHz-100MHz is shown.

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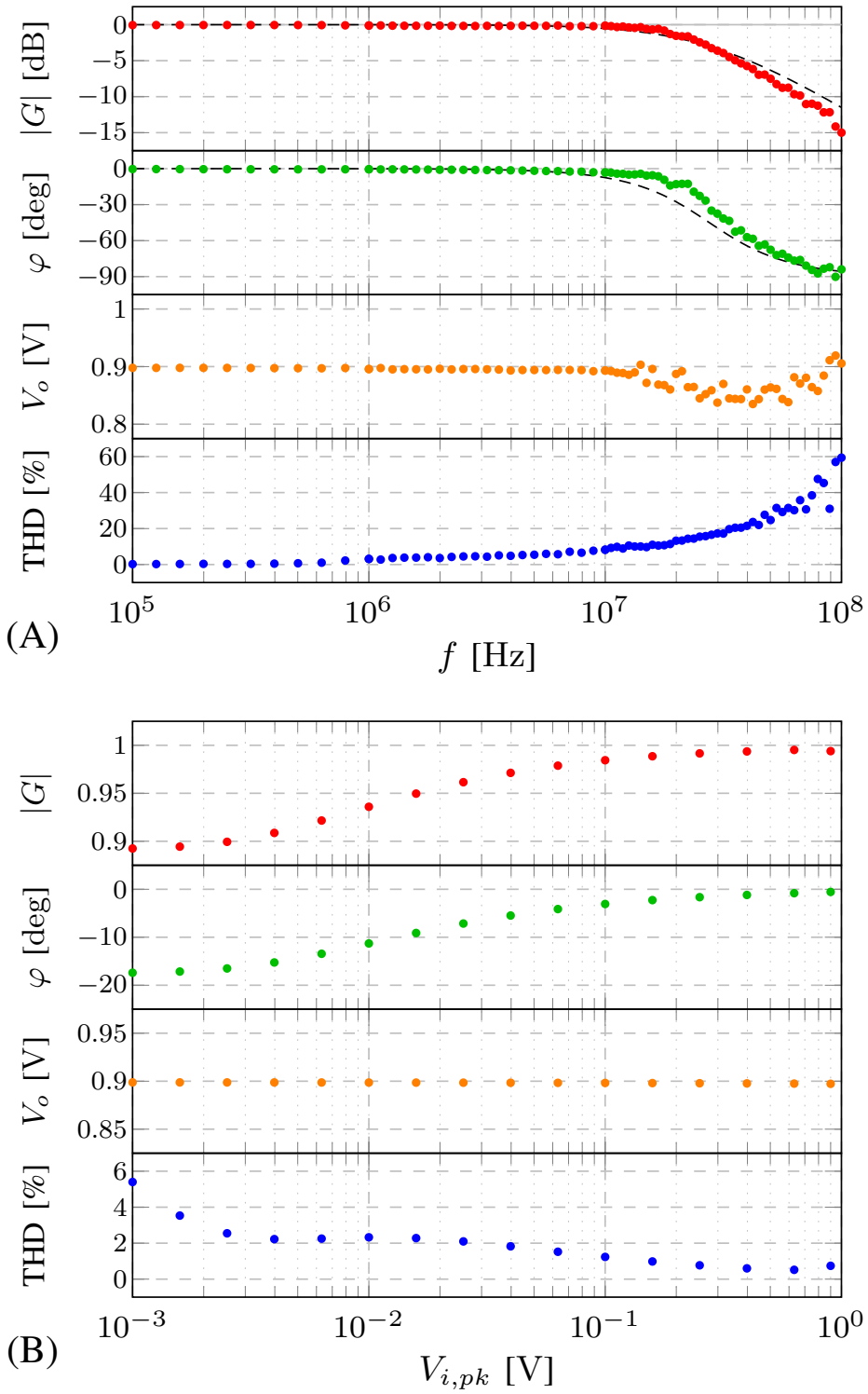

Figure 8. Buffer: G, φ, output voltage, and THD as a function of frequency (A), and of the input signal amplitude (B)

The amplifier act as a single pole dominant system with a unity gain frequency of about 27.6MHz. The output voltage v_o (gain and phase) is almost ideal up to 10MHz, while the THD starts rising at a lower frequency: about 1MHz. It is worth stressing that simulations are worked out at 1.8V. Nevertheless, one of the most appealing feature of the DDA is the small power consumption and lower V_{DD} are often used: in that case, the overall performance degrades rather quickly. Finally, simulations were worked out by changing the amplitude of the input voltage at constant frequency

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(500kHz), i.e. within the bandwidth of the amplifier. The results are shown in Figure 8 (B), for an input signal ranging from 1mV up to 900mV. One can see that the DDA works very well when the amplitude of the input signal is large enough and slightly deteriorates as input voltage gets lower and lower. The resistive compensation network, in fact, limits the input impedance of the amplifier. In several applications, such as biomedical, wearable, IoT and sensoring, these limits do not represent a real drawback, and the DDA is a very promising architecture. High frequencies or low input signals represent the most important limit of the DDA that require some adjustments. To this aim, a more recent DDA architecture [16], [19] with a new compensation network based on floating inverters, was reported. Thanks to this new common mode compensation circuit, the DDA in [16], [19] can amplify low amplitude signals with very good overall performances.

4. Conclusions

The digital-based analog amplifier was designed and investigated along with its main mathematical relations. We have shown that the amplifier can operate in 5 different regions and that the power consumption peaks when v_D is small. Several simulations were worked out both in the open and closed loop configuration. The simulations show that the amplifier represents a really attractive approach for the signal conditioning of the integrated circuits with advantages on power consumption and ease of design. The amplifier is better suited for low to medium frequency input signals with rather large amplitude. Nevertheless, it represent a very appealing architecture when the area on chip and the power dissipation are of paramount importance.

Author Contributions: All the authors have contributed substantially to the paper. Anna Richelli, Luigi Colalongo have supervised the work, have provided the simulation tools and have written the paper; Paolo Faustini is graduated-five years Laurea degree- student and Andrea Rosa is PhD student, they have investigated on the power consumption of the amplifier and performed the simulations.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

DDA	Digital-based Differential Amplifier
CAD	Computer-aided Design
UMC	United Microelectronics Corporation
CMOS	Complementary Metal Oxide Semiconductor
CM	Common Mode
GBW	Gain Bandwidth
CMFB	Common Mode Feedback
DC	Direct Coupling
VCO	Voltage Controlled Oscillator
FFT	Fast Fourier Transform
G	Loop Gain
THD	Total Harmonic Distortion
IoT	Internet of Things

References

1. B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, Feb. 1992.
2. Rodovalho, L.H.; Toledo, P.; Mir, F.; Ebrahimi, F. Hybrid "Inverter-Based Fully Differential Operational Transconductance Amplifiers", Chips 2023, 2, 1-19.
3. A. P. Nicholson, A. Iberzanov, J. Jenkins, T. J. Hamilton and T. Lehmann, "A Statistical Design Approach for a Digitally Programmable Mismatch-Tolerant High-Speed Nauta Structure Differential OTA in 65-nm

CMOS," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 9, pp. 2899-2910, Sept. 2016.

4. Manfredini, G.; Catania, A.; Benvenuti, L.; Cicalini, M.; Piotto, M.; Bruschi, P. "Ultra-Low-Voltage Inverter-Based Amplifier with Novel Common-Mode Stabilization Loop", Electronics 2020, 9.
5. J. Wei, Y. Yao, L. Luo, S. Ma, F. Ye and J. Ren, "A Novel Nauta Transconductor for Ultra-Wideband gm-C Filter with Temperature Calibration," *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, 2019.
6. F. Guanziroli, R. Bassoli, C. Crippa, D. Devecchi, and G. Nicollini, "A 1 W 104 dB SNR filter-less fully-digital open-loop class D audio amplifier with EMI reduction," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 3, Mar. 2012.
7. S. Kalani, A. Bertolini, A. Richelli and P. R. Kinget, "A 0.2V 492nW VCO-based OTA with 60kHz UGB and 207 μVrms noise," *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, USA, 2017.
8. A. Richelli, L. Colalongo, Zs. M. Kovacs-Vajna, "EMI Effect in Voltage-to-Time Converters", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 8, No. 4, Apr. 2021.
9. R. Rubino, F. Musolino, Y. Chen, A. Richelli and P. Crovetti, "A 880 nW, 100 kS/s, 13 bit Differential Relaxation-DAC in 180 nm," 2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Valencia, Spain, 2023, pp. 269-272.
10. M. Privitera, P. S. Crovetti and A. D. Grasso, "A novel Digital OTA topology with 66-dB DC Gain and 12.3-kHz Bandwidth," in IEEE Transactions on Circuits and Systems II: Express Briefs, doi: 10.1109/TCSII.2023.3283566.
11. P. Crovetti, "A digital-based analog differential circuit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 12, Dec. 2013.
12. Palumbo, G.; Scotti, G. "A Novel Standard-Cell-Based Implementation of the Digital OTA Suitable for Automatic Place and Route", J. Low Power Electron. Appl. 2021, 11, 42.
13. P. Toledo, P. Crovetti, O. Aiello and M. Alioto, "Fully Digital Rail-to-Rail OTA With Sub-1000-μm2 Area, 250-mV Minimum Supply, and nW Power at 150-pF Load in 180 nm," in IEEE Solid-State Circuits Letters, vol. 3, pp. 474-477, 2020.
14. P. Toledo, P. Crovetti, O. Aiello and M. Alioto, "Design of Digital OTAs With Operation Down to 0.3 V and nW Power for Direct Harvesting," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 9, pp. 3693-3706, Sept. 2021.
15. P. Toledo, P. Crovetti, H. Klimach, S. Bampi, O. Aiello and M. Alioto, "A 300mV-Supply, Sub-nW-Power Digital-Based Operational Transconductance Amplifier," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 9, pp. 3073-3077, Sept. 2021.
16. P. Toledo, P. S. Crovetti, H. D. Klimach, F. Musolino and S. Bampi, "Low-Voltage, Low-Area, nW-Power CMOS Digital-Based Biosignal Amplifier," in IEEE Access, vol. 10, pp. 44106-44115, 2022.
17. P. Toledo, O. Aiello and P. S. Crovetti, "A 300mV-Supply Standard-Cell-Based OTA with Digital PWM Offset Calibration," 2019 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), Helsinki, Finland, 2019.
18. P. Toledo, P. Crovetti, H. Klimach and S. Bampi, "A 300mV-Supply, 2nW-Power, 80pF-Load CMOS Digital-Based OTA for IoT Interfaces," 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Genoa, Italy, 2019, pp. 170-173.
19. R. Rubino, S. Carrara and P. Crovetti, "Direct Digital Sensing Potentiostat targeting Body-Dust," *2022 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Taipei, Taiwan, 2022.