An Analytical Model of Dynamic Power Losses in eGaN HEMT Power Devices

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Article

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Abstract: In this work, we present an analytical model of dynamic power losses for enhancement-mode AlGaN/GaN high-electron-mobility transistor power devices (eGaN HEMTs). To build this new model, the dynamic on-resistance (R_{dson}) is first accurately extracted by our extraction circuit based on a double-diode isolation (DDI) method for a high operating frequency up to 1 MHz and a large drain voltage up to 600 V, thus the unique problem of an increase in the dynamic R_{dson} is presented. Then the impact of the current operation mode on the on/off transition time is evaluated by a dual-pulse-current-mode test (DPCT) which including a discontinuous conduction mode (DCM) and a continuous conduction mode (CCM), thus the transition time is revised for different current mode. Afterward the discrepancy between the drain current and the real channel current is qualitative investigated by an external shunt capacitance (ESC) method, thus the losses due to device parasitic capacitance are also taken into account. After these improvements, the dynamic model will be more compatible for eGaN HEMTs. Finally, the dynamic power losses calculated by this model are verified to be in good agreement with experimental results. Based on this model, we propose a superior solution with quasi-resonant mode (QRM) to achieve lossless switching and accelerate switching speed.

Keywords: AlGaN/GaN HEMT device; CCM; DCM; dynamic on-resistance; dynamic power loss

1. Introduction

Enhancement-mode AlGaN/GaN high electron mobility transistor power devices (eGaN HEMTs) are the most promising candidates for next-generation power devices. In such devices, III-V materials have several merits due to their wide bandgap energy, high critical breakdown electric field, high electron mobility and capability [1,2], and polarization effect [3]. Because of these advantages, a high-frequency (high-fs) converter operating in the range of 1-5 MHz based on eGaN HEMTs can be readily realized. Although high-fs operation can help reduce converter size, it will generate more challenges with respect to dynamic power loss. Thus, building an analytical dynamic power loss model for an eGaN-based high- fs switch becomes important for prototype application circuit design.

Recently, some state-of-the-art dynamic power loss models for eGaN HEMTs have been proposed. Wang et al. developed two analytical loss models based on detailed parasitic parameters for high-voltage and low-voltage GaN eHEMTs [4,5]. In these models, the gate charge (Q_g) and output charge (Q_{oss}) instead of the voltage-dependent capacitance were used to improve the nonlinear characteristics. Shen et al. fully accounted for the effects of parasitic parameters and transconductance [6]. Hou et al. and Guacci et al. investigated the losses caused by output capacitance in a hard switch and soft switch, respectively [7,8]. However, these models did take into account the impact on device loss from some aspects instead of fully evaluated, the results accuracy is affected.

Chen et al. presented a complete analytical loss model for low-voltage eGaN HEMTs, which a piecewise model was employed [9]. Piecewise models are also usually used to evaluate the dynamic

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power losses for Si- and SiC-based metal-oxide-semiconductor field-effect transistors (MOSFETs) [10–15]. These models are carefully considered and allow accurate evaluation of device power losses. However, these models did not take into account the exclusive dynamic physical characteristics of eGaN HEMTs, such as a strong defect trapping-effect, increased dynamic on-resistance (R_{dson}), and no reverse body diode. Therefore, these analytical models need to be modified for eGaN HEMTs. In addition, the effect of current operation mode on device transition time and loss is not considered in all known device loss models.

To improve the dynamic power loss model of eGaN HEMTs, we propose three experimental methods according to the practical application of devices in high-fs circuits, such as a double-diode isolation (DDI) method, a dual-pulse-current-mode test (DPCT) method, and an external shunt capacitance (ESC) method. Then, the dynamic R_{dson} is accurately extracted in a high operating frequency (fs) up to 1 MHz and a high drain voltage up to 600 V; the effect of current operation mode on transition time is revealed for the first time and thus the loss of the device is affected; and the real channel current (Ich) is qualitative modified compared to the drain current (I_{drain}) we can directly test in device drain side. Afterward the dynamic power loss of eGaN HEMTs is carefully described by a modified 12-segment piecewise model. Finally, we propose a quasi-resonant mode (QRM) with a low off-state drain voltage (V_{ds_off}), zero turn-on current, and a relatively large on-state peak current for a lossless design and fast transit speed in power switches.

2. Background And Methodology

2.1. A. Parameters and Traditional Power Loss Model

V_{gs} : gate voltage.

V_{drive_H} : gate voltage in high level.

V_{drive_L} : gate voltage in low level.

V_{mr} : Miller gate voltages during the turn-on transition.

V_{mf} : Miller gate voltages during the turn-off transition.

V_{th} : threshold voltage.

t_{on} : total turn-on time during the turn-on transition.

t_{dr} : turn-on delay time.

t_{cr} : turn-on current rise time.

t_{vf} : turn-on voltage fall time.

t_{mr} : turn-on Miller rise time.

t_{gr} : turn-on gate voltage rise remaining time.

t_{off} : total turn-off time during the turn-off transition.

t_{df} : turn-off delay time.

t_{mf} : Miller fall time.

t_{vr} : voltage rise time.

t_{cf} : current fall time.

t_{vr} : voltage continuous rise time.

Q_{gs} : gate-source charge.

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Q_{gd} : gate-drain charge.

Q_{od} : overcharge gate charge.

Q_g : total gate charge, equal to the sum of Q_{gs}, Q_{gd}, and Q_{od}.

I_{ds} : drain-source current.

I_{sta} : start drain-source current at turn-on transition.

I_{pk} : peak drain-source current during on-state.

V_{ds} : drain-source voltage.

In the piecewise model, the operating sequence of the device is shown in Figure 1. In particular, the device is usually connected to a choke or a transformer in power switches, thus the value of I_{sta} indicate the current mode of device. (I_{sta}=0) denotes the device operate in discontinuous conduction mode (DCM), while (I_{sta}>0) denotes the device operate in continuous conduction mode (CCM).

A traditional calculation formula for high-f_s power losses of device is given by [16]

$$P_{sw}=\frac{1}{2}I_{ds}V_{ds}(t_{on}+t_{off})f_s+\frac{1}{2}C_{oss}{V_{ds}}^2 f_s+K_{th}{I_{dson\_rms}}^2 R_{dson}+Q_g V_{gs} f_s \quad (1)$$

where I_{dson_rms} is the on-state drain-source current in root-mean-square (RMS) value, K_{th} is the temperature coefficients related to R_{dson}. The first term in Eq. (1) occurs in the crossing area of I_{ds} and the V_{ds}, while the second term is the output capacitor energy dissipated in the device during the turn-on transition. Then, the third and fourth terms are the conductive loss and driving loss, respectively. Equation (1) is approximate, as it does not take into account the problem of a dynamic R_{dson} increase, the impact of I_{drain} on the transition time, and the discrepancy between I_{drain} and the real channel current.

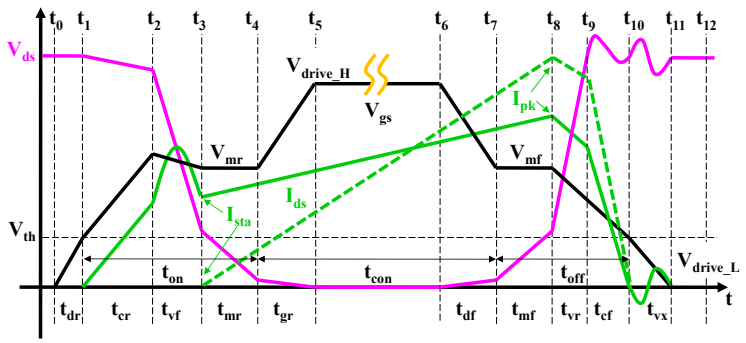

Figure 1. Piecewise timing diagram of the power switching devices.

2.2. B. Experimental Circuit and Method

A switching circuit with a floating buck-boost topology is employed to analyze the switching processes, as shown in Figure 1a. In this circuit, an HEMT device is used and shown with a simple three-capacitor model that includes the parasitic capacitors C_{gs}, C_{gd} and C_{ds}. The pulse width modulation (PWM) is produced by a pulse generator (81150A, Keysight Inc.) with a maximum PWM of 120 MHz, and is amplified by a gate driver (SI8271GB), which has a 1.8 A peak source current and a 4.0 A peak sink current, D_1 is selected as a SiC diode (C3D10065E) rated at 15 A / 650 V, which is used to reduce the reverse recovery problem. The parasitic resistor and parasitic inductor are ignored to simply study the important role of the parasitic capacitors at a relatively high-f_s that is smaller than 30 MHz. Then, various voltages and PWM in DCM and CCM are applied to elucidate the switching processes and the production of dynamic power losses.

Figure 1b shows our novel dynamic R_{dson} extraction circuit [17]. In this design, the model of the gate driver is SI8271GB, and D_1 and D_2 (1 A/1k V UF4007) are used in series to isolate the high off-

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state voltage of the eGaN HEMTs. Then, the dynamic R_{dson} of the eGaN HEMTs can be easily extracted. Diodes in series make it possible to test the real-time forward voltage drop (V_F) of D_2 in a low-voltage range and then to precisely estimate V_F of D_1 in the same forward current. In addition, diodes in series will reduce the parasitic capacitor by half, which is very helpful to the high-f_s response of the extraction circuit. We call this method a DDI method. Moreover, ZD_1 and D_3 are freewheeling diodes and ZD_1 is also a positive clamping diode. These two diodes are a general 5 V Zener ZD_1 and a general small signal diode D_3 (1N4148) with 75 V/150 mA. All of the functional diodes including D_1, D_2, ZD_1 and D_3 are specially selected with a very low parasitic capacitance, which will improve the high-f_s response of the extraction circuit to several MHz. I_1 is a constant-current source of only several mA, so it cannot produce a temperature problem and an extra self-heating effect. I_1 consists of a constant-current diode, which is actually a junction field transistor with a gate-source short connection. Therefore, I_1 can achieve an excellent constant current over a wide operating voltage range. R_t provides a minimum load for I_1 and suppresses the voltage spike at point B. An isolated low-voltage probe (P2221 from Keysight Inc.) with a 1:1 attenuation can be used to test V_F of D_2 and the voltage at point B. The low-voltage probe with a 1:1 attenuation will not amplify the background noise and operate in a low-voltage range, so it can obtain an improved test accuracy.

We build the above switching circuit and extraction circuit with one printed circuit board (PCB), as shown in Figure 1c.

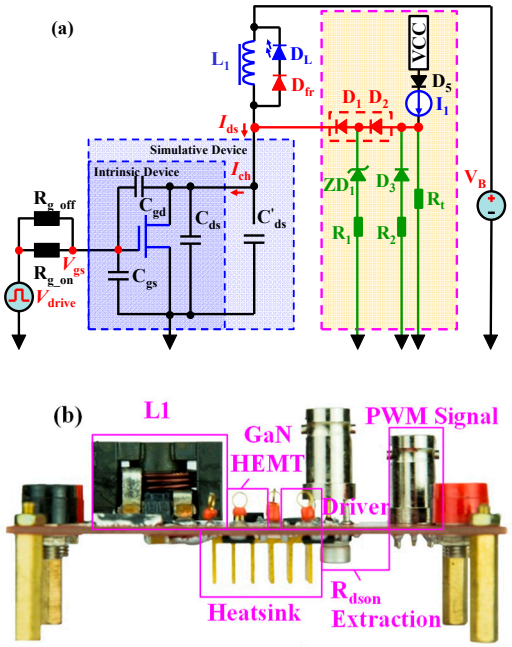

Figure 2. Lumped equivalent switching circuit with a floating buck-boost topology (a), and a photograph of the assembled printed circuit board (b).

2.3. C. Qualitative Method to Discover the Channel Behavior

Since we cannot perform the measurements inside the HEMT device directly, we propose a new evaluation method by employing an extended parallel capacitor C_{ds}', as shown in Figure 3. In this lumped circuit, the intrinsic capacitor C_{ds} is assumed to not exist, and the extended capacitor C_{ds}' outside the device is assumed to be the intrinsic capacitor. Therefore, the channel current ($I_{channel}$) and I_{drain} can be measured directly and separately by an oscilloscope and current probes. Although an extra parallel capacitor will lead to an increase in the measured I_{drain} and $I_{channel}$, this qualitative method can be used to assess the difference between these two currents, and thereby, the cause of the discrepancy can be located. After understanding this reason, the resulting loss effect on the eGaN HEMT device can be further quantified by an analytical method. In the analytical method, the additional C_{ds}' is no longer required, therefore, the C_{ds}' does not materially affect the device losses.

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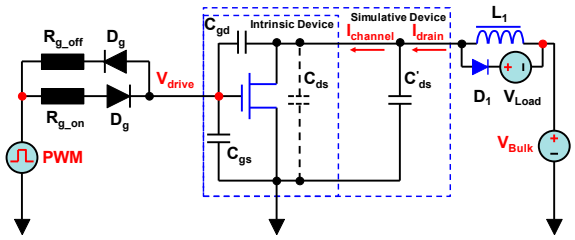

Figure 3. The lumped simulation circuit with an extra parasitic capacitor.

3. Extraction of the Dynamic R_{dson}

It is well known that a high V_{ds_off} will cause surface- and buffer-related trapping processes, which will lead to a larger dynamic R_{dson} compared to the direct current (DC) R_{dson} (R_{dson_DC}) [18,19]. Figure 4 illustrates the mechanism of the increase in the dynamic R_{dson} induced by the trapping effect. The high electric field helps the electrons escape from the GaN well, and then these electrons are captured by traps or some of the surface states that are activated by a high electric field. When removing the electric field, these trapped electrons cannot be released to the well instantaneously. The reason for the slow return of electrons is that the trapping time of electrons in the off-state is on the order of ns, whereas the detrapping time of electrons in the on-state is on the order of second [20,21]. Thus, trapped electrons accumulate and worsen the device performance at a high f_s. Meanwhile, electrons migrate from the gate to the gate-drain side adjacent surface to form a virtue gate; hence, the number of electrons in the access region decreases. The decreasing number of electrons in the drift region will result in a large dynamic R_{dson} [22,23].

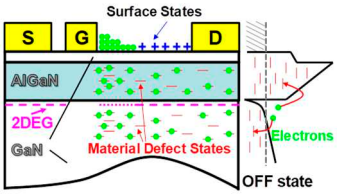

Figure 4. Mechanism for the dynamic R_{dson}.

In the circuit of Figure 1b, the current I_1 flows partly through R_t and partly through the HEMT device, and the voltage of point B (V_B) can be tested by the voltage probe P2221 directly. Then, the dynamic R_{dson} can be calculated by

$$R_{dson} = (\overline{V}_B - 2\overline{V}_{F\_D2}) / (\overline{I}_{drain} - I_1 + \overline{V}_B / R_t) \quad (2)$$

where $\overline{V}_B$, $\overline{V}_{F\_D2}$, $\overline{I}_{drain}$, $\overline{I}_{D2}$, and I_1 are the average voltages of point B and D_2, the average currents through a resistive load and D_2, and the current of the constant-current supply, respectively. I_{drain}, the voltage of point A (V_{drain}) and V_{F_D2} of D_2 are tested by a current probe (TCP0020), a high-voltage differential probe (THDP0200), and a low-voltage differential probe with a 1:1 attenuation (TIVH02) and displayed on an oscilloscope (MDO3104). Finally, the calculated dynamic R_{dson} is normalized by R_{dson_DC}, which is 200 $m\Omega$, from an eGaN HEMT (GS66502B from GaN Systems Inc.) [24].

Figure 5b–f show the results of the dynamic R_{dson} of the eGaN HEMT for various V_{ds_off}, f_s, duty cycles, I_{drain} and operating temperatures, which are extracted in the on-state by taking average values in the stable region marked in Figure 5a,b shows that the dynamic R_{dson} increases as V_{drain} increases, under the conditions of an 80% duty cycle and an f_s of 100 kHz, so the dynamic R_{dson} is voltage-dependent. Figure 5c,d show the dynamic R_{dson} increases as f_s increases and duty cycle decreases, respectively for a 500 V V_{drain} condition, so the dynamic R_{dson} is also time-dependent. Considering that the dynamic R_{dson} is not only affected by the trapping effect, we further test the relationship between the dynamic R_{dson} and I_{drain} and temperature, as shown in Figure 5e,f, respectively. These two tests

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will help us isolate the trapping effect caused by the increase in the dynamic R_{dson} in a particular complex test condition.

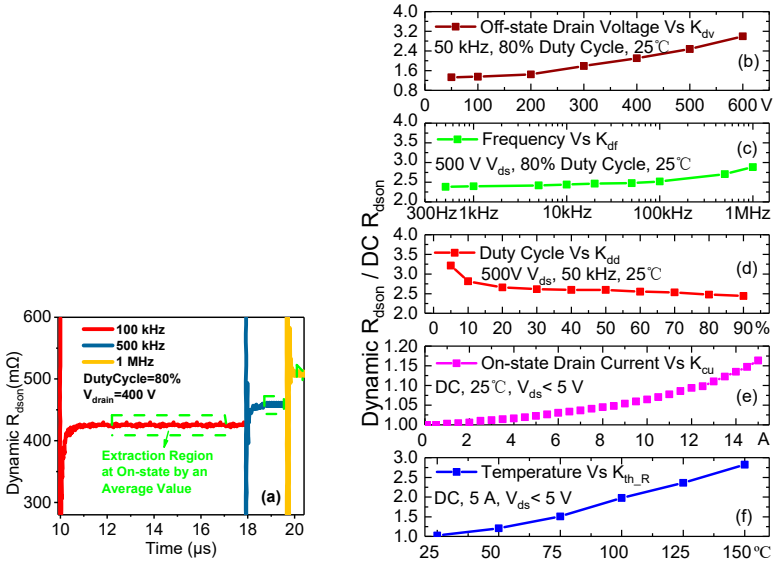

Figure 5. Dynamic R_{dson} extraction waveforms at various f_s (a) and the dynamic R_{dson} normalized by R_{dson_DC} for various V_{ds_off} (b), fs (c), duty cycles (d), I_{drain} (e) and temperatures (f).

In conclusion, the trend of the results of the extracted dynamic R_{dson} of the eGaN HEMT is consistent with the mechanism of the trapping-effect-induced increase in the dynamic R_{dson}. From Figure 6, we can obtain the real conduction resistance of the eGaN HEMT device under a certain working condition, and then the conduction loss can be corrected.

4. Discussion on the Effect of the Drain Current by a Double-Mode Test Technique

Base on the test circuit in Figure 1, a new double-mode test technique which including a DCM and a CCM is proposed. Then, the tested waveforms during the turn-on and turn-off transitions for various voltage and PWM conditions are illustrated in the Figure 6. To ensure that the switching circuit operates in open-loop CCM and DCM, V_{Bulk} is set to 400 V, and the V_{Load} is set to 80 V in DCM and 20 V in CCM, so the V_{ds_off} values of the devices in the two modes are different.

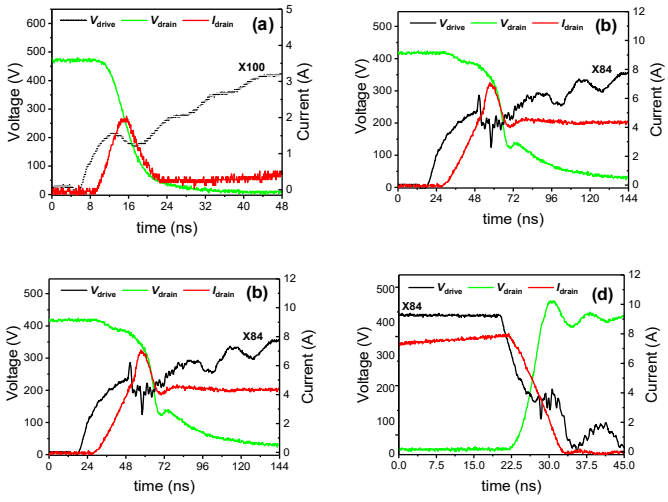

Figure 6. Experimental waveforms of the HEMT device during the turn-on transitions in 400 V DCM with a V_{Load} of 80 V (a) and 400 V CCM with a V_{Load} of 20 V (b) and during turn-off transitions in 400 V DCM with a V_{Load} of 80 V (c) and 400 V CCM with a V_{Load} of 20 V (d).

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The current I_{drain} in DCM exhibits only one resonant waveform when the drain voltage decreases, as shown in Figure 6a, while I_{drain} in CCM has an extra linear increase before the resonant waveform occurs, as shown in Figure 5b. The corresponding voltage fall time is approximately 14 ns in Figure 6(a) and is approximately 42 ns in Figure 6b, so that the extra linear increase in the current will increase the turn-on time and cause a high dynamic power loss. This linear increase in the current is caused by the high start current and the linear conduction of the eGaN HEM at this time. This means that DCM is a better operating mode for reducing the turn-on time.

In addition, the rise time of the drain voltage during the turn-off transition, which is approximately 10 ns, as shown in Figure 6d, is faster than that of approximately 30 ns in Figure 6c. This is because I_{drain} in Figure 6d is higher than that in Figure 6c, and the rise time of the drain voltage during the turn-off transition mainly depends on the charge time of C_{oss}. Moreover, the peak current in DCM during the turn-off transition will be higher than that in CCM under the same output power conditions. This means that DCM is a better operating mode for reducing the turn-off time.

In conclusion, the drain current will significantly affect the turn-on and turn-off times, and DCM is better than CCM for reducing the crossover power losses.

5. Investigation on the Real Channel Current

According to the qualitative method in Figure 2, we can study the discrepancy between I_{drain} and $I_{channel}$. Figure 7a shows the tested I_{drain}, $I_{channel}$, V_{drain} and V_{drive} values of the AlGaN/GaN HEMT in the turn-on transition for a V_{ds_off} of 500V, an f_s of 100 kHz, and a duty cycle of 16.5%. It is shown that $I_{channel}$ is larger than I_{drain} while the drain voltage decreases. The current path in this time interval is shown in Figure 7b, where the channel current partially results from the discharging current of the parasitic output capacitor.

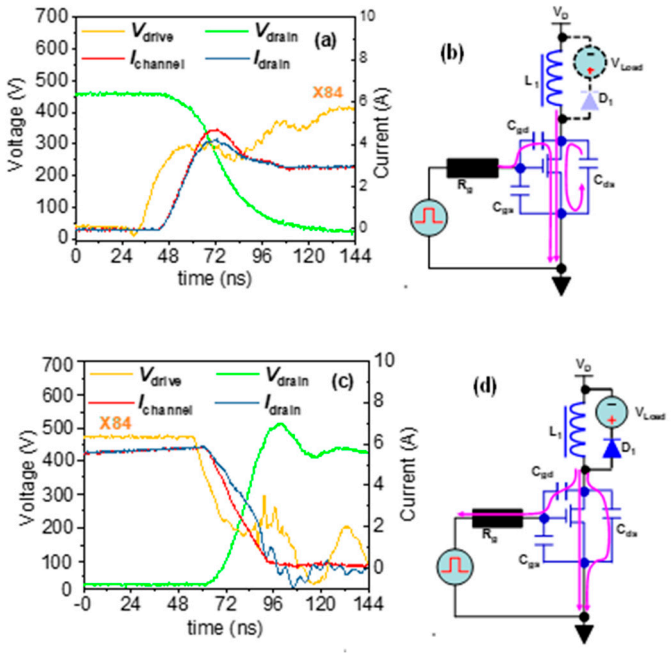

Figure 7. Experimental results during the turn-on transition in 500 V CCM (a) and a schematic diagram of the corresponding current path (b) and the experimental results during the turn-off transition in 500 V CCM and a schematic diagram of corresponding current path (d).

Figure 7c shows the tested I_{drain}, $I_{channel}$, V_{drain} and V_{drive} values of the AlGaN/GaN HEMT during the turn-off transition for a V_{ds_off} of 500 V, an f_s of 100 kHz, and a duty cycle of 16.5%. It is shown that $I_{channel}$ is smaller than I_{drain} while the drain voltage increases. The current path in this time interval is shown in Figure 7d where the channel current is partially diverted to the branch of output capacitor.

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In conclusion, $I_{channel}$ is not exactly equal to I_{drain}, and unfortunately, $I_{channel}$ cannot be tested directly. However, with the above test results and the current path analysis, we can acquire the reason for the discrepancy between $I_{channel}$ and I_{drain} so that the real $I_{channel}$ value can be obtained by a test of I_{drain} and an analytical method, and the power losses of eGaN HEMTs can be correctly evaluated.

6. Modeling of Switching Power Losses

Figure 8 shows a detailed timing diagram of the switching period [25] for eGaN HEMTs in DCM or CCM. The operating period of the power devices can be divided into 12-time intervals from t_0 to t_{12} according to the status of the drain voltage and I_{drain} in the off-state, on-state, turn-on transition, and turn-off transition. To investigate the detailed dynamic power loss, we reclassify the 12-time intervals into the following four stages (S1-S4) according to their different contributions to the dynamic power loss.

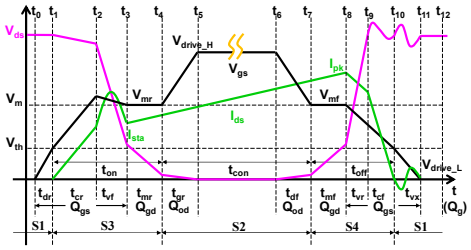

Figure 8. Timing diagram of the GaN HEMT devices.

6.1. A. Stage 1(S1) – Off-state with a High V_{ds}

During the t_0–t_1, t_{10}–t_{11}time intervals and the time of the off-state, the device sustains a high V_{ds}. Thus, the voltage-dependent leakage current (I_{lk}) will lead to an off-state power loss (P_{off}). We can no longer ignore this power loss, especially at a very high drain voltage and a very high frequency. In general, the t_0–t_1 and t_{10}–t_{11}time intervals can be neglected in comparison with the off-state time, so P_{off} can be written as

$$P_{off} = I_{lk} V_{ds} [t_{t_0 - t_1} + t_{t_{11} - t_{12}} + (1 - \mathrm{D})T] f_s \approx I_{lk} V_{ds} (1 - \mathrm{D}) \tag{3}$$

where T and D are the period and duty cycle, respectively. In addition, eGaN HEMTs have no reverse recovery problem because the 2DEG in the channel is naturally formed by the polarization effect. This will reduce the power loss and mitigate the electromagnetic interference (EMI) problem which is produced by the reverse recovery caused by ringing.

6.2. B. Stage 2(S2) – On-state in Saturation Region

During the t_4–t_7 time intervals, the device is in the on-state. The RMS value of the drain current (I_{drain_rms}) can be written as

$$I_{\mathrm{drain}\_rms} = \sqrt{f_s \int_0^{1/f_s} I_{drain}{}^2(\mathrm{t})\,\mathrm{dt}} \tag{4}$$

To take the problem of the increase in the dynamic R_{dson} into account, the traditional conductive power loss (P_{con}) can be modified by

$$P_{con} = I_{drain\_rms}{}^2 R_{dson\_DC} k_{dv} k_{df} k_{dd} k_{th\_R} k_{cu} \tag{5}$$

where k_{dv}, k_{df}, k_{dd}, k_{at} and k_{th_R} are the dynamic coefficients of R_{dson} related to the voltage, f_s, the duty cycle, the current and the temperature, respectively.

6.3. C. Stage 3(S3) – Turn-on Transition

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During the t_1–t_4 time interval, the device is in turn-on transition. In the t_1–t_2 time interval, I_{drain} increases while V_{drain} decreases slightly in CCM, but this time interval does not exist in DCM; in the t_2–t_3 time interval, V_{drain} decreases and leads to a resonant I_{drain}; in the t_3–t_4 time intervals, V_{drain} decreases to very low voltage, and the device starts to operate in an ohmic conducting state. These crossovers of V_{drain} and I_{drain} will cause power losses during the turn-on transition (P_{turn_on}):

$$P_{\text{turn}\_on} = \int_{t_1-t_4} V_{ds}(t) I_{drain}(t) f_s dt + \frac{1}{2} C_{oss} V_{ds}^{\ 2} f_s \tag{6}$$

1) In the t_1–t_2 time interval, I_{drain} increases almost linearly from 0 to the I_{sta} at t_2, similar to a Si-based MOSFET [26–27], while V_{drain} decreases slightly from V_{ds} to V_r due to the result of the parasitic inductance voltage drop caused by a high di/dt in the circuit. At t_2, the current of the freewheeling diode D_1 decreases to zero. In this time interval, the gate voltage of the device slightly exceeds V_{th}, so the device is operating in a linear region. Meanwhile, the trapping effect for a high electric field will also lead to a large dynamic R_{dson} in the linear region ($R_{turn\_on\_cr}$), similar to that in the on-state, as well as an extra gate lag. Thus, the coefficients of the dynamic R_{dson} should be the same as those in Figure 4. Assuming that the heatsink is large enough and the self-heating effect is ignored, the t_1-t_2 time interval, V_r and the power losses in this time interval ($P_{turn\_on\_cr}$) can be written by

$$R_{turn\_on\_cr} = \frac{\Delta V_{ds}}{\Delta I_{channel}} \approx \frac{k_{dv} k_{df} k_{dd} k_{th\_R} k_{cu} L_{eff\_Gate}}{W_{eff\_Gate} \mu_s C_{gs} (V_{drive\_H} - V_{th})} \tag{7}$$

$$t_1 - t_2 = \frac{C_{gs} R_{g\_on} i_{sta} + L_s i_{sta} g_m}{[V_{drive\_H} - 0.5(V_{mr} + V_{th})] g_m} k_{lag} \tag{8}$$

$$V_r = V_{ds} - L_s \frac{i_{sta}}{t_1 - t_2} - R_{turn\_on\_cr} \frac{i_{sta}}{2} \tag{9}$$

$$P_{\text{turn}\_on\_cr} = \frac{1}{2} i_{sta} V_r (t_1 - t_2) f_s \tag{10}$$

where, L_{eff_Gate} and W_{eff_Gate} are the effective channel length and width, respectively. L_s is the source inductor which is in series with and between the source terminal and the ground. The coefficient of the gate lag（k_{lag}）is a fitting parameter, which can be obtained by measuring the turn-on delay for various V_{ds_off}, f_s and duty cycles.

2) In the t_2–t_3 t.ime interval, the HEMT device takes over the total inductive load current, and V_{ds} decreases to a boundary voltage of (V_{mr}-V_{th}) at t_3 due to the discharging of C_{oss}. The stray inductors in series around the circuit are resonant with C_{oss} and the stray capacitors (C_{stray}) in this time interval. The current path through the device is illustrated in Figure 5b. It is assumed here that V_{gs} and i_{sta} remain unchanged, and the reverse recovery of the D_1 is zero. In addition, the current in this time interval is usually large enough; and hence, the charging time of C_{oss} can be ignored. Moreover, voltage-dependent C_{oss} is not suitable for calculating power losses in this time interval because V_{drain} is always changing. Therefore, Q_{gd} is used to replace C_{oss}, and then the time interval of t_2-t_3 can be written as

$$C_{gd\_vf} = \frac{Q_{gd}}{\Delta V} = \frac{Q_{gd}}{V_r - V_{mr} + V_{th}} \tag{11}$$

$$t_2 - t_3 = \frac{Q_{gd} R_{g\_on} + C_{stray}(V_r - V_{mr} + V_{th}) / g_m}{V_{drive\_H} - V_{mr}} \tag{12}$$

Then, the power losses in this time interval ($P_{turn\_on\_vf}$) can be written by [28]:

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$$\bar{I}_{vf} \approx 0.5\left(\frac{V_r}{R_{turn\_on\_cr}} + \frac{V_{mr} - V_{th}}{R_{dson}}\right) \tag{13}$$

$$\begin{aligned} P_{\text{turn\_on\_vf}} &= \frac{1}{2}(i_{sta} + \bar{I}_{vf})(V_r - V_{mr} + V_{th})(t_2 - t_3) f_s \\ &+ \frac{1}{2} C_{stray}[V_r^2 - (V_r - V_{mr} + V_{th})^2] f_s \end{aligned} \tag{14}$$

where $\bar{I}_{vf}$ is the average channel current during the t_2–t_3 time interval.

3) During the t_3–t_4 time interval, the HEMT device operates in an ohmic conducting state. Then, V_{drain} continues to decrease until it reaches a low on-voltage (V_{on}) from(V_{mr}-V_{th}). Assuming that i_{sta} and the Miller voltage V_{mr} do not change, then the t_3-t_4 time interval, V_{on_r} and the power losses in this time interval ($P_{turn\_on\_mr}$) can be written by [29]:

$$t_3 - t_4 = \frac{Q_{gd} R_{g\_on}}{V_{drive\_H} - V_{mr}} \tag{15}$$

$$V_{on\_r} = i_{sta} R_{dson} k_{dv} k_{df} k_{dd} k_{th\_R} k_{cu} \tag{16}$$

$$\begin{aligned} P_{\text{turn\_on\_mr}} &= \frac{1}{2} i_{sta}(V_{mr} - V_{th} - V_{on\_r})(t_3 - t_4) f_s \\ &+ \frac{1}{2} C_{stray}[(V_{mr} - V_{th} - V_{on\_r})^2 - V_{on\_r}^2] f_s \end{aligned} \tag{17}$$

From the above analysis, Equation (6) can be modified by

$$P_{\text{turn\_on}}(\text{measured}) = P_{\text{turn\_on\_cr}} + P_{\text{turn\_on\_vf}} + P_{\text{turn\_on\_mr}} \tag{18}$$

Notice that in this stage, i_{sta} is a tested drain current instead of a real channel current and they are actually different in the t_2–t_3 time interval, as shown in Figure 5a. However, $I_{channel}$ is the real factor that results in the power losses in this stage, and the real $I_{channel}$ is the combined current of I_{drain} and the discharging current of C_{oss}:

$$I_{channel} = I_{drain} + I_{Cds} + I_{Cgd} \approx I_{drain} + I_{Cds} \tag{19}$$

Thus, Equation (18) can be finally modified by [12]

$$P_{\text{turn\_on\_act}} = P_{\text{turn\_on\_mea}} + P_{\text{turn\_on\_dis}} \tag{20}$$

where

$$P_{\text{turn\_on\_dis}} = \frac{1}{2} C_{oss} V_{ds\_\text{off}}^2 f_s \tag{21}$$

Thus,

$$\begin{aligned} P_{\text{turn\_on\_act}} &= P_{\text{turn\_on\_cr}} + P_{\text{turn\_on\_vf}} \\ &+ P_{\text{turn\_on\_mr}} + \frac{1}{2} C_{oss} V_{dsf}^2 f_s \end{aligned} \tag{22}$$

6.4. D. Stage 4(S4) – Turn-off Transition

During the t_7–t_{11} time intervals, the device is in a turn-off transition. In the t_7-t_8 time intervals, the drain voltage increases while I_{drain} stays almost constant; in the t_8–t_9 time intervals, the drain voltage continuously increases while I_{drain} decreases slightly; in the t_9–t_{10} time intervals, I_{drain} decreases while the drain voltage stays almost constant. Finally, I_{drain} decreases to zero, and the drain voltage becomes resonant in the t_{10}–t_{11} time intervals. These crossovers of V_{drain} and I_{drain} will cause power losses during the turn-off transition (P_{turn_off}):

$$P_{\text{turn\_off}} = \int_{t_7 - t_{10}} V_{ds}(t) I_{drain}(t) f_s dt \tag{23}$$

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4) In the t_7–t_8 time interval, the observations are very similar to those in the t_3–t_4 time interval. The HEMT device goes into a linear region from an ohmic conducting state. V_{drain} increases to a boundary voltage of $V_{mf}-V_{th}$. Assuming that the peak current is unchanged, and $V_{mf}=V_{mr}$, then the t_7-t_8 time interval, V_{on_f} and the power losses in this time interval ($P_{turn\_on\_mf}$) can be written by:

$$t_7 - t_8 = \frac{Q_{gd} R_{g\_off}}{V_{mf} - V_{drive\_L}} \tag{24}$$

$$V_{on\_f} = I_{pk} R_{dson} k_{dv} k_{df} k_{dd} k_{th\_R} k_{cu} \tag{25}$$

$$P_{\text{tum\_off\_mf}} = \frac{1}{2} i_{pk} (t_7 - t_8)(V_{mf} - V_{th} - V_{on\_f}) f_s \tag{26}$$

5) In the t_8–t_9 time interval, the observations are very similar to those in the t_2–t_3 time intervals. V_{drain} continues to increase faster towards the off-state V_{ds_off}, while I_{drain} decreases slightly to i_r. This current drop is caused by a charging shunt to other peripheral devices [25], and the current path through the device is illustrated in Figure 5d. Assuming that the Miller voltage (V_{mf}) remains unchanged and that the current-dependent charging time of C_{oss} can no longer be ignored, we have:

$$t_8 - t_9 \approx \frac{Q_{gd} R_{g\_off} + C_{stray}(V_{ds} - V_{mf} + V_{th})/(2g_m)}{V_{mf} - V_{drive\_L}} + \frac{C_{oss}(V_{ds} - V_{mf} + V_{th})}{i_{pk}} \tag{27}$$

$$i_r = i_{pk} - C_{stray}\frac{dV_{ds}}{dt} = i_{pk} - C_{stray}\frac{V_{ds} - V_{mf} + V_{th}}{t_8 - t_9} \tag{28}$$

$$P_{\text{tum\_off\_vr}} = \frac{i_{pk} + i_r}{2}(V_{ds} + V_{mr} - V_{th})(t_8 - t_9) f_s \tag{29}$$

6) In the t_9–t_{10} time interval, the observations are similar to those in the t_1–t_2 time interval. I_{drain} decreases from i_r to a low value because the current begins to divert from the HEMT device to D_1. In this time interval, the drain voltage is in a state of resonance, while V_{gs} decreases to (V_{mr}-V_{th}) and the device channel current reaches zero at t_{10} [30]. Then, the t_9-t_{10} time interval and the power losses at this time interval ($P_{turn\_off\_cf}$) can be written by:

$$t_9 - t_{10} = \frac{(C_{gs} R_{g\_off} + L_s g_m) i_r}{[0.5(V_{mf} + V_{th}) - V_{drive\_L}] g_m} \tag{30}$$

$$P_{\text{tum\_off\_cf}} = \frac{1}{2} i_r V_{ds\_off}(t_9 - t_{10}) f_s + \frac{L_{stray} i_r^{\,2}}{2} \tag{31}$$

7) During the t_{10}–t_{11} time interval, the device is turned off but V_{drain} ringing occurs due to the resonance between C_{oss} and L_{stray}. These fluctuations of the drain voltage will lead to a slight power loss which depends on the ringing peak voltage (V_{ds_pk}). Assuming that the reverse recovery of D_1 is zero, we have:

$$\frac{L_{stray} i_r^{\,2}}{2} = \frac{C_{oss}\Delta V^2}{2} \rightarrow \Delta V = \sqrt{\frac{L_{stray} i_r^{\,2}}{C_{oss}}} \rightarrow V_{ds\_pk} = V_{ds\_\text{off}} + \Delta V \tag{32}$$

$$P_{\text{tum\_off\_vx}} \approx \frac{1}{2} C_{oss}(V_{ds\_pk}^{\,2} - V_{ds\_off}^{\,2}) f_s \tag{33}$$

From the above analysis, Equation (23) can be modified by

$$P_{turn\_off}(\text{measured}) = P_{\text{turn\_off\_mf}} + P_{\text{turn\_off\_vr}} + P_{\text{turn\_off\_cf}} + P_{\text{turn\_off\_vx}} \tag{34}$$

instead of real channel currents and they are actually different in the t_8–t_9 time interval, as shown in Figure 5c. However, $I_{channel}$ is the real factor that results in the power losses in this stage, and the real $I_{channel}$ is the diverted current of I_{drain} and the charging current of C_{oss}:

$$I_{channel} = I_{drain} - I_{Cds} - I_{Cgd} \approx I_{drain} - I_{Cds} \tag{35}$$

Therefore, Equation (34) can be finally modified as [12]:

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$$P_{\text{turn\_off}}(\text{actual}) = P_{\text{turn\_off}}(\text{measured}) - P_{\text{turn\_off}}(\text{charge}) \quad (36)$$

where

$$P_{\text{turn\_off\_char}} = \frac{1}{2} C_{oss} V_{ds\_off}^{\ 2} f_s \quad (37)$$

Thus,

$$P_{\text{turn\_off\_act}} = P_{\text{turn\_off\_mf}} + P_{\text{turn\_off\_vr}} + P_{\text{turn\_off\_cf}} + P_{\text{turn\_off\_vx}} - \frac{1}{2} C_{oss} V_{ds\_off}^{\ 2} f_s \quad (38)$$

Finally, the total power loss (P_{total}) should be described with the sum of Equations (3)–(38):

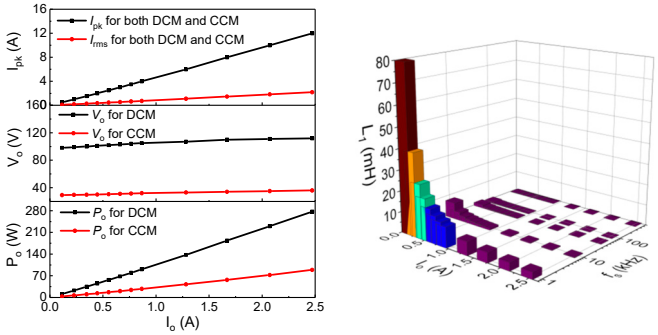
$$P_{total} = P_{off} + P_{con} + P_{turn\_on\_act} + P_{\text{turn\_off\_act}} \quad (39)$$

In particular, the effects of $I_{channel}$ and I_{drain} on P_{total} can finally cancel out for a hard switch. However, in a soft switch application such as a zero-voltage switch (ZVS), $P_{turn\_on\_dis}$ is zero; hence, $P_{\text{turn\_off\_char}}$ can no longer cancel out. This correction becomes very meaningful to the universality of the dynamic power loss model for eGaN HEMTs.

As can be seen, P_{total} in Equation (39) is very different from that in Equation (1). Equation (39) has no power loss of reverse recovery, but it takes the trapping-effect-induced dynamic R_{dson} and the impacts of the I_{drain} and the real $I_{channel}$ into account.

7. Model Verification by Experiments

To verify our dynamic power loss model, we adopt a floating buck-boost power converter with a light-emitting diodes (LEDs) operating in DCM and CCMs. To maintain the operation mode and the output current (I_o) in an open-loop control system, some key parameters are adjusted (such as L_1) or tested (such as the output voltage V_o, peak operating current I_{pk}, and the output power P_o) in the circuit, as shown in Figure 8, for an input voltage (V_{Bulk}) of 400 V, a duty cycle of 10%, and various f_s and I_o values.



(a) (b)

Figure 9. The relationship between Io and V_o, P_o, and I_{pk} (a) and the relationship between I_o and inductance of L_1 for various f_s (b) in an open-loop controlled floating buck-boost power converter.

The power losses are then tested by a power analyzer (PW6001-03 from HIOKI Inc.). Figure 10a–c reveal that the analytical results of the total dynamic power losses by the proposed model are in good agreement with experimental results both in CCM and DCMs, even for various I_o, f_s and V_{Bulk} values. The experimental results are slightly different from the analytical results, which may be because of the measurement accuracy of the power meter reduced at a high f_s.

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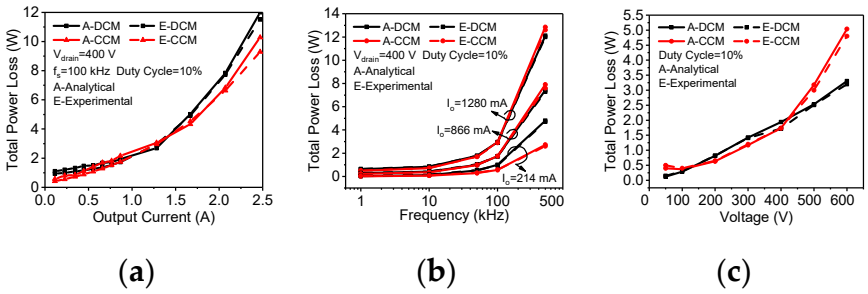

Figure 10. Comparison of the total dynamic power losses from the analytical and experimental results both in CCM and DCMs and for various I_o (a), f_s (b) and V_{Bulk} (c).

Figure 11a shows the relationship between the total dynamic power losses and I_o in CCM and DCMs. In the case of a small I_o, the switching loss is dominant, while in the case of a large I_o, the conduction loss is dominant. In addition, the dynamic power loss increases faster with the increase in I_o in DCM than in CCM, indicating that DCM is not suitable for high current conditions.

Figure 11b shows the switching loss during the turn-on and turn-off transitions in CCM and DCM. The results reveal that the switching loss is lower in DCM than in CCM during the turn-on transition but larger during the turn-off transition when Io is larger than 1.25 A. This means that DCM is more suitable for a relatively small Io. In this case, from Figures 10b and Figure 11a, 1.25 A is a moderate output current that is acceptable.

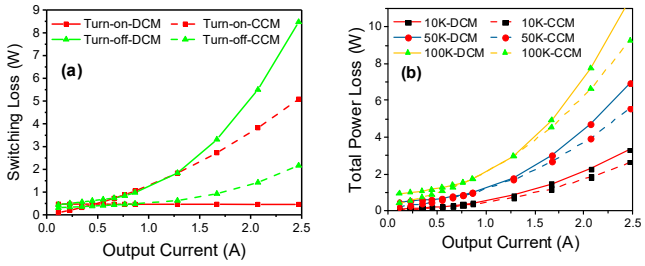

Figure 11. Experimental total dynamic power losses (a) and switching losses (b) as a function of the output current in DCM and CCM

To restrain the peak current and obtain a high operating efficiency, the QRM is then proposed. The reason is that QRM works at the DCM boundary, where V_{drain} will decrease to a minimum value at the beginning of the turn-on transition while I_{drain} decreases to zero. In addition, the peak on-state current in DCM is usually larger than that in CCM, and the current will be at a controllable high level, so the turn-off time is fast in QRM. Therefore, QRM is more suitable for achieving a lossless switch and even for reducing the turn-off transition time.

8. Conclusions

An improved 12-time-interval piecewise dynamic power loss model for eGaN HEMTs is developed by specially quantifying the effects of the increase in the dynamic R_{dson}, the impact of I_{drain} on the turn-on and turn-off times, and the real $I_{channel}$, good agreement with some experimental results is verified.

In this work, three new methods or techniques are proposed, which are DDI method, double-mode test technique and qualitative, respectively. Then, the dynamic R_{dson} is obtained by our new extraction circuit at a high operating fs up to 1 MHz and high drain voltage up to 600 V, and the drain current is found to significantly affect the turn-on and turn-off times by a switching circuit operating in DCM and CCM, and the real channel current is accurately calculated to distinguish it from the measured drain current. All of these parameters are included into the power loss model.

Moreover, the QRM has a low V_{ds_off}, zero turn-on current, and relatively large peak current. Therefore, on the basis of the model, we propose the QRM to obtain a high efficiency and decrease the turn-off switching time for the application of eGaN HEMTs.

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