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Article

Using the LabVIEW Simulation Program to Design and Determine the Characteristics of the Amplifiers

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Abstract: Because of the large number of parameters that interact in their function, determining dynamic regime parameters as well as the mode of function of amplifying stages is an extremely complex problem. This paper describes a LabVIEW application for studying the functioning of an amplifier in various connections. The user selects the generator's parameters, the type of connection and its parameters, as well as the electric charge characteristics. The application can determine both the stage characteristics and the Bode characteristics. The amplifier's stability zone, as well as its gain and phase, are determined based on these characteristics. An important advantage of this application is that the design of the amplifier stage can be made starting from some parameters that the amplifier can establish, from which the values of components can be determined. In order to validate the simulation results using the LabVIEW application, a specialized program Multisim was used, as well as experimental measurements using the Electronics Explorer Board. Both Multisim and Electronics Explorer Board can determine Bode characteristics. In both simulations and experimental amplifiers, the same schemes with the same transistor was used. The application can be used for educational purposes as well as to design the amplifier's stage to achieve specific parameters.

Keywords: amplifier stage; dynamic regime parameters; Bode characteristics; gain and phase

1. Introduction

Although amplifiers are useful on their own, the design of an amplifier allows for the evaluation of various circuit design and analysis methods. When designing an amplifier, circuit design and PCB architecture should always consider amplifier stability. However, there are times when an amplifier is pushed to its absolute limit and fails to perform as expected, resulting in output signal distortion. Several publications in specialized journals investigate amplifier stability [1–3].

A variety of criteria, including Bode, are used to assess amplifier stability [1,4].

Because amplifier stability is a complex problem, many mathematical modelling methods have been developed to investigate it [2]. A computer tool that enables a mathematical examination of the physical stability of the bipolar transistor in the design of amplifiers is described in [2]. Users can set values for voltage gain, output impedance, input impedance, transistor current gain, and power supply current gain, and the software will return resistance values as a result. The study concluded that the power wasted in a bipolar transistor amplifier is inversely related to the magnitude of the input signal and directly proportional to the distance of the half of the input signal from the operating point. It has been determined that the operation point should be located higher than 0.05 and lower than 0.95, with 90% of the load line used for amplification.

In our study we used LabVIEW software to simulate various amplifier types. This program is useful and appropriate for simulating analogue electronic circuits [5].

Other software programs for modelling electronic circuits are described in specialized literature. Multisim simulation software is one example [6]. Multisim was used to study an amplifier used as a second order filter in the paper [6]. Multisim software can be used to create a circuit with inputs and outputs. Multisim was used in [6] to simulate a Bode plotter component and generate a frequency

signal graph. Bode plotter simplifies the examination of circuits, signal magnitude, and phase shape, and it can compare variations between circuits.

In [7], amplifiers were analysed using another software package, this time one written in Java. The software presented in [7] is a learning tool that enhances understanding of multi-stage amplifiers. This makes it possible for it to serve as a virtual guide with a user-friendly graphical interface that facilitates learning.

Several publications have proposed the common emitter (CE) amplifier design as a method for obtaining suitable amplifier performance parameters. The authors of [3] presented an amplifier that would perform well for devices that operate at low frequencies. The PSPICE program was used to research the proposed amplifier in [3,8]. For the investigation of amplifiers, the PSPICE program is useful. This bipolar junction transistor SPICE model from [8] was created to help students better understand amplifier design and analysis methods.

Because there is a need in technology to amplify electrical signals, i.e. to obtain on a load circuit higher power signals but identical in form of time variation with those of low power available, amplifiers are used [9–14]. Electronic amplifiers are constructed using bipolar or field effect transistors, either as discrete circuits or as integrated circuits.

In practice, there is a wide range of amplifiers. Their classification can be done using a variety of criteria, [15].

According to the frequency range of the amplified signals, there are direct current amplifiers, where the lower limit of the frequency of the amplified signal is 0 Hz, low frequency amplifiers, where the frequency band is in the range $n \times 10 \text{ Hz} \div n \times 10 \text{ kHz}$, broadband amplifiers, where the frequency band can be in the range $0 \text{ Hz} \div n \times 10 \text{ MHz}$, and narrowband amplifiers, in which the ratio between the maximum and minimum frequency of the signal to be processed is of the order units.

According to the amplitude of the signal applied to the input, there are small signal amplifiers, where the amplitude of the input signal is small enough for the static operating point of the transistor to remain in a linear region of the dynamic or transfer characteristic, and large signal amplifiers, where the amplitude of the input signal is large enough for the static operating point of the transistor to remain in a linear region of the dynamic or transfer characteristic at which the amplitude of the input signal exits the linear region of the dynamic or transfer characteristic.

In dynamic mode, there are three types of connections made by the terminal of the bipolar transistor that is common at the input and output: common emitter connection, common collector connection, and common base connection.

According to the operating regime of the transistor, materialized by the conduction duration during a period of the signal, the amplifiers can operate in class A, where there is collector current throughout the period of the input signal, class B, where the current collector exists only on one half-period of the input signal, class C, where the transistor conducts less than one half-period of the input signal, and class AB, which represents an intermediate category between classes A and B.

According to the type of coupling between stages, there are amplifiers with direct coupling, capacitive coupling, transformer coupling, optical coupling, and so on, depending on the type of coupling between stages.

The following main characteristics are used to evaluate and compare amplifier quality, [15,16]: amplification, linear distortions such as frequency distortions, phase distortions, and transient distortions, nonlinear distortions, and noises.

The main characteristics of an amplification stage can be determined using the transistor's quadrupole parameters: current amplification, voltage amplification, input impedance or resistance, and output impedance or resistance. In this regard, the quadrupole parameters selected based on the frequency of the input signal can be used. For low frequencies, the parameters "h", considered in this paper to have real values, the parameters " π " or the parameters "r" are particularly useful. For high frequencies, the parameters "y" or the natural equivalent circuit parameters, "g", are used [15–18].

Because the functioning of amplification stages with bipolar transistors at low and medium frequencies was studied in this paper, the quadrupole "h" parameters, which are valid for any type of transistor connection, were taken into account.

Figure 1 depicts the equivalent circuit of the amplifier stage with bipolar transistor using the quadripole parameters "h", [15].

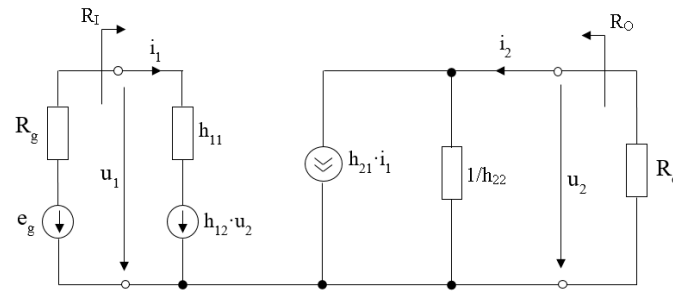


Figure 1. The equivalent circuit of the amplifier stage using the quadripole "h" parameters.

The transistor's quadripole equations are given by relation (1).

$$\begin{aligned} u_1 &= h_{11} \cdot i_1 + h_{12} \cdot u_2 \\ i_2 &= h_{21} \cdot i_1 + h_{22} \cdot u_2 \end{aligned} \quad (1)$$

Because the usual values of the quadripole parameters h_{12} and h_{22} have no significant influence on the values of an amplifier's main characteristics, these parameters were ignored in the application.

The effects of capacitors coupling between the signal generator and the amplifier, as well as between the amplifier and the load circuit, are independent and are included in the amplification expression in conventional amplification schemes. These effects consist of each capacitor introducing a low cut pulsation into the Bode diagram. The use of a bipolar transistor in the scheme of an amplification stage, on the other hand, generates a high cut pulsation due to the transistor's parasitic capacitances [15].

The Bode diagrams gain-pulsation and phase-pulsation can be used to study the behaviour of an amplifier while accounting for these pulsations. The use of these diagrams also provides the benefit of determining the amplifier's stability area, [15,16].

The amplifier for that is represents the gain-pulsation and phase-pulsation characteristics has a single amplification stage. Common emitter, common collector, and common base connections were all considered. In the case of each connection, the values of the elements in the diagram can be selected and used to calculate the parameters of the amplification stages, [14–16]. The values of the signal generator and load circuit elements, as well as the coupling elements, will be determined.

2. Determination of the amplifying parameters of the stages in various connections

The stage amplifier parameters in common emitter, common collector and common base connections will be determined in this section.

2.1. Common emitter connection

The main issue concerning common emitter connections will be presented in this paragraph, [19–23]. Figure 2 shows the electronic scheme.

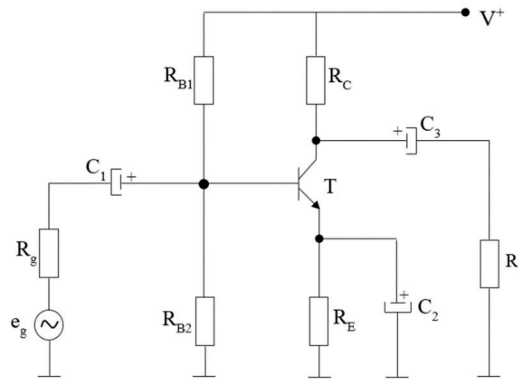


Figure 2. Electronic scheme for common emitter connection.

In this figure, the capacitor C_E , if connected in the scheme, decouples resistance R_E , so that the value of R_E taken into account in the simulation process is given in relation (2).

$$R_E = \begin{cases} 0 & \text{with } C_E \\ R_E & \text{without } C_E \end{cases} \quad (2)$$

Two cases were studied in terms of equivalent resistance from the transistor's base. In the first case, assume that both R_{B1} and R_{B2} are present in the scheme, implying that the transistor polarization is with a resistive divider in the base. In the second case, assume that only R_{B1} is present in the scheme, implying that the transistor is polarized with resistance in the base. Both scenarios are taken into account during the simulation process.

Figure 3 depicts the equivalent scheme in the dynamical regime for a common emitter connection.

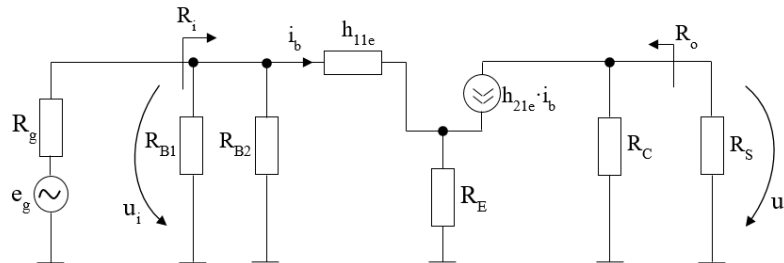


Figure 3. The equivalent scheme in dynamical regime for common emitter connection.

For both cases presented previously, the determination of the input resistance in dynamical regime, R_i , of the common emitter connection is based on relations (3) and (4).

$$R_i = R_{B1} \parallel R_{B2} \parallel [h_{11e} + (1 + h_{21e})R_E] \quad \text{with resistive divider in base} \quad (3)$$

$$R_i = R_{B1} \parallel [h_{11e} + (1 + h_{21e})R_E] \quad \text{with resistance in base} \quad (4)$$

Relation (5) made it possible to calculate the value of the output resistance, R_o , in a dynamical regime.

$$R_o = R_C \quad (5)$$

Relation (6) can be used to calculate the value of voltage amplification, A_u .

$$A_u = - \frac{h_{21e} \cdot (R_C \parallel R_S)}{h_{11e} + (1 + h_{21e})R_E} \quad (6)$$

In relation (6), the dynamical parameters of the used transistor are the input impedance, h_{11e} , and amplification factor, h_{21e} . The choice of load resistance R_S , as shown in relation (7), is dependent on whether the common emitter stage whose operation is being simulated is the final or not from a multiple stage amplifier.

$$R_S = \begin{cases} R_S & \text{if it is the final stage} \\ R_{IN} & \text{if isn't final stage} \end{cases} \quad (7)$$

2.2. Common collector connection

The main issue concerning common collector connections will be presented in this paragraph, [15,16]. Figure 4 shows the electronic scheme.

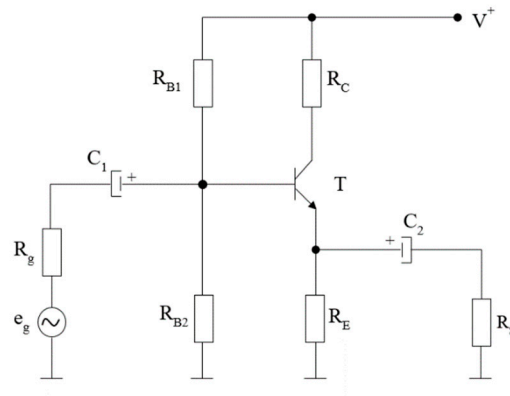


Figure 4. Electronic scheme for common collector connection.

In terms of equivalent resistance from the transistor's base, the same two cases were studied as in the common emitter connection in terms of the presence of R_{B1} and R_{B2} resistance. Both scenarios are taken into account during the simulation process.

Figure 5 depicts the equivalent scheme in the dynamical regime for a common collector connection.

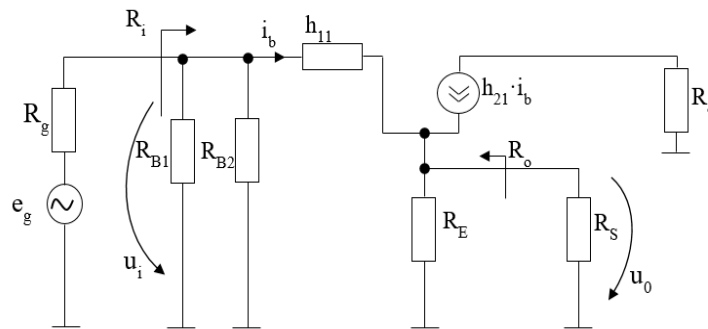


Figure 5. The equivalent scheme in dynamical regime for common collector connection.

For both cases presented previously, the determination of the input resistance in dynamical regime, R_i , of the common collector connection is based on relations (8) and (9).

$$R_i = R_{B1} \parallel R_{B2} \parallel [h_{11c} + (1 + h_{21c}) \cdot R_E \parallel R_S] \quad \text{with resistive divider in base} \quad (8)$$

$$R_i = R_{B1} \parallel [h_{11c} + (1 + h_{21c}) R_E] \quad \text{with resistance in base} \quad (9)$$

The determination of the output resistance in dynamical regime, R_0 , of the common collector connection is based on relations (10) and (11) for both cases presented previously.

$$R_0 = R_E \parallel [h_{11c} + R_{B1} \parallel R_{B2} \parallel R_G] / (1 + h_{21c}) \quad \text{if is the first stage with resistive divider in base} \quad (10)$$

$$R_0 = R_E \parallel [h_{11c} + R_{B1} \parallel R_G] / (1 + h_{21c}) \quad \text{if is the first stage with resistance in base} \quad (11)$$

The choice of generator resistance R_G , as shown in relation (12), is determined by whether or not the common collector stage whose operation is being simulated is the first stage of a multiple stage amplifier.

$$R_G = \begin{cases} R_G & \text{if is the first stage} \\ R_{0,prev} & \text{if isn't first stage} \end{cases} \quad (12)$$

Relation (13) can be used to calculate the value of voltage amplification, A_u .

$$A_u = \frac{u_o}{u_i} = \frac{(R_E \parallel R_S)(1 + h_{21c})}{h_{11c} + (R_E \parallel R_S)(1 + h_{21c})} \quad (13)$$

The dynamical parameters of the used transistor in relation (13) are the input impedance, h_{11c} , and amplification factor, h_{21c} . The choice of load resistance R_S , as shown in relation (14), is determined by whether or not the common collector stage whose operation is being simulated is the final stage of a multiple stage amplifier.

$$R_S = \begin{cases} R_S & \text{if is the final stage} \\ R_{IN} & \text{if isn't final stage} \end{cases} \quad (14)$$

2.3. Common base connection

This paragraph will focus on the main issue of common base connections, [15,21,22]. The electronic scheme is depicted in Figure 6.

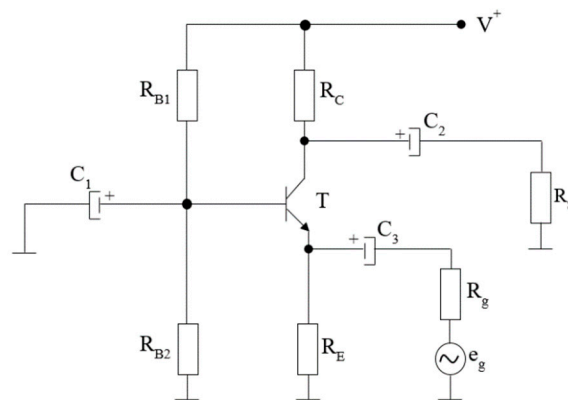


Figure 6. Electronic scheme for common base connection.

Figure 7 depicts the dynamical equivalent scheme for a common base connection.

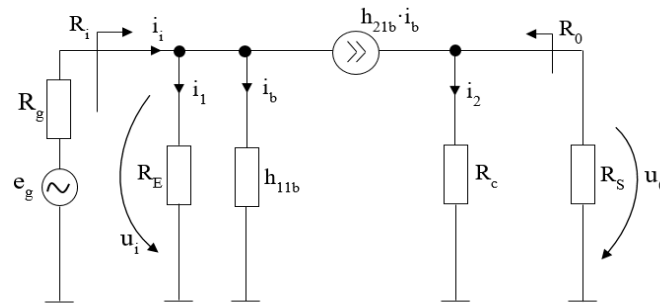


Figure 7. The equivalent scheme in dynamical regime for common base connection.

In relation (15), the determination of the input resistance, R_i , in the dynamical regime in the common base connection is presented. The dynamical parameters of the used transistor in relation (15) are the input impedance, h_{11b} , and amplification factor, h_{21b} .

$$R_i = \frac{h_{11b} \cdot R_E}{h_{11b} + (1 + h_{21b})R_E} \quad (15)$$

The value of the output resistance, R_o , in dynamical regime in the common base connection can be computed from relation (16).

$$R_o = R_C \quad (16)$$

Relation (17) can be used to calculate the value of voltage amplification, A_u .

$$A_u = \frac{h_{21b} \cdot R_C \parallel R_S}{h_{11b}} \quad (17)$$

The choice of load resistance R_s , as shown in relation (18), is determined by whether or not the common base stage whose operation is being simulated is the final stage of a multiple stage amplifier.

$$R_s = \begin{cases} R_S & \text{if is the final stage} \\ R_{IN} & \text{if isn't final stage} \end{cases} \quad (18)$$

3. Presentation of LabVIEW-implemented applications

Figure 8 depicts the main application, which is a study of an amplifier using bipolar transistors, [15]. The application is intended to use three stages of amplifier, but this paper focuses on the situation with only one stage.

The number of stages can be selected in the left-upper part of Figure 8, which in this case contains only one stage. In the left section, there are also five control buttons that allow to select the amplifier's input/output parameters, one of three amplifier stages, and finally a representation of the Bode diagram, [24–27].

3.1. Input/output parameters

The "Input/output parameters" menu is depicted in Figure 8. This menu displays the equivalent scheme for the case where there is only one amplifier stage, as well as the relationships that allow voltage amplification to be calculated.

This menu allows you to select values for generator parameters, R_g and e_g , load resistance, R_s , and coupling capacitors between the generator and the amplifier stage, C_G , as well as the amplifier stage and the load, C_s .

In this figure, the parameters of the amplifier stage that is connected to the generator are also shown: input resistance, R_{i1} , output resistance, R_{o1} , and voltage amplification, A_{u1} .

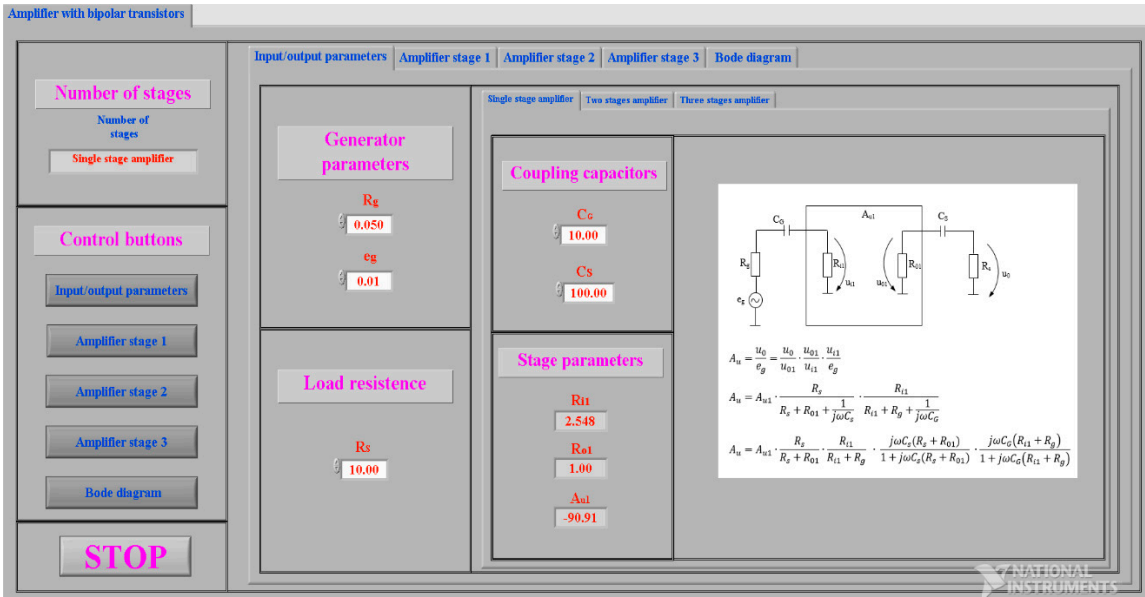


Figure 8. Front panel for input/output parameters.

3.2. Implementation of the presented connections in LabVIEW.

The implementation of all three connections will be presented in this section. For each connection, the front panel and the role of each element, as well as the programming panel, will be described, [28–30].

3.2.1. Implementation of an amplifier stage with a common emitter connection

Figure 9 depicts the "Common emitter" menu, [20,22]. This menu displays the amplifier stage's scheme, as well as the option to view the dynamic regime diagram shown in Figure 10 a), and dynamic parameters for a common emitter connection shown in Figure 10 b).

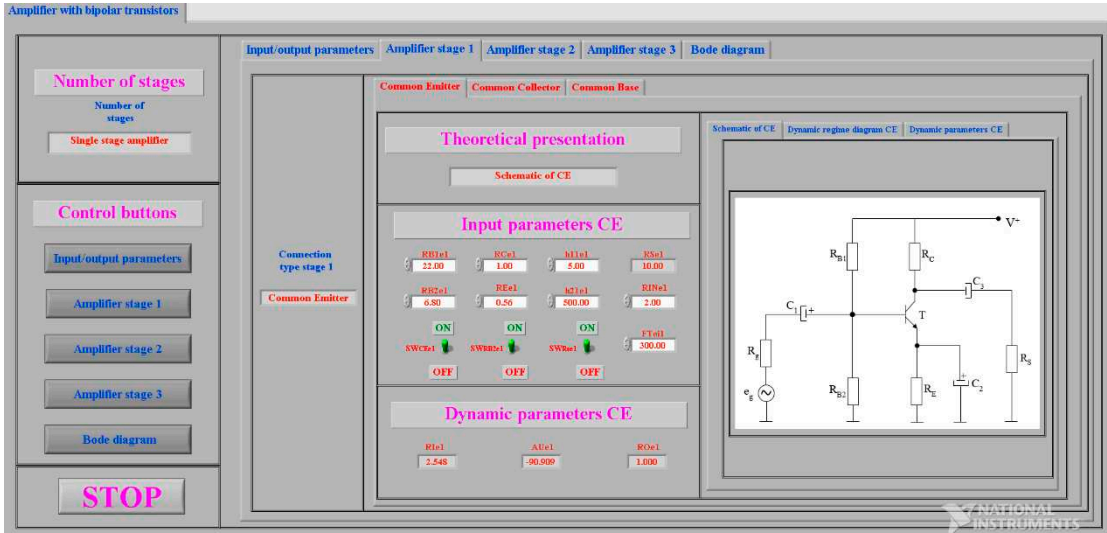


Figure 9. Front panel for common emitter stage parameters.

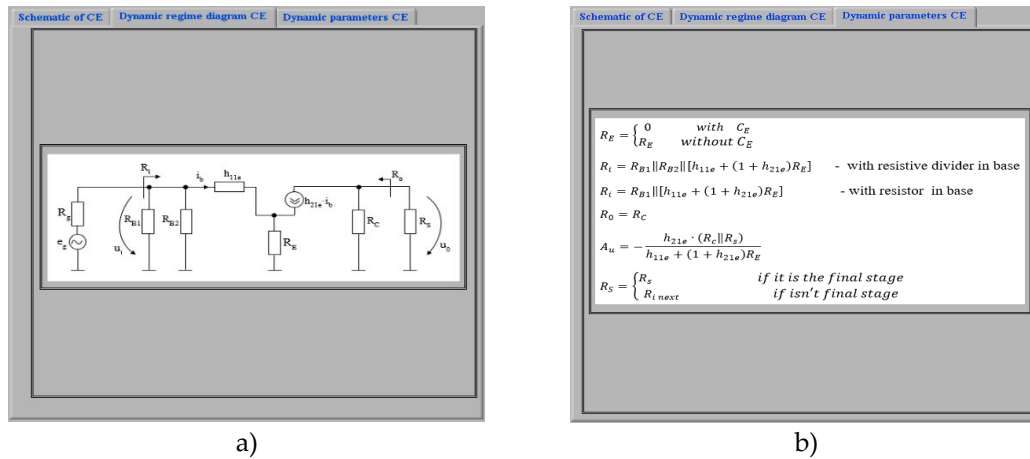


Figure 10. a) Dynamic regime diagram CE, b) Dynamic parameters CE.

Users could select settings for common emitter stage input characteristics including base resistances R_{B1e1} and R_{B2e1} , collector resistance R_{Ce1} , emitter resistance R_{Ee1} , and dynamic regime parameters like input impedance, h_{11e1} , and amplification factor h_{21e1} . The high cutting frequency of the used transistor can be set from F_{Te1} using the data sheet transistor parameters.

The switch "SW_{Rs1}" selects the value of R_s from relation (6) according to relation (7), in the context of calculating stage voltage amplification.

The program allows the user to select the polarization mode of the transistor base with resistive divider or resistance in the base by using the switch "SW_{RB2e1}".

It is also possible to use the "SW_{Ce1}" switch to connect/disconnect the resistor from the emitter and observe the effect on the amplifier parameters.

The dynamic parameters of the amplifier stage are computed based on the values of the input parameters: input resistance, R_{ie1} , output resistance, R_{oe1} , and voltage amplification, A_{ue1} .

Figure 11 a) depicts the program implementation of parameters computed in the common emitter connection. This program employs the "EC1" subroutine, shown in Figure 11 b, which is used to compute the output parameters.

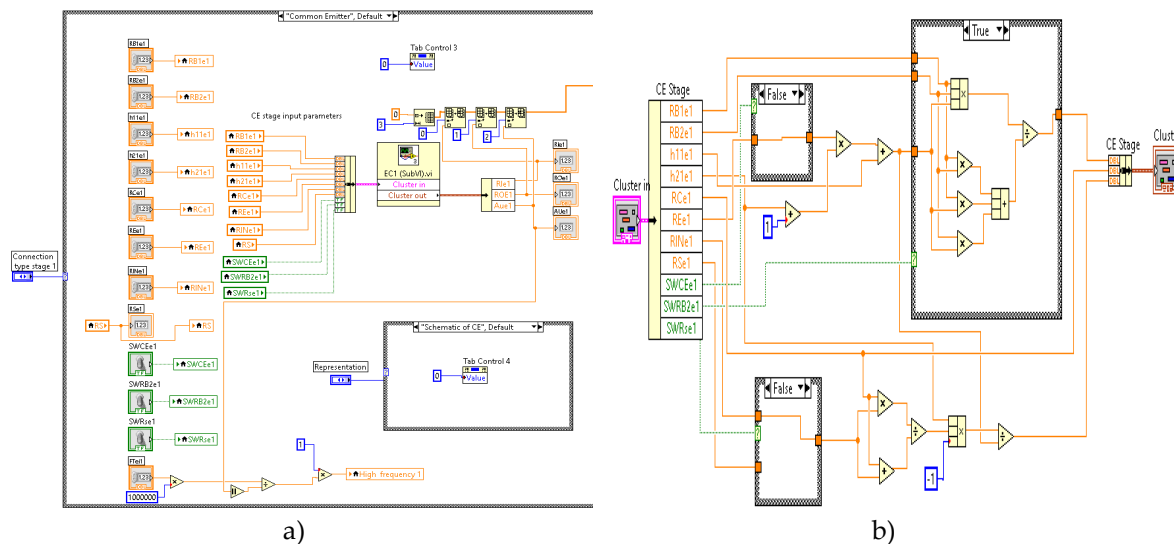


Figure 11. a) Program implementation of computed parameters, b) Subroutine EC1.

3.2.2. Implementation of an amplifier stage with a common collector connection

Figure 12 depicts the "Common collector" menu. This menu displays the amplifier stage's scheme, as well as the option to view the dynamic regime diagram shown in Figure 13 a), and dynamic parameters for a common collector connection shown in Figure 13 b).

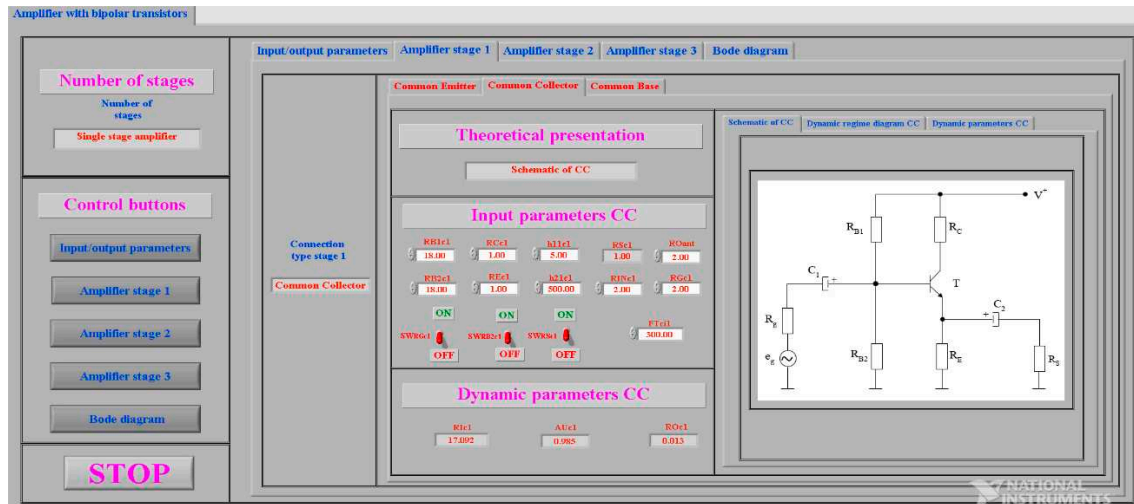


Figure 12. Front panel for common collector stage parameters.

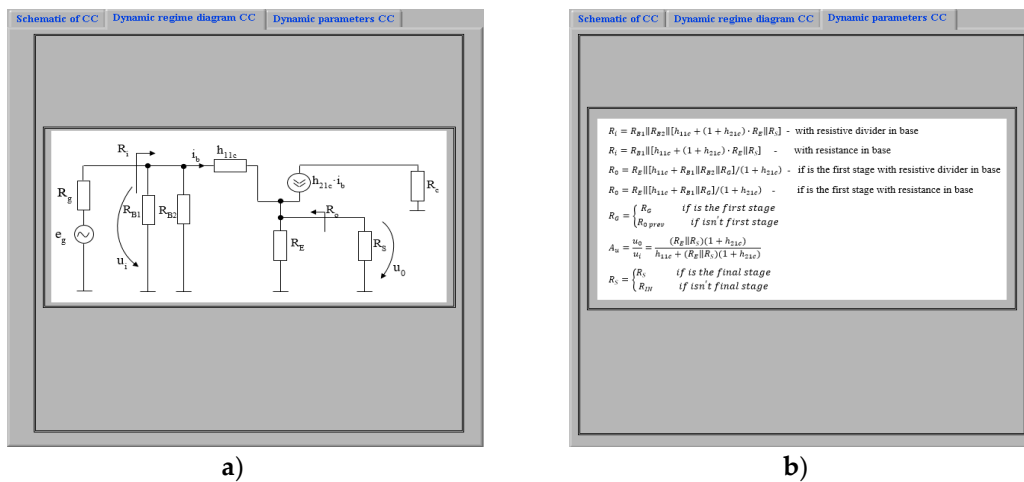


Figure 13. a) Dynamic regime diagram CC, b) Dynamic parameters CC.

Users could select settings for common collector stage input characteristics including base resistances R_{B1c1} and R_{B2c1} , collector resistance R_{Cc1} , emitter resistance R_{Ec1} , and dynamic regime parameters like input impedance, h_{11c1} , and amplification factor h_{21c1} . The high cutting frequency of the used transistor can be set from F_{Tc1} using the data sheet transistor parameters.

The switch "SW_{RS1}" selects the value of R_s from relation (13) according to relation (14), in the context of calculating stage voltage amplification.

The program allows the user to select the polarization mode of the transistor base with resistive divider or resistance in the base by using the switch "SW_{RB2c}".

To compute the value of R_o according to relations (10) and (11), the value of the R_C can be selected as in (12) using the switch "SW_{RG1}".

The dynamic parameters of the amplifier stage are computed based on the values of the input parameters: input resistance, R_{ic1} , output resistance, R_{oc1} , and voltage amplification, A_{vc1} .

Figure 14 a) depicts the program implementation of parameters computed in the common collector connection. This program employs the "CC1" subroutine shown in Figure 14 b), which is used to compute the output parameters.

3.2.3. Implementation of an amplifier stage with a common base connection

Amplifier with bipolar transistors
Input/output parameters
Amplifier stage 1
Amplifier stage 2
Amplifier stage 3
Mode diagram

Number of stages

Number of stages

Single stage amplifier

Control buttons

Input/output parameters

Amplifier stage 1

Amplifier stage 2

Amplifier stage 3

Mode diagram

STOP

Input/output parameters
Amplifier stage 1
Amplifier stage 2
Amplifier stage 3
Mode diagram

Common Emitter
Common Collector
Common Base

Schematic of CB
Dynamic regime diagram CB
Dynamic parameters CB

Theoretical presentation

Schematic of CB

Input parameters CB

R01k1	RCk1	U1k1	ESk1
50.00	2.20	5.00	10.00
R02k1	REk	k21k1	hFEk
12.00	1.00	500.00	2.00

ON

SWk1

OFF

Dynamic parameters CB

g0k1	AUk1	g0k1
0.030	104.762	2.200

Schematic of CB Dynamic regime diagram CB Dynamic parameters CB

Schematic of CB
Dynamic regime diagram CB
Dynamic parameters CB

Schematic of CB
Dynamic regime diagram CB
Dynamic parameters CB

$$i_i = i_1 + i_b + h_{21b} \cdot i_b$$

$$i_1 \cdot R_E = i_b \cdot h_{11b} \Rightarrow i_1 = i_b \cdot \frac{h_{11b}}{R_E}$$

$$i_i = i_b \left(1 + \frac{h_{11b}}{R_E} + h_{21b} \right)$$

$$u_i = i_b \cdot h_{11b}$$

$$R_i = \frac{u_i}{i_i} = \frac{i_b \cdot h_{11b}}{i_b \left(1 + \frac{h_{11b}}{R_E} + h_{21b} \right)} = \frac{h_{11b}}{1 + \frac{h_{11b}}{R_E} + h_{21b}} = \frac{h_{11b} \cdot R_E}{h_{11b} + (1 + h_{21b}) R_E}$$

$$R_o = \frac{u_o}{i_2} = R_c$$

$$u_o = i_2 \cdot R_c = h_{21b} \cdot i_b \cdot R_c \parallel R_S$$

$$A_u = \frac{u_o}{u_i} = \frac{h_{21b} \cdot i_b \cdot R_c \parallel R_S}{i_b \cdot h_{11b}} = \frac{h_{21b} \cdot R_c \parallel R_S}{h_{11b}}$$

$$R_S = \begin{cases} R_S & \text{if is the final stage} \\ R_{IN} & \text{if isn't final stage} \end{cases}$$

Figure 16. a) Dynamic regime diagram CB, b) Dynamic parameters CB.

Users could select settings for common emitter stage input characteristics including base resistances R_{B1b1} and R_{B2b1} , collector resistance R_{Cb1} , emitter resistance R_{Eb1} , and dynamic regime parameters like input impedance, h_{11b1} , and amplification factor h_{21b1} . The high cutting frequency of the used transistor can be set from F_{Tb1} using the data sheet transistor parameters.

The switch "SW_{RSb1}" selects the value of R_s from relation (17) according to relation (18), in the context of calculating stage voltage amplification.

The dynamic parameters of the amplifier stage are computed based on the values of the input parameters: input resistance, R_{ib1} , output resistance, R_{ob1} , and voltage amplification, A_{ub1} .

Figure 17 a) depicts the program implementation of parameters computed in the common base connection. This program employs the "BC1" subroutine shown in Figure 17 b), which is used to compute the output parameters.

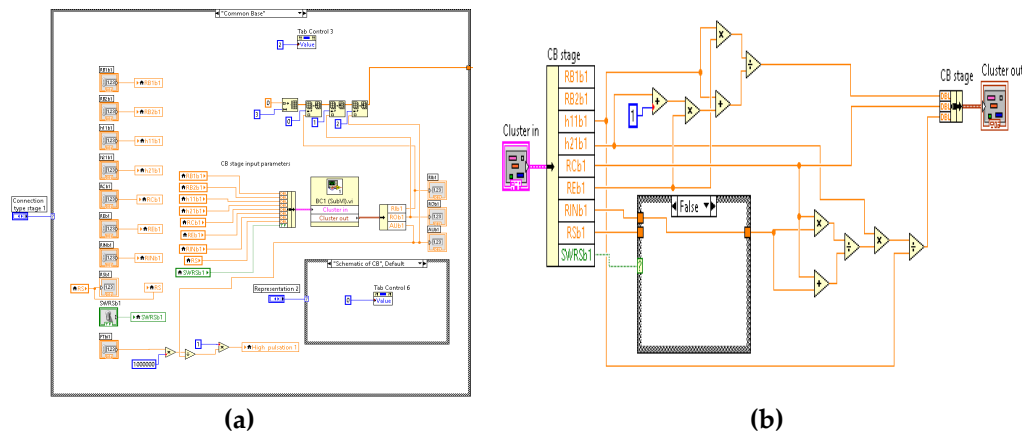


Figure 17. a) Program implementation of computed parameters, b) Subroutine BC1.

3.3. Computing and implementation of Bode diagram

Figure 18 depicts the "Bode diagram" menu, which can be accessed via the control button "Bode diagram", [24–27]. The characteristics "Gain-Frequency" and "Phase-Frequency" are represented in semi logarithmic scale on the right side of this menu (linear scales for gain and phase and logarithmical scale for frequency). The gain and phase dependency for the frequency choose domain are represented by white lines. The red line represents the stability domain, where the phase is between -90 and 90 degrees. A green line represents the position of a specified point on the graphics.

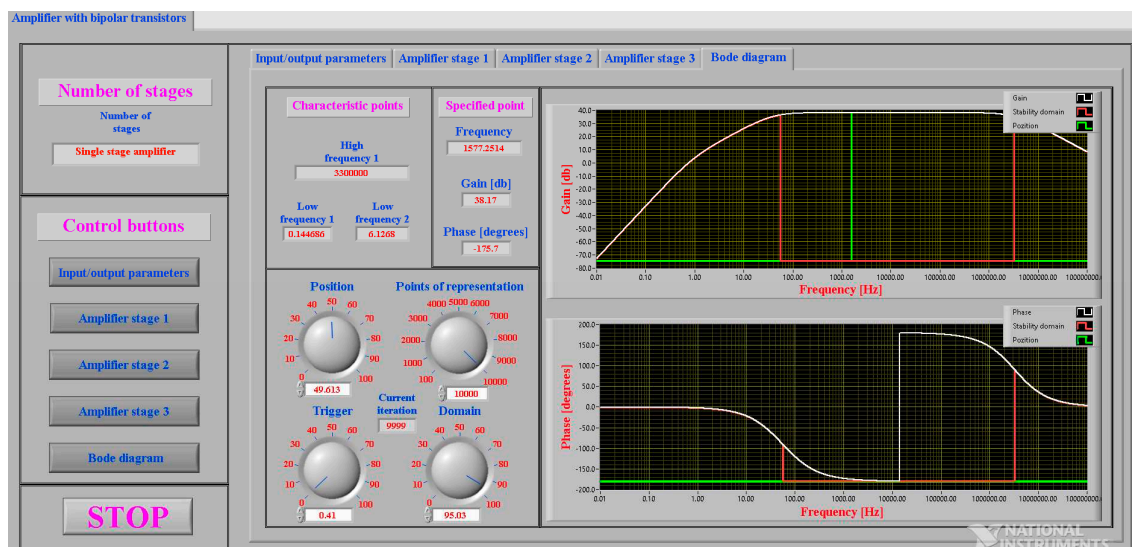


Figure 18. Bode diagram menu.

As seen in the gain-frequency characteristic, there are three characteristic points for a single stage of the amplifier. The first of them represents the high cutting frequency of the used transistor, which was set in the "Amplifier stage 1" menu in Figure 9. The next two characteristic points represent low cut frequency caused by C_G and C_S from Figure 8 and calculated using relations (19) and (20).

$$f_1 = \frac{1}{2 \cdot \pi \cdot C_G \cdot (R_{i1} + R_g)} \quad (19)$$

$$f_2 = \frac{1}{2 \cdot \pi \cdot C_S \cdot (R_{o1} + R_S)} \quad (20)$$

According to relations (21) and (22), the frequency domain is chosen from a minimum frequency f_{\min} to a maximum frequency f_{\max} , providing the possibility of representing all three characteristic points.

$$f_{\min} = \frac{\min\{f_1; \omega f_2\}}{10} \quad (21)$$

$$f_{\max} = 10 \cdot F_{Ti1} \quad (22)$$

To obtain the graphics from Figure 18, the application computes the gain and phase values into a number of points that can be selected from the "Points of representation" knob, which is located in the [100;10000] domain. The graphic resolution of diagrams is defined by the number of points represented, N . Because the frequency has a logarithmic representation, the distance between two consecutive points is defined in relation (23).

$$\Delta_f = \frac{\log(f_{\max}) - \log(f_{\min})}{N - 1} \quad (23)$$

The start point of graphic representation can be set using the "Trigger" knob, which ranges from 0% to 100% of the full range of representation. The domain of representation can be selected from 0% to 100% of the total range of representation using the "Domain" knob.

The "Position" knob can be used to obtain information about a specific point. After selecting a specific point from the "Specific point" menu, information on frequency, gain, and phase can be obtained.

The program implementation of Bode diagrams for a single stage amplifier is shown in Figure 19.

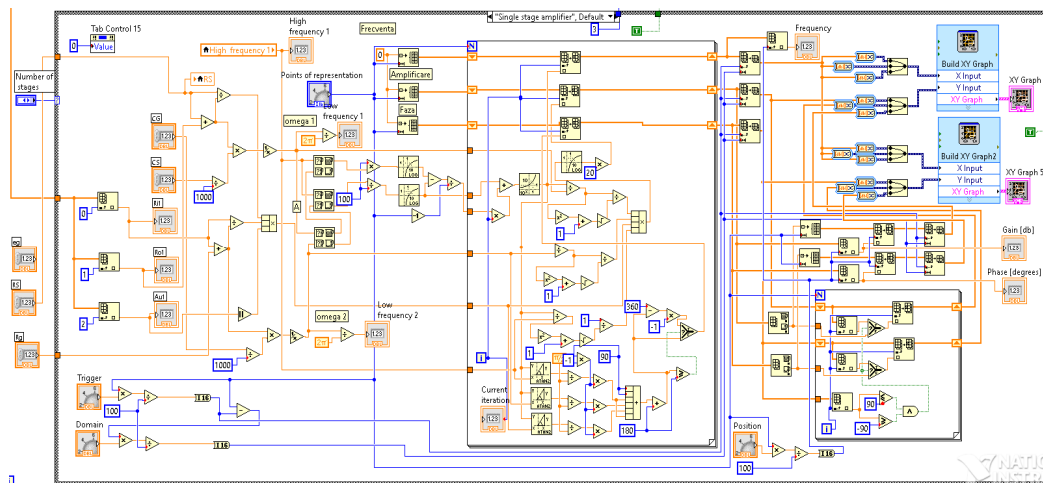


Figure 19. Program implementation of Bode diagram menu.

4. Results of simulation and experimentation

This section contains simulation and experimentation results for the amplifier operating in the connections presented in section 2: common emitter, common collector, and common base, [31–37].

In order to validate the simulation results using the LabVIEW application, a specialized program Multisim was used, as well as experimental measurements using the Electronics Explorer Board. Bode characteristics can be determined using both Multisim and the Electronics Explorer Board. In both simulations and experimental amplifiers, the same transistor was used.

4.1. Simulation and experimentation results for common emitter connection

The input parameter values for this connection were chosen in such a way that the Bode diagram presented two different low pulsations, [15,16]. These values are: for generator parameters, $R_g = 0.05 \text{ k}\Omega$ and $e_g = 10 \text{ mV}$, for load resistance, $R_s = 10 \text{ k}\Omega$, for coupling capacitors between the generator and the amplifier stage, $C_g = 10 \text{ }\mu\text{F}$ and for coupling capacitors between amplifier stage and the load, $C_s = 100 \text{ }\mu\text{F}$.

The parameters values for the common emitter connection are presented in Figure 9.

As previously stated, the structure of the amplifier stage can be modified using the switches SW_{CE1} , SW_{RB2e1} and SW_{RSe1} . Table 1 present the values of the output parameters, R_{Ie1} , A_{Ue1} and R_{Oe1} for all situations in which SW_{CE1} , SW_{RB2e1} and SW_{RSe1} can be established.

Table 1. The values of the output parameters.

	SW_{RB2e1}	SW_{RSe1}	$R_{Ie1} [\text{K}\Omega]$	A_{Ue1}	$R_{Oe1} [\text{K}\Omega]$
	OFF	OFF	20.426	-1.167	1.000
	OFF	ON	20.426	-1.592	1.000
	ON	OFF	5.102	-1.167	1.000
	ON	ON	5.102	-1.592	1.000
	OFF	OFF	4.074	-66.667	1.000
	OFF	ON	4.074	-90.909	1.000
	ON	OFF	2.548	-66.667	1.000
	ON	ON	2.548	-90.909	1.000

Table 1 reveals some conclusions regarding the effect of the three switches on the values of the output parameters.

1. Connecting the capacitor C_2 from figure 20 with the switch SW_{CE1} in the ON state results in a significant increase of A_{Ue1} and a decrease of R_{Ie1} .
2. Selecting the polarization mode of the transistor base with resistive divider by connecting the switch SW_{RB2e1} in ON state causes the input resistance R_{Ie1} to decrease.
3. Switching SW_{RSe1} in ON state conduct to increasing of A_{Ue1} with about 35%.
4. None of the three switches have any effect on the R_{Oe1} value.

The effect of switch SW_{CE1} can be seen in the Bode diagrams in Figures 20–22 for SW_{CE1} to ON, line 8 from Table 1, and in Figures 26–28 for SW_{CE1} to OFF, line 4 from Table 1. All of these figures were obtained through simulations with the presented application and allow for the low and high cut frequency to be determined. These frequencies were determined as the points where the gain was reduced by 3 decibels.

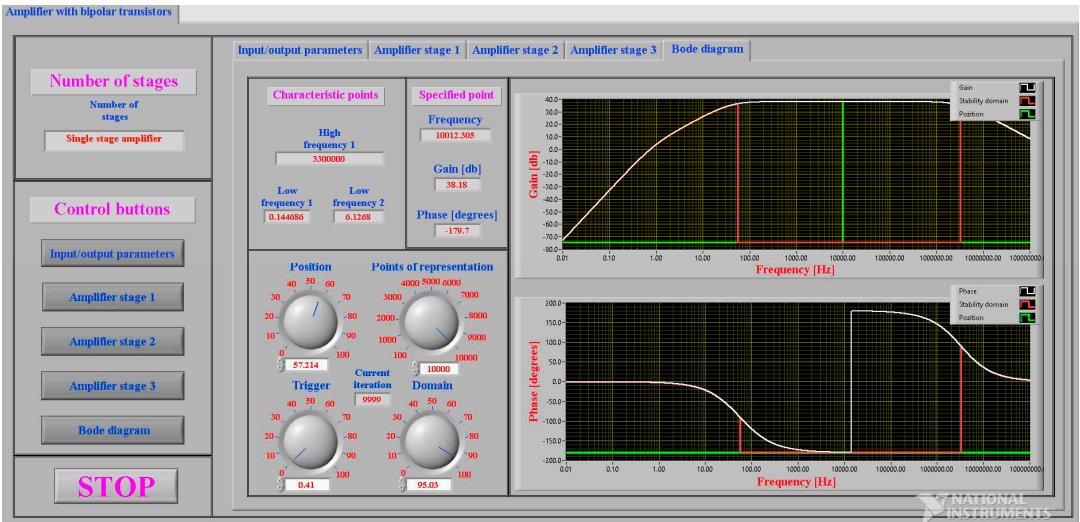


Figure 20. Bode diagram for line 8 from Table 1, for SW_{CE1} to ON, for 10 kHz frequency.

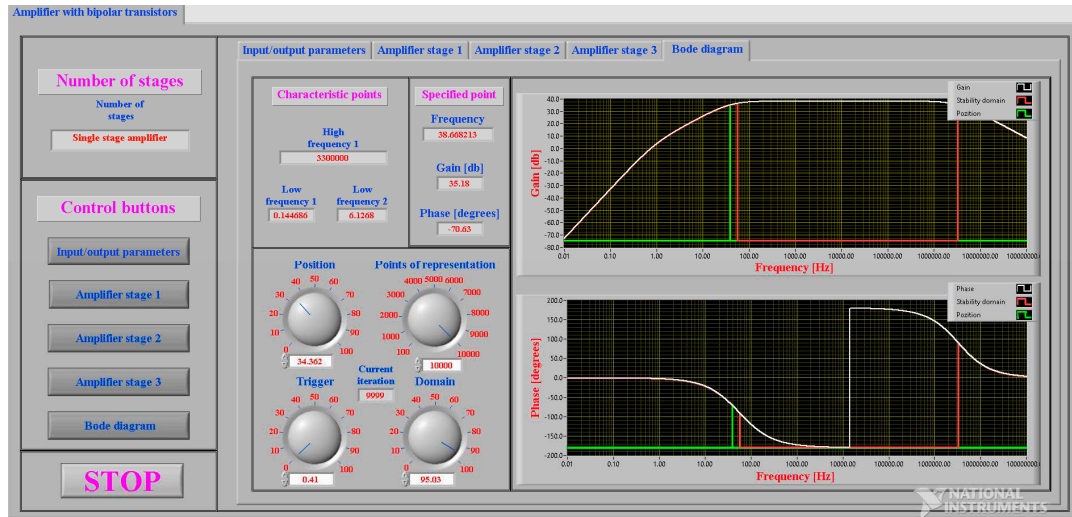


Figure 21. Bode diagram for line 8 from Table 1, for SW_{CE1} to ON, for low cut frequency of 38.66 Hz.

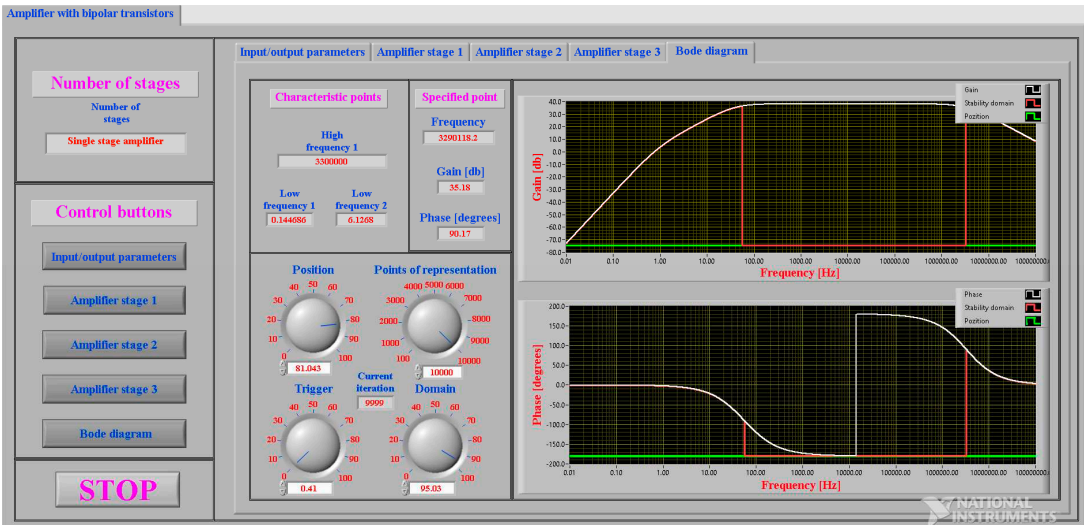


Figure 22. Bode diagram for line 8 from Table 1, for SW_{CE1} to ON, for high cut frequency of 3.29 MHz.

Multisim, a specialized simulation program, was used to verify the LabVIEW simulation results. The simulation results obtained with Multisim are shown in Figure 23.

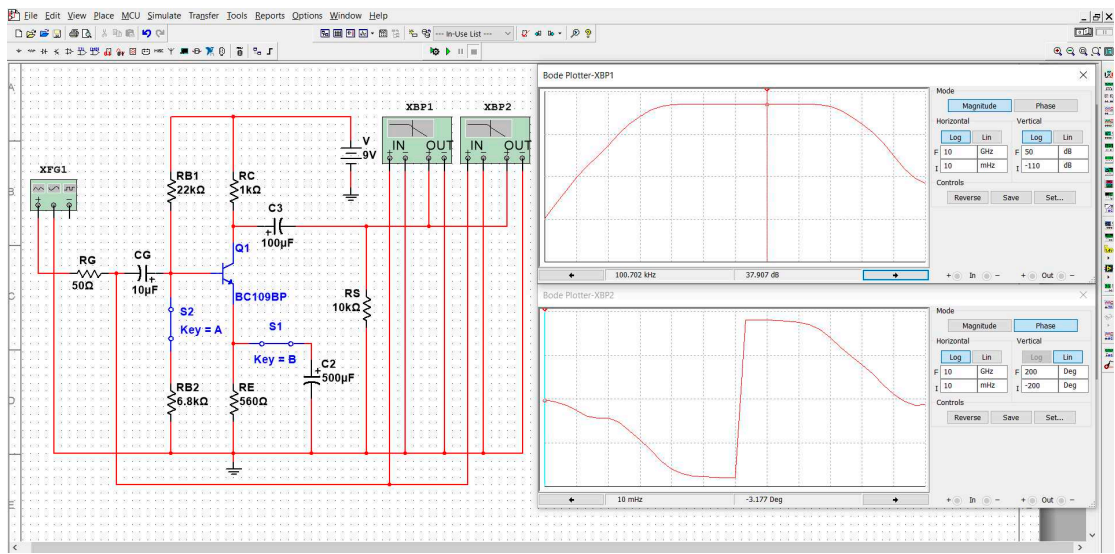


Figure 23. Simulation results for common emitter connection, for SW_{CE1} to ON, using Multisim.

In order to validate the simulation results produced by LabVIEW and Multisim, experimental measurements were performed on a real circuit using an Electronic Explorer Board, which can also be used to determine the Bode characteristics. The Electronic Explorer Board has a frequency range of up to 10 MHz.

The measurement results obtained with Electronic Explorer Board are presented in Figure 24.

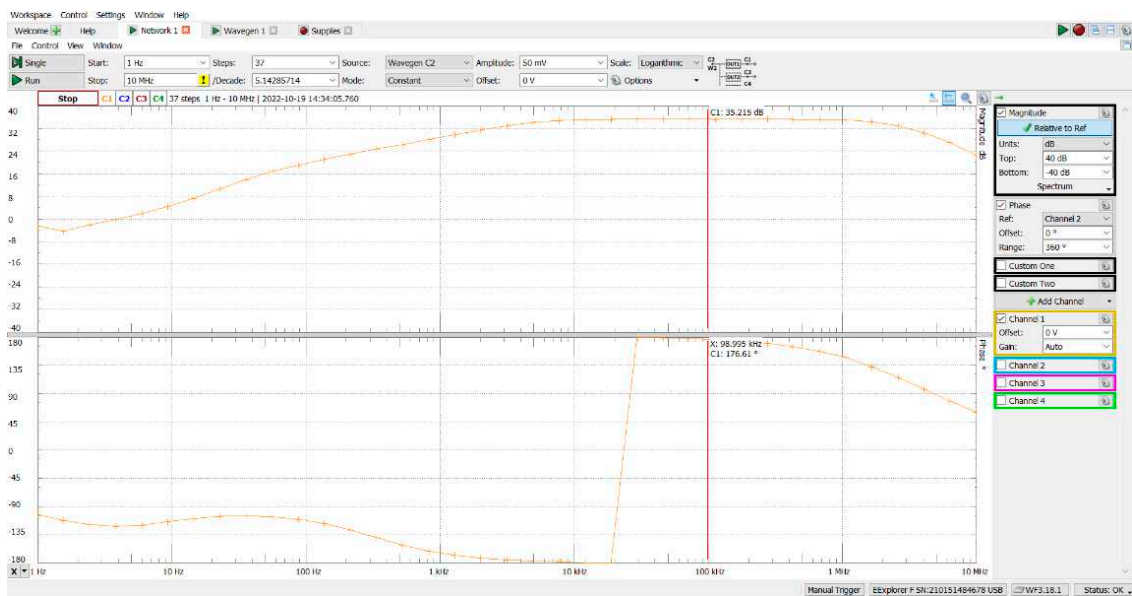


Figure 24. Measurement results for common emitter connection, for SW_{CE1} to ON, using Electronic Explorer Board.

A comparison between the simulations and experimental results can be seen in Figure 25.

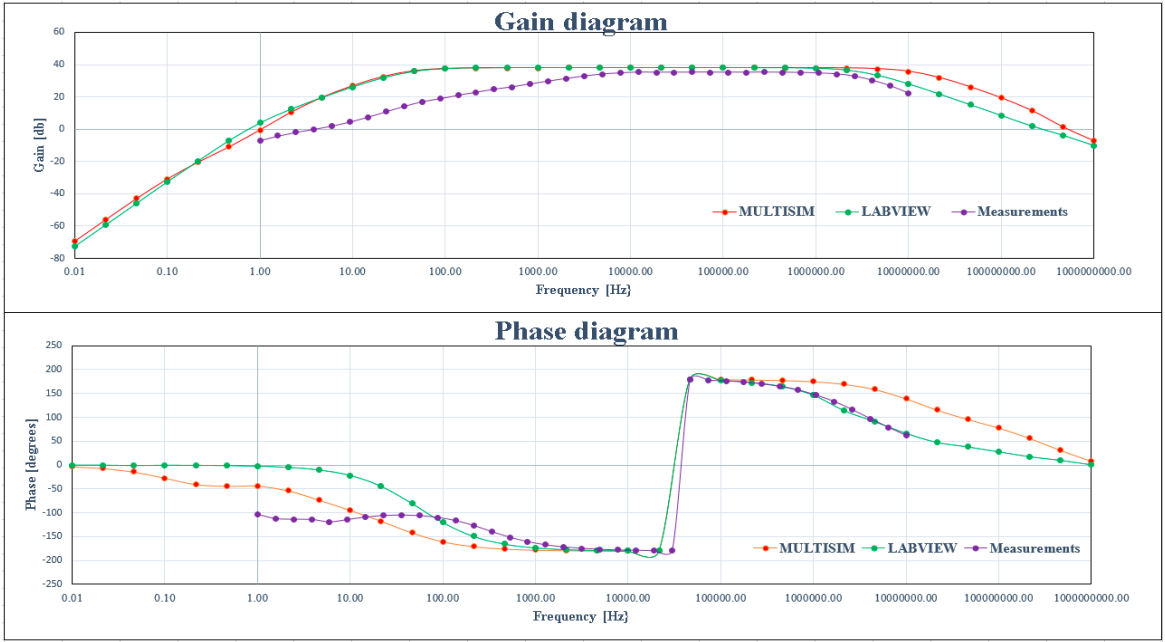


Figure 25. Simulations and experimental results for common emitter connection, for SW_{CE1} to ON.

Analyzing the gain diagram reveals that the simulation and experimental results are very similar at medium and high frequencies. In terms of the phase diagram, both simulations and measurements achieve the same crossing from -180 to 180 degrees, and the LabVIEW simulations and measurements are nearly identical at medium and high frequencies.

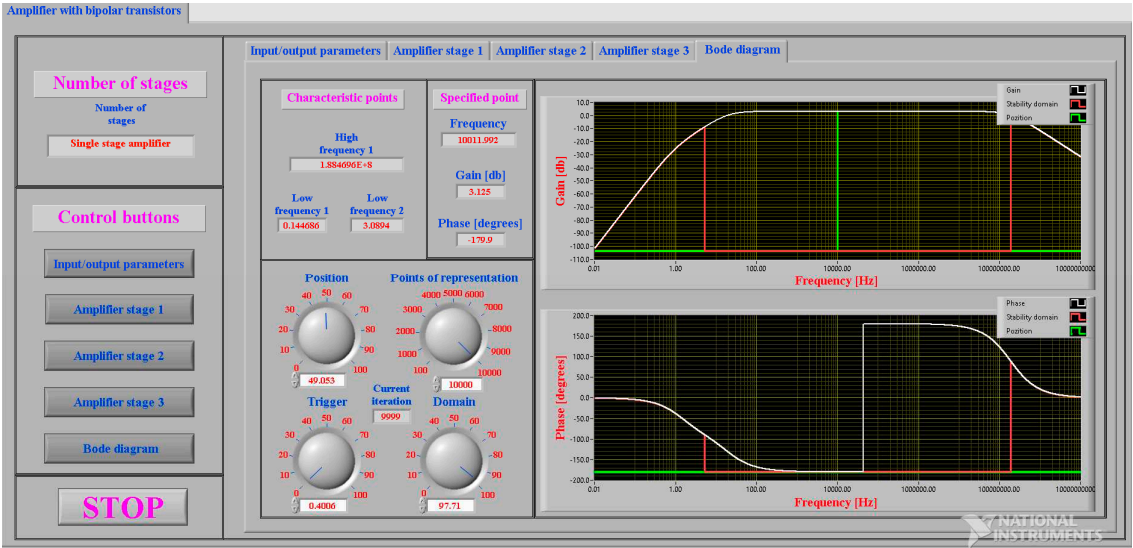


Figure 26. Bode diagram for line 4 from Table 1, for SW_{CE1} to OFF, for 10 kHz frequency.

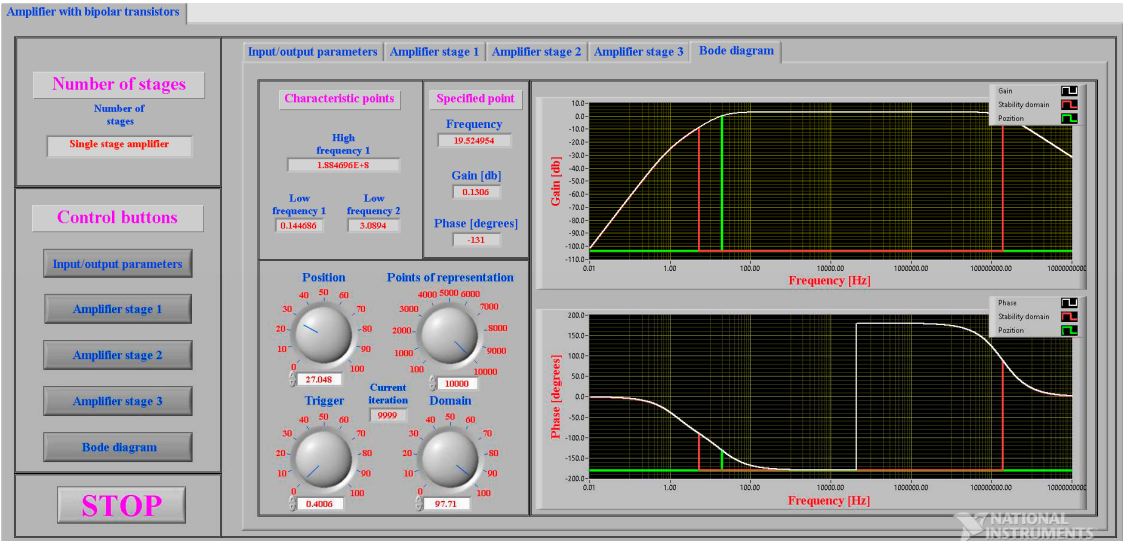


Figure 27. Bode diagram for line 4 from Table 1, for SW_{CE1} to OFF, for low cut frequency of 19.5 Hz.

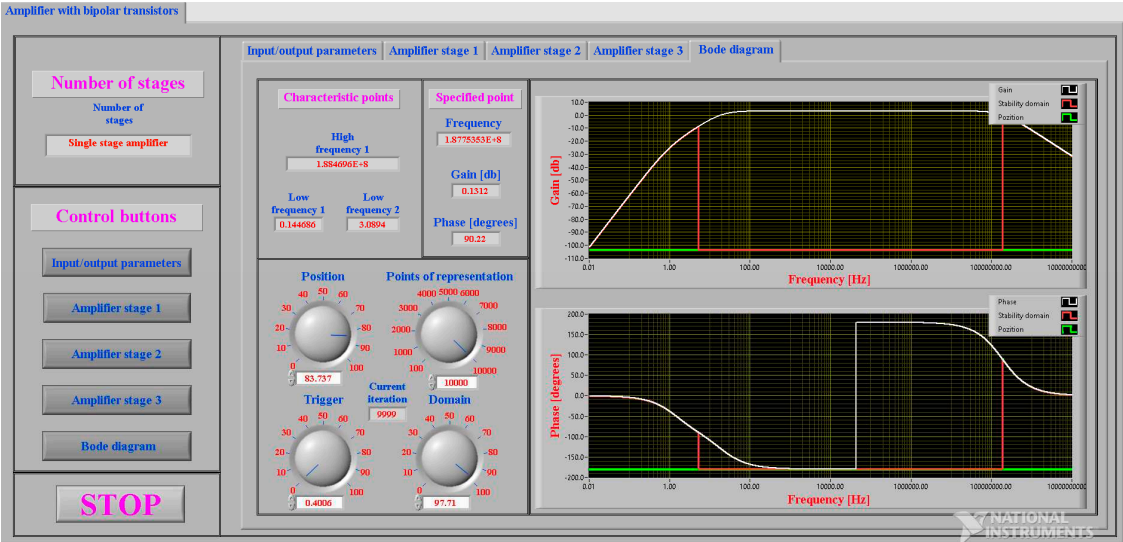


Figure 28. Bode diagram for line 4 from Table 1, for SW_{CE1} to OFF, for high cut frequency of 188.7 MHz.

As in previous situation when SW_{CE1} was ON, a similar comparison between the simulations and experimental results can be made when SW_{CE1} was OFF. The comparison results can be seen in Figure 29.

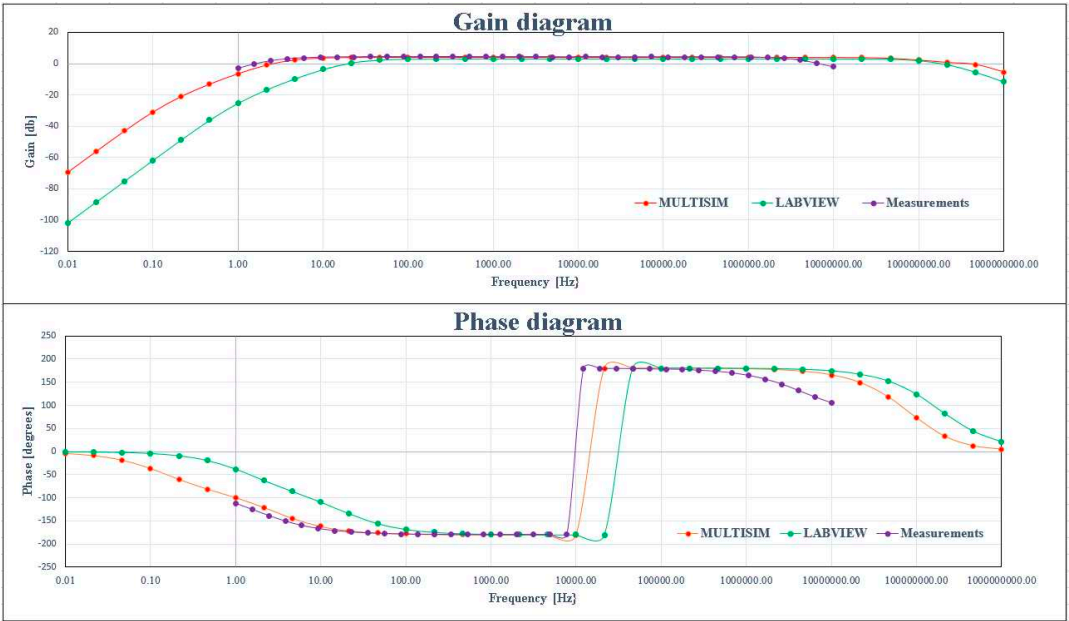


Figure 29. Simulations and experimental results for common emitter connection, for SW_{CE1} to OFF.

Analyzing the gain diagram reveals that the simulation results are very similar at medium and high frequencies. At medium frequencies both the simulations and measurements are very closed. In terms of the phase diagram, both simulations and measurements achieve similar values to crossing from -180 to 180 degrees, and the LabVIEW simulations and measurements are nearly identical at medium frequencies.

4.2. Simulation and experimentation results for common collector connection

The input parameter values for this connection were chosen, like in previous section, in such a way that the Bode diagram presented two different low pulsations, [14–16]. These values are: for generator parameters, $R_g = 0.05\text{ k}\Omega$ and $e_g = 10\text{ mV}$, for load resistance, $R_s = 1\text{ k}\Omega$, for coupling capacitors between the generator and the amplifier stage, $C_g = 10\text{ }\mu\text{F}$ and for coupling capacitors between amplifier stage and the load, $C_s = 10\text{ }\mu\text{F}$.

The parameters values for the common collector connection are presented in Figure 12.

As previously stated, the structure of the amplifier stage can be modified using the switches SW_{RGc1} , SW_{RB2c1} and SW_{RSc1} . Table 2 present the values of the output parameters, R_{Ic1} , A_{Uc1} and R_{Oc1} for all situations in which SW_{RGc1} , SW_{RB2c1} and SW_{RSc1} can be established.

Table 2. The values of the output parameters.

SW_{RGc1}	SW_{RB2c1}	SW_{RSc1}	$R_{Ic1}\text{ [K}\Omega\text{]}$	A_{Uc1}	$R_{Oc1}\text{ [K}\Omega\text{]}$
OFF	OFF	OFF	17.092	0.985	0.013
OFF	OFF	ON	16.815	0.980	0.013
OFF	ON	OFF	8.767	0.985	0.013
OFF	ON	ON	8.694	0.980	0.013
ON	OFF	OFF	17.092	0.985	0.013
ON	OFF	ON	16.815	0.980	0.013
ON	ON	OFF	8.767	0.985	0.013
ON	ON	ON	8.694	0.980	0.013

Table 2 reveals some conclusions regarding the effect of the three switches on the values of the output parameters.

1. Selecting the polarization mode of the transistor base with resistive divider by connecting the switch SW_{RB2c1} in ON state causes the input resistance R_{ic1} to decrease.
2. None of the three switches have any effect on the A_{Uc1} value.
3. None of the three switches have any effect on the R_{Oc1} value.

Figures 30 and 31 show the Bode diagrams generated by simulations for the selected line from Table 2.

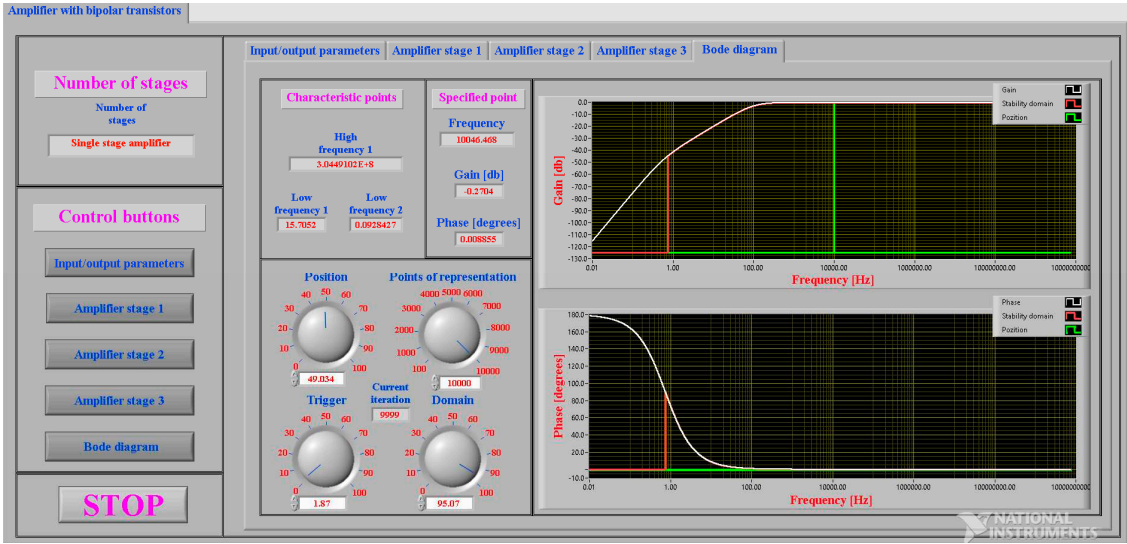


Figure 30. Bode diagram for line 5 from Table 2, for 10 kHz frequency.

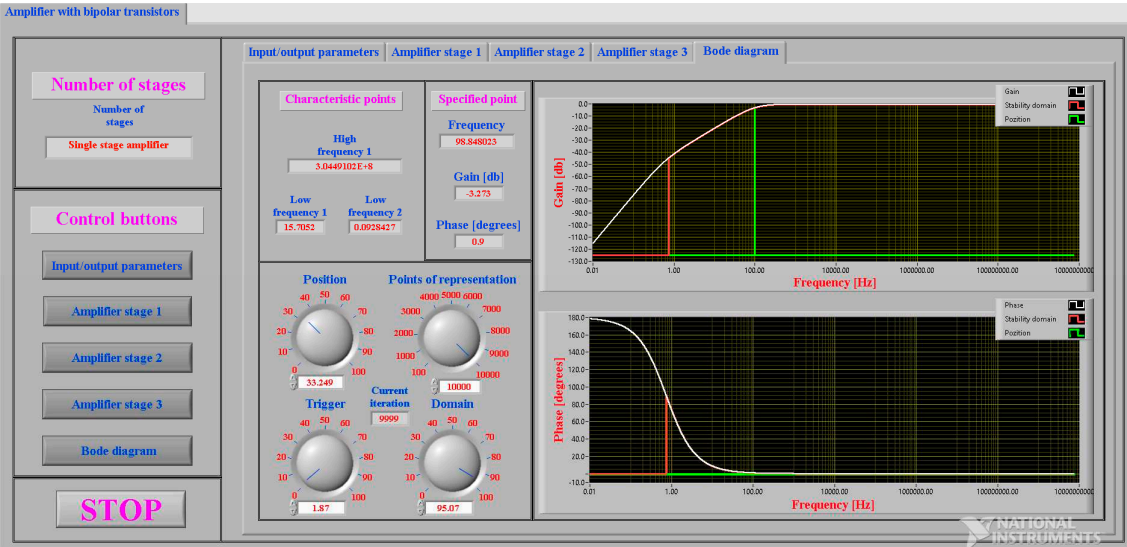


Figure 31. Bode diagram for line 5 from Table 2, for low cut pulsations of 98.85 Hz.

The simulation results for common collector connection obtained with Multisim are shown in Figure 32.

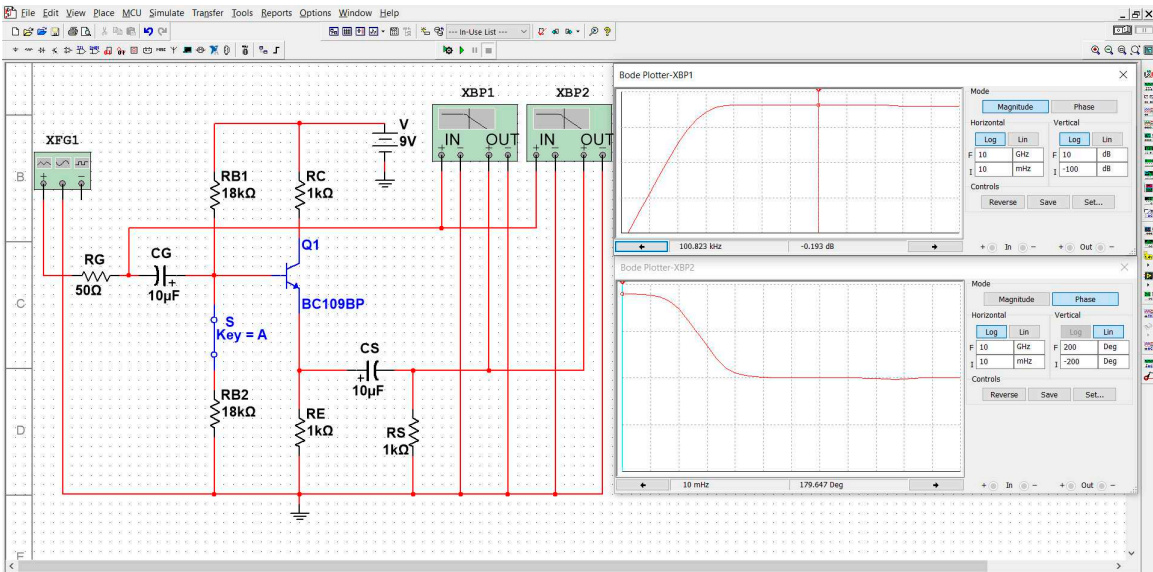


Figure 32. Simulation results for common collector connection, using Multisim.

Experimental measurements were performed on a real circuit using an Electronic Explorer Board, which can also be used to determine the Bode characteristics. The measurement results obtained with Electronic Explorer Board are presented in Figure 33.

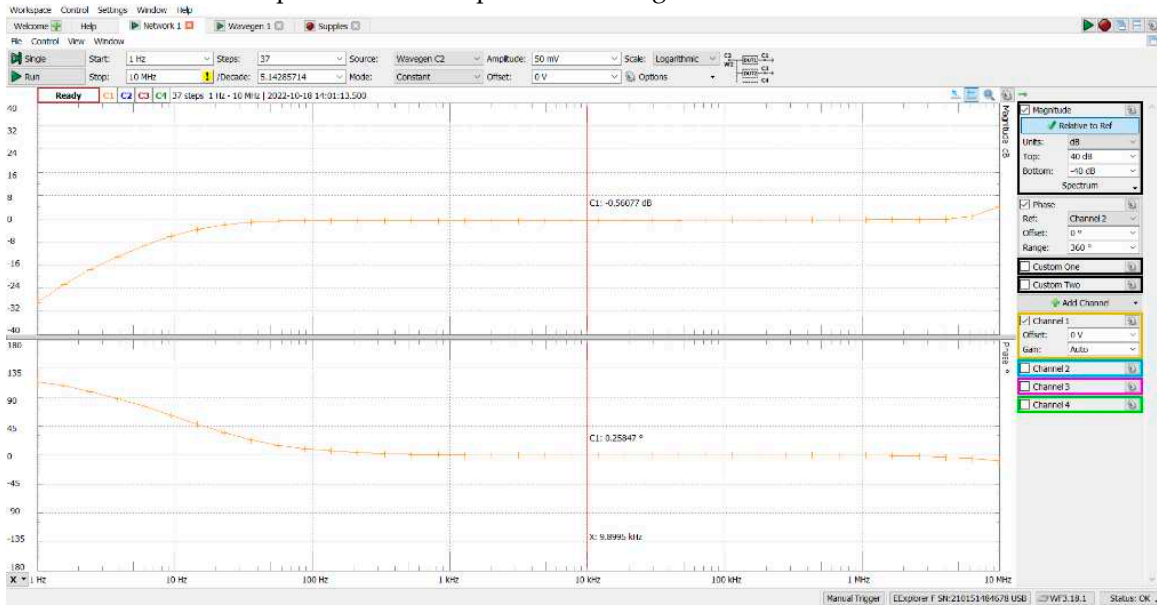


Figure 33. Measurement results for common collector connection, using Electronic Explorer Board.

A comparison between the simulations and experimental results can be seen in Figure 34.

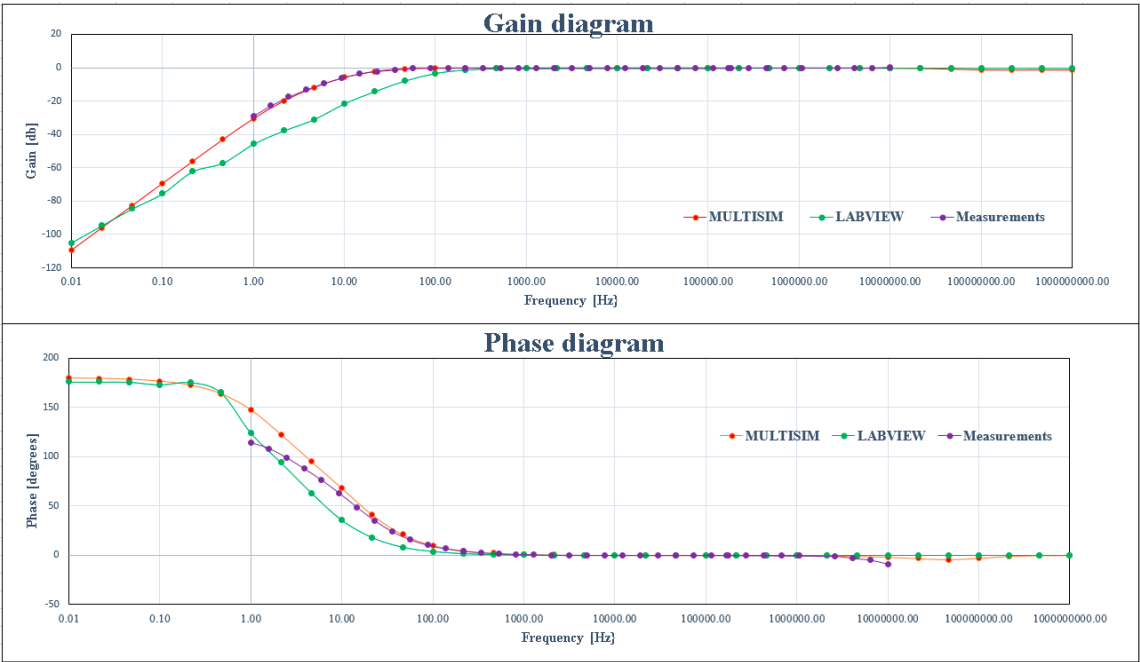


Figure 34. Simulations and experimental results for common collector connection.

Analyzing the gain diagram reveals that the simulation and experimental results are similar at all frequencies.

4.3. Simulation and experimentation results for common base connection

The input parameter values for this connection were chosen, like in previous sections, in such a way that the Bode diagram presented two different low pulsations, [14–16]. These values are: for generator parameters, $R_g = 0.05\text{ k}\Omega$ and $e_g = 10\text{ mV}$, for load resistance, $R_s = 10\text{ k}\Omega$, for coupling capacitors between the generator and the amplifier stage, $C_G = 1\text{ }\mu\text{F}$ and for coupling capacitors between amplifier stage and the load, $C_s = 100\text{ }\mu\text{F}$.

The parameters values for the common base connection are presented in Figure 15.

As previously stated, the structure of the amplifier stage can be modified using the switch SW_{RSb1} . Table 3 present the values of the output parameters, R_{ib1} , A_{Ub1} and R_{Ob1} for the two situations in which SW_{RSb1} can be established.

Table 3. The values of the output parameters.

SW_{RSb1}	$R_{ib1}\text{ [K}\Omega\text{]}$	A_{Ub1}	$R_{Ob1}\text{ [K}\Omega\text{]}$
OFF	0.013	104.762	2.200
ON	0.013	180.328	2.200

Table 3 reveals some conclusions regarding the effect of the switch SW_{RSb1} on the values of the output parameters.

1. The state of the switch SW_{RSb1} has no effect on the input resistance R_{ib1} or the output resistance R_{Ob1} .
 2. The ON state of switch SW_{RSb1} causes the A_{Ub1} value to increase.
- Figures 35–37 show the Bode diagrams generated by simulations for the selected line from Table 3.

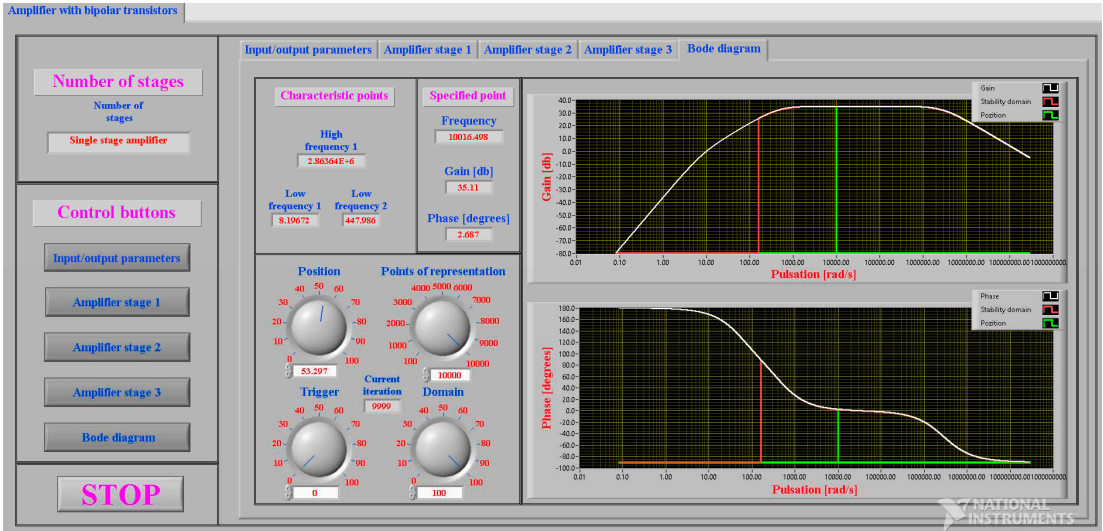


Figure 35. Bode diagram for line 1 from Table 3, for 10 kHz frequency.

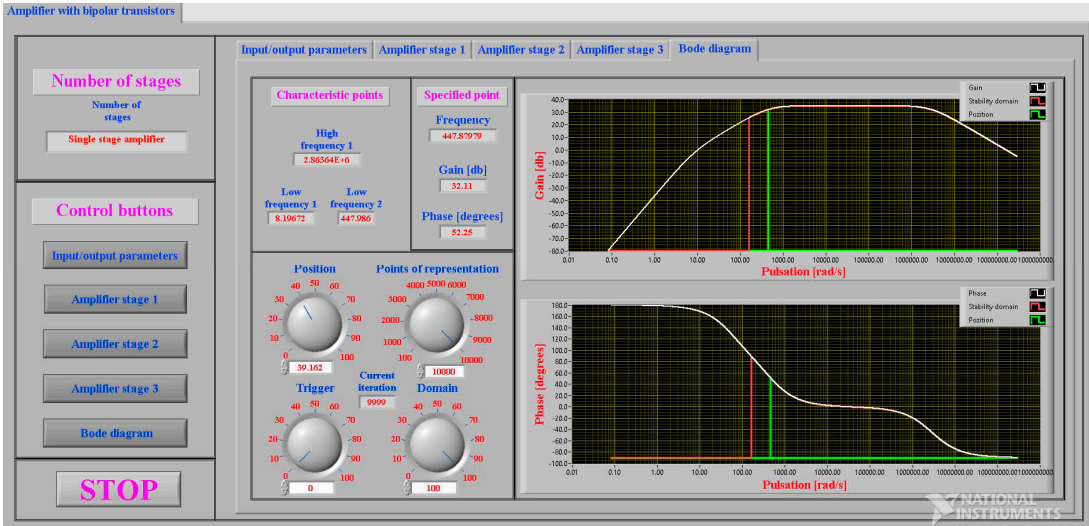


Figure 36. Bode diagram for line 1 from Table 3, for low cut pulsations of 447.9 Hz.

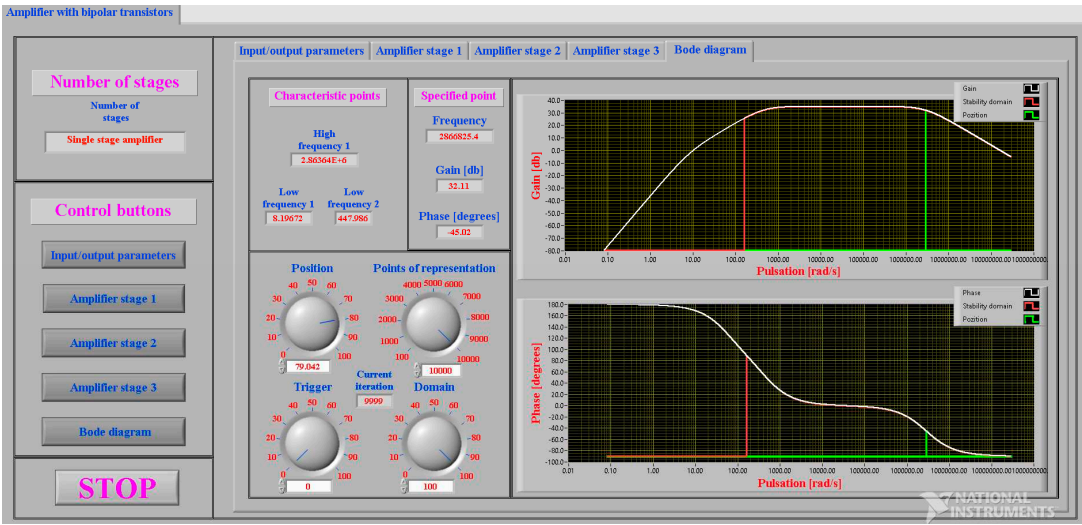


Figure 37. Bode diagram for line 1 from Table 3, for high cut pulsations of 2.86 MHz.

The simulation results obtained with Multisim are shown in Figure 38.

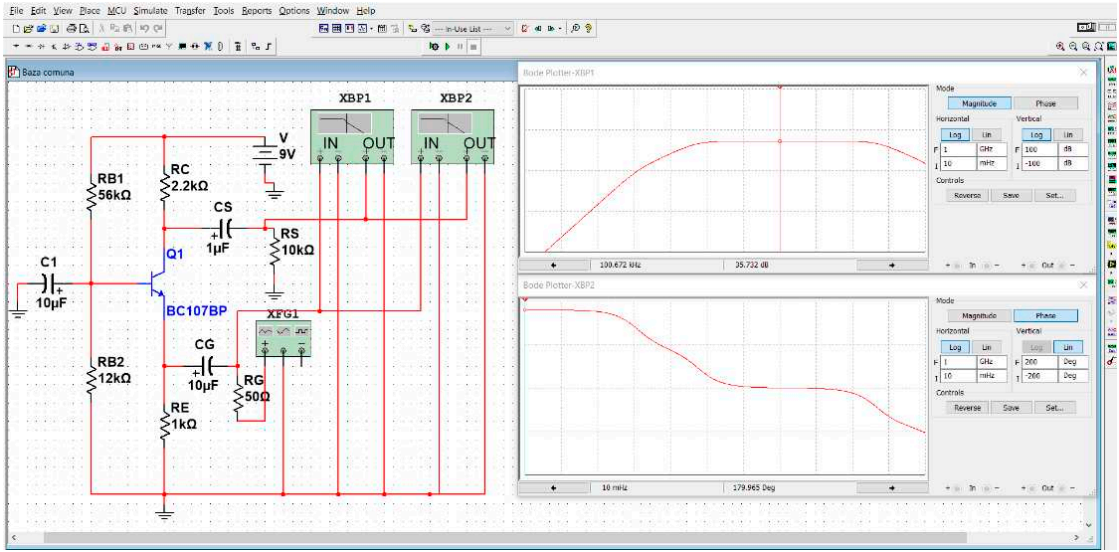


Figure 38. Simulation results for common base connection, using Multisim.

As in previous connections, to validate the simulation results produced by LabVIEW and Multisim, experimental measurements were performed on a real circuit using an Electronic Explorer Board.

The measurement results obtained with Electronic Explorer Board are presented in Figure 39.

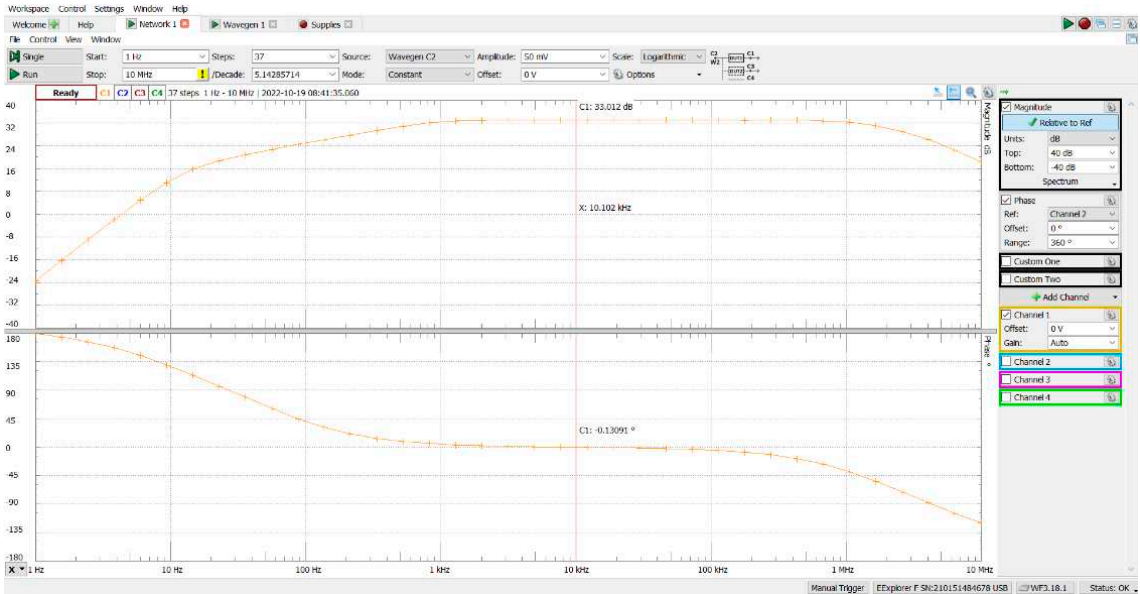


Figure 39. Measurement results for common base connection, using Electronic Explorer Board.

A comparison between the simulations and experimental results can be seen in figure 40.

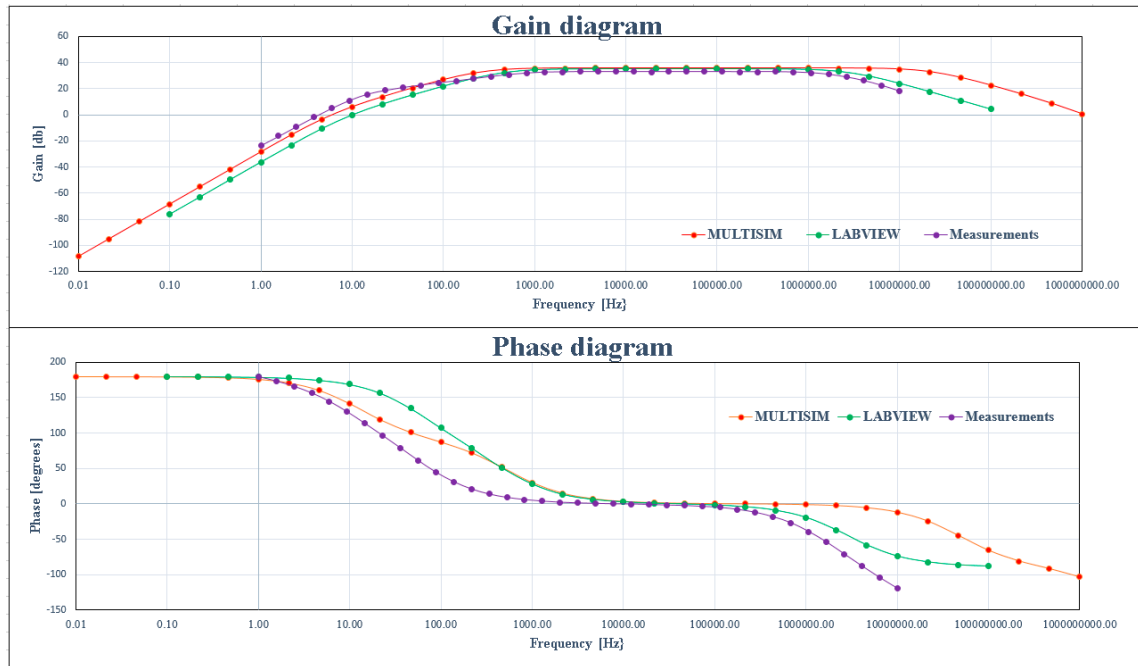


Figure 40. Simulations and experimental results for common base connection.

Analyzing the gain diagram reveals that the simulation and experimental results are similar at low and medium frequencies. At high frequencies the LabVIEW simulations and measurements are nearly identical.

In terms of the phase diagram, both simulations and measurements have the same behavior from 180 to -180 degrees.

5. Conclusions

The investigation of the functionality of an amplifier with discrete components in various connections is a complex process due to the large number of circuit elements whose values influence the amplifier's output parameters.

This paper describes a LabVIEW application that calculates the output parameters of a single stage amplifier, such as input and output resistance, voltage amplification, gain-frequency and phase-frequency Bode diagrams.

The stage amplifier can be studied in three different configurations: common emitter, common collector and common base. Different transistor polarisation possibilities can be selected for each connection. The application allows for the generation of various transistor polarization schemes by coupling some circuit elements with switches.

The amplifier's stability zone, as well as the gain and phase amplifier for a given frequency value, can be determined using Bode diagrams.

A specified single stage amplifier can be designed by changing both the configuration of the amplifier as well as the value of some circuit element.

Because the application allows each connection to visualize the electronic scheme, the mathematical relations for determining the output parameters, and the dynamical scheme, it can be used for educational purposes.

In order to validate the simulation results using the LabVIEW application, a specialized program Multisim was used, as well as experimental measurements using the Electronics Explorer Board. Both Multisim and Electronics Explorer Board can determine Bode characteristics. In both simulations and experimental amplifiers, the same schemes with the same transistor was used.

This paper demonstrated that the LabVIEW application can produce similar simulate results using Multisim and also measured results using Electronics Explorer Board. The application

described in this article is an innovative type tool that may be used as a learning tool because it performs circuit analysis in simulation software and experiments comparisons.

Author Contributions: Conceptualization, Cuntan C. and Panoiu C.; methodology, Panoiu M.; software Panoiu C. and Cuntan C.; validation Baci I. and Mezinescu S.; writing—original draft preparation Panoiu M. and Mezinescu S.; writing—review and editing, Cuntan C., Panoiu C. and Panoiu M.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

u_1	input voltage
u_2	output voltage
i_1	input current
i_2	output current
$h_{11}, h_{12}, h_{21}, h_{22}$	quadrupole "h" parameters
$h_{11e}, h_{12e}, h_{21e}, h_{22e}$	quadrupole "h" parameters in common emitter connection
$h_{11c}, h_{12c}, h_{21c}, h_{22c}$	quadrupole "h" parameters in common collector connection
$h_{11b}, h_{12b}, h_{21b}, h_{22b}$	quadrupole "h" parameters in common base connection
R_i, R_o	input and output resistance
R_{ie1}, R_{oe1}	input and output resistance in common emitter connection
R_{ic1}, R_{oc1}	input and output resistance in common collector connection
R_{ib1}, R_{ob1}	input and output resistance in common base connection
R_g	generator resistance
R_d	dynamic resistance
e_g	generator voltage
C_1, C_3	coupling capacitors
C_2	decoupling capacitors
R_{B1}, R_{B2}	resistors connected on base
R_{B1e1}, R_{B2e1}	resistors connected on base in common emitter connection
R_{B1c1}, R_{B2c1}	resistors connected on base in common collector connection
R_{B1b1}, R_{B2b1}	resistors connected on base in common base connection
R_C	resistors connected on collector
R_{Ce1}	resistors connected on collector in common emitter connection
R_{Cc1}	resistors connected on collector in common collector connection
R_{Cb1}	resistors connected on collector in common base connection
R_E	resistors connected on emitter
R_{Ee1}	resistors connected on emitter in common emitter connection
R_{Ec1}	resistors connected on emitter in common collector connection
R_{Eb1}	resistors connected on emitter in common base connection
R_s	load resistor
A_u	voltage amplification
A_{ue1}	voltage amplification in common emitter connection
A_{uc1}	voltage amplification in common collector connection
A_{ub1}	voltage amplification in common base connection
$R_{i,next}, R_{IN}$	input resistance of the next stage
$R_{o,prev}$	output resistance of the previous stage
C_G	coupling capacitors between the generator and the amplifier stage
C_s	coupling capacitors between the amplifier stage and the load
R_{i1}	input resistance
R_{o1}	output resistance
$SW_{RSe1}, SW_{RB2e1}, SW_{CEe1}$	used switches in common emitter connection
$SW_{RSc1}, SW_{RB2c}, SW_{RGC1}$	used switches in common collector connection

SW_{RSb1}	used switch in common base connection
F_{Tei1}	high cutting frequency transistor in common emitter connection
F_{Tci1}	high cutting frequency transistor in common collector connection
F_{Tbi1}	high cutting frequency transistor in common base connection
ω_1, ω_2	low cut pulsations of the stage
$\omega_{min}, \omega_{max}$	minimum and maximum pulsation domain
$\Delta\omega$	graphic resolution of the pulsation axis
N	number of points represented

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