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Article

Simulation of Total Ionizing Dose Effects Technique for CMOS Inverter Circuit

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Abstract: The total ionizing dose (TID) effect significantly impacts the electrical parameters of fully depleted silicon on insulator (FDSOI) devices and even invalidates the on-off function of devices. At present, most of the irradiation research on the circuit level is focused on the single event effect, and the research on the total ionizing dose effect is very little. Therefore, this study mainly analyzes the influence of TID effects on a CMOS inverter circuit based on 22 nm FDSOI transistors. First, we constructed and calibrated an N-type FDSOI metal-oxide semiconductor (NMOS) structure and P-type FDSOI metal-oxide semiconductor (PMOS) structure. The transfer characteristics and trapped charge distribution of these devices were studied under different irradiation doses. Next, we studied the TID effect on an inverter circuit composed of these two MOS transistors. The simulation results show that when the radiation dose is 400 krad (Si), the logic threshold drift of the inverter is approximately 0.052 V. These results help further investigate the impact on integrated circuits in the irradiation environment.

Keywords: Total ionizing dose effect; FDSOI devices; Inverter

1. Introduction

Power electronics technology is widely used in the aerospace and other fields. Owing to the influence of irradiation, the electrical performance of electronic devices, which operate in an irradiation environment, are disturbed and degraded, resulting in the failure of the entire integrated circuit system. The cumulative effect of electrical performance degradation of electronic devices is caused by high-energy rays and charged particles, that is, the total ionizing dose (TID) effect[1–3], which is the main factor affecting the life of electronic devices and cannot be eliminated. Owing to the presence of a buried oxygen (BOX) layer, FDSOI technology separates the substrate layer from the top silicon layer, resulting in good radiation resistance[4–6]. Therefore, FDSOI devices are used as the basic research objects. At present, most circuit-level radiation studies focus on the single particle effect, and few studies have investigated the TID effect. Inverters are widely used most basic MOS circuit structures[7,8]. Therefore, analyzing the impact of the total dose effect, in integrated circuit systems, which is based on the TID effect of inverter circuits is important.

2. Device Structure and Calibration

2.1. Device Structure

The 3D simulation models of the 22 nm fully depleted silicon on insulator (FDSOI) NMOSFET and PMOSFET were established using Sentaurus software, as shown in Figure 1. The source, drain, N well, and P well of the devices were doped with Gaussian doping, and the device substrate was uniformly doped. Some process parameters, such as the doping concentration in the active region and well depth, are the core secrets of the foundry. Therefore, during building of the device model, setting some process parameters through empirical values and then comparing and calibrating them

with the electrical characteristic curve measured in the experiment is necessary to finally determine the device parameters.

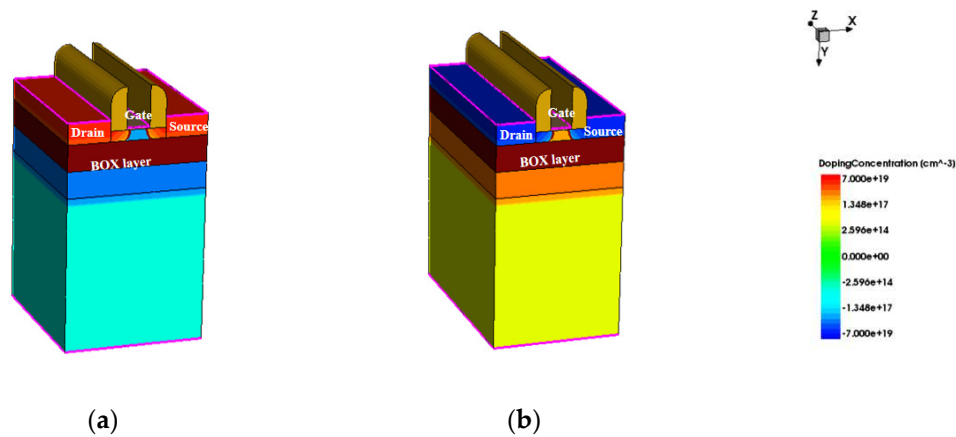


Figure 1. Structure of (a) NMOS and (b) PMOS.

These devices are all based on 22 nm process nodes. The gate length was 22 nm, and the equivalent oxide thickness (EOT) was 20 Å. The gate width of devices (a) and (b) were 160 nm and 220 nm. A 10 nm top silicon layer was just above the BOX layer, and the spacer width was 10 nm. The BOX layers of devices (a) and (b) were 20 nm SiO₂.

2.2. Calibration Model

To ensure the accuracy of the established model, a B1500 semiconductor tester was used to test the saturation zone and linear zone transfer characteristic curves of the non-irradiated 22nm FDSOI. The test device diagram is shown in Figure 2. The specific testing conditions are as follows. Setting the drain voltage of the NMOS device to 0.8V and 0.1V, and the gate voltage scanning range to 0V~1.0V, testing the changes in drain current. Similarly, Setting the drain voltage of the PMOS device to -0.8V and -0.1V, and the gate voltage scanning range to -1.0 V~0 V, Testing the changes in drain current.

As the doping concentration and specific process of the device are confidential documents of the factory, based on the layout file, as shown in Figure 3, we can understand the size of the device, and use this as a basis to obtain the structural model of the device in TCAD software through structural modeling, as shown in 0. To further obtain a more accurate physical model, we need to modify and calibrate the device's work function, doping concentration and mobility in the source and drain regions. Figure 4 and Figure 5 show comparison between the TCAD simulation and experimental results of the 22 nm FDSOI device. Compare the threshold voltage parameters, Compared with the experimental data, the threshold voltage errors of the NFET and PFET devices were 1.82% and 5.05%, respectively, which were less than 10%. In conclusion, the electrical characteristic parameters of the built device simulation model satisfied these requirement. The final determined device parameter information is shown in Table 1.

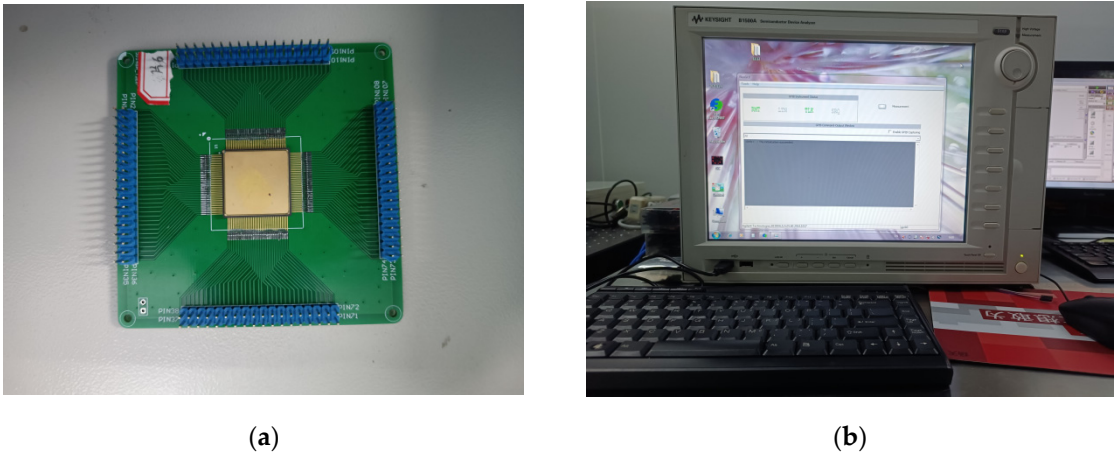


Figure 2. The test device diagram (a) Device to be tested (b) B1500 semiconductor tester.

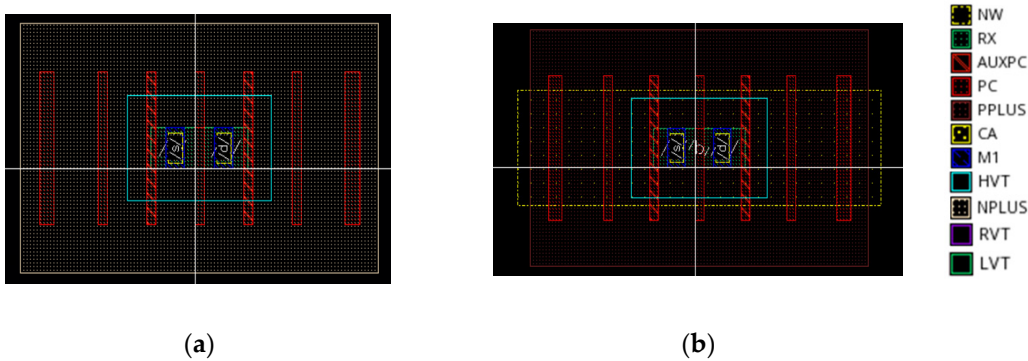


Figure 3. Layout file of (a) NMOS and (b) PMOS.

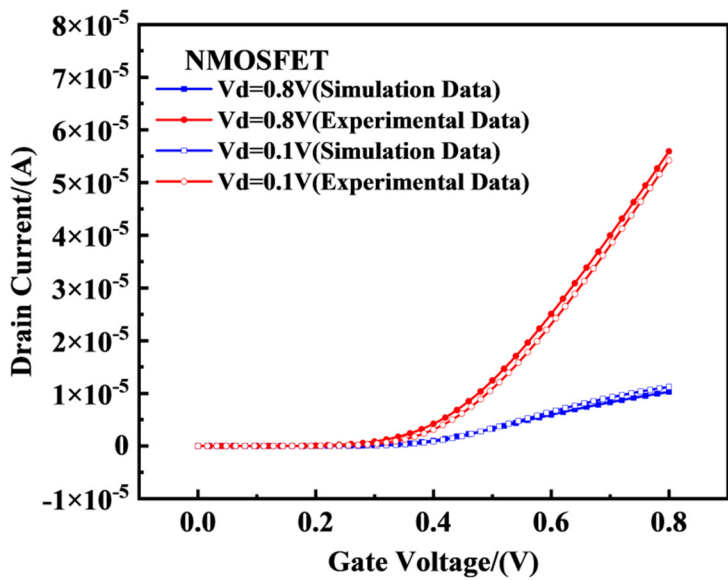


Figure 4. Comparison of experimental transfer characteristic curves of NMOS devices. When simulating irradiation, the bias was set as $V_{ds} = 0.1V/0.8V$.

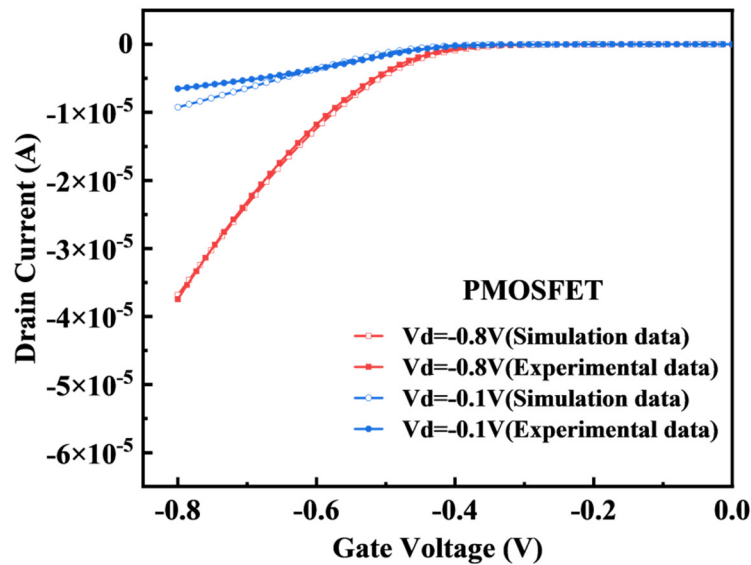


Figure 5. Comparison of experimental transfer characteristic curves of PMOS devices. When simulating irradiation, the bias was set as $V_{ds} = -0.1\text{ V} / -0.8\text{ V}$.

Table 1. 22nm FDSOI device model parameters.

Parameter	NMOSFET	PMOSFET
Gate length (nm)	22	22
Width of device (nm)	160	220
Length of drain (nm)	40	40
Width of drain (nm)	10	10
Thickness of BOX layer (nm)	35	35
Thickness of well (nm)	25	25
Thickness of substrate layer (nm)	146	146
Thickness of gate oxide layer (nm)	2	2
Drain Doping/Ldd Doping(cm-3)	7e19/7e18	7e19/7e18
Substrate Doping (cm-3)	1e15	1e15
Well Doping (cm-3)	2e18	2e18
Workfunction (eV)	4.50	4.68

3. The Influence of TID Effect on FDSOI MOS Devices

Irradiation has changed the electrical properties of electronic devices, which has greatly changed the drain current and charge collection efficiency. From the point of view after irradiation, the effect of total ionizing dose (TID) can be evaluated by calculating the generated fixed charge and interface trap [9].

TCAD software is a finite element software used to simulate the semiconductor continuity equation model. It can numerically solve the nonlinear Poisson equation combined with the carrier continuity equation. Therefore, some special models in TCAD tools are usually used to simulate these effects.The physical model of TID effect simulation includes some basic simulation models, such as mobility model, generation recombination model, thermodynamic dynamic model, etc. Among them, the mobility model is used to describe the mechanism by which doping concentration, electric field, and other factors affect particle mobility, making its characteristics closer to actual devices. The generation recombination model is used to describe the basic recombination mechanism of particles and the related recombination behavior of collision ionization, mainly describing the carrier exchange

process of valence and conduction bands. The thermodynamic dynamic model extends the drift diffusion method to explain the electrothermal effect, and solves the lattice temperature equation other than the Poisson's equation and the carrier continuity equation. The radiation model is used to simulate the effects of different Radiation exposure, different radiation times and irradiation on transistors. Due to radiation changing the electrical performance of electronic devices, it greatly alters the drain current and charge collection efficiency. From the perspective of irradiation, the impact of total ionizing dose (TID) can be evaluated by calculating the generated fixed charges and interface traps.

Synopsys Sentarus TCAD includes some radiation models, but they are not fully applicable. However, due to the fact that TCAD simulation software cannot directly solve the equations for insulator materials (such as oxides). Therefore, it is necessary to perform material transformation on this model, and a "OxideAs Semiconductor" module has been specially designed in TCAD, which can assume that the insulator has the electron hole transmission characteristics of a semiconductor. By modifying the material of the buried oxygen layer, silicon dioxide, to the "OxideAsSemiconductor" module, an irradiation related model can be added to simulate the total dose effect of irradiation on the device. The added irradiation model is as follows.

(1) Radiation model

This model relates the volume charge to the absorbed dose. However, this software cannot directly solve the equation of insulator materials (such as oxides) [10]. Therefore, it is necessary to carry out material transformation for this model. The OxideAsSemiconductor material is specially designed in TCAD to make the insulator have the electron hole transmission characteristics of semiconductor. The total dose effect of irradiation on the device can be simulated by modifying the material silicon dioxide of the buried oxygen layer to OxideAsSemiconductor and adding the relevant model of irradiation in it.

(2) Trap model

The trap model can be used to reproduce the existence of traps on the interface. The setting of trap concentration needs to consider the absorbed dose [10].

3.1. Physical Models

The Radiation radiation model used in the study is as follows.

$$G_r = g_0 \cdot \frac{dD}{dt} \cdot Y(E) \quad (1)$$

$$Y(E) = \left(\frac{E + E_0}{E + E_1} \right)^m \quad (2)$$

where, G_r is the number of holes without initial recombination; g_0 is the number of electron hole pairs per unit volume of material after absorbing 1 rad radiation energy, and the SiO_2 material is $7.6 \times 10^{12} \text{ ehp/rad} \cdot \text{cm}^3$; D is the total irradiation dose; $\frac{dD}{dt}$ is dose rate ($\text{rad} \cdot \text{s}^{-1}$) $Y(E)$ is the hole yield, which is related to the electric field, E_0 is the constant 0.1V/cm, E_1 is the 0.55MV/cm, and the constant m is 0.7 when the irradiation source is Co-60 [10].

Due to the high electron mobility, the carriers in the oxide will be swept out within a few picoseconds after generation and collected on the corresponding electrode. Compared with the mobility of electrons, the mobility of holes is much lower. Because of the slow jump propagation of holes, the probability of holes being captured near the interface is greatly increased. Due to the tunneling mechanism, some holes are also swept into the top layer of silicon. The remaining holes in the oxide volume can be calculated by the fraction function of formula (2), which depends on many processing parameters and applied electric field. The trapped holes in the oxide layer form the fixed oxide charge component of ionization damage. In order to simulate the total fixed charge in the irradiated oxide, if the oxide is thick enough (more than 15 nm to avoid tunneling effect), the total oxide charge concentration caused by radiation can be expressed as formula[11].

$$N_{ot} = g_0 \cdot D \cdot Y(E) \quad (3)$$

Sentaurus TCAD includes this model. Refer to relevant literature and adjust the parameters, where the generation rate of electron hole pair $g_0 = 7.6 \times 10^{12} \text{ rad}^{-1} \cdot \text{cm}^{-3}$, $E_0 = 0.1 \text{ V/cm}$, $m = 0.9$.

After the electron-hole pair is generated by ionizing radiation, the electrons are swept out of the oxide layer, and the remaining holes are transported slowly inside. The shallow level intrinsic defect oxygen vacancy ($V_{0\delta}$) in the oxide layer is easy to capture the hole and form the metastable field center E_{δ}' . The center constantly captures and releases the hole, making the hole exchange between different oxygen vacancies. The oxygen vacancy defect level near the Si/SiO₂ interface is deep, and the trapped hole is easy to generate stable E_{γ} Center. The TCAD numerical simulation method usually measures and characterizes the ability of defects to capture electrons or holes by capture cross section (σ_n, σ_p), and σ_n, σ_p is defined as the target region, where electrons or holes will be captured by defects. The capture cross section is related to the concentration, energy level and spatial distribution of defects. With reference to relevant literature, the defect distribution type, energy level position, concentration and the cross section size of trapped electrons or holes in SiO₂ are set quantitatively. In the Traps model, the hole trap concentration in the layer is defined as $1 \times 10^{18} \text{ cm}^{-3}$, the capture cross sections of holes and electrons are $1 \times 10^{-14} \text{ cm}^2, 1 \times 10^{-16} \text{ cm}^2$. Neutral hole traps do not show electricity when no holes are captured, and they are positively charged after the holes are captured [12].

In the simulation, the mobility of electrons and holes generated by irradiation in is set to a constant value of $20 \text{ cm}^2/\text{V}\cdot\text{s}$ and $1 \times 10^{-5} \text{ cm}^2/\text{V}\cdot\text{s}$.

The simulation model in Sentaurus TCAD is specifically expressed as follows.

```
Physics (Region="R.Box") {
Radiation(DoseRate=@doserate@ DoseTime=(0.2,@<dosetime+0.2>@) doseTsigma=0.2)
Traps(ElectricField hNeutral Conc=1e18 EnergyMid=-0.5 FromMidBandGap
eXsection=1.0e-14 hXsection=1.0e-16 eJfactor=0 hJFactor=0)
}
```

3.2. Simulation Setup

Physical models simulating the TID effect include the mobility, generation recombination, thermodynamic, and radiation models.

In the TCAD simulation model, simulations of γ -ray irradiation with 0k, 100k, 300k, 500k, 800k rad(Si) were performed on aforementioned types of devices in the TID experiments. The transfer characteristic curves of irradiation are shown in Figure 6 and Figure 7. The results show that the threshold voltage of the NMOS device drifts in the negative direction with an increase in radiation dose, and the threshold voltage of the PMOS device also drifts in the negative direction with an increase in radiation dose. Compared with the irradiation curve of FDSOI devices with a buried oxygen layer thickness of 28nm[13], the simulated transfer characteristic curve changes and threshold voltage drift are basically consistent with the trend and range of changes in the reference literature.

The maximum transconductance method was used to extract the curve parameters. The variation in threshold voltage drift with irradiation dose under different irradiation doses was obtained, as shown in Figure 8. The results show that the threshold voltage of the NFET decreases and the absolute value of the threshold voltage of the PFET increases with increasing radiation dose. This is because the external diffusion of oxygen atoms in the oxide layer does not match the surface lattice; therefore, there are a large number of oxygen vacancies near the Si/SiO₂ interface, which act as trap centers. Since the transport speed of a hole is lesser than that of an electron, the probability of hole capture is greater, which forms a positively charged trapped hole [14], as shown in Figure 9 and Figure 10. With an increase in the irradiation dose, the number of trapped charges also increases in the BOX layer, which is directly below the channel. Taking NMOS as an example, the hole trap charges captured by the BOX layer are mainly distributed below the channel, and as the irradiation dose increases, the concentration of trap charges in the buried oxygen layer (BOX layer) becomes

higher and higher. These traps that capture holes display positive electrical properties, the formation of positive oxide layer trap charges at the Si-SiO₂ interface, These trapped charges change the potential of the interface between the top silicon and BOX and further affect the potential of the top silicon front gate through the coupling effect between the front and rear channels, causing a drift in the threshold voltage.

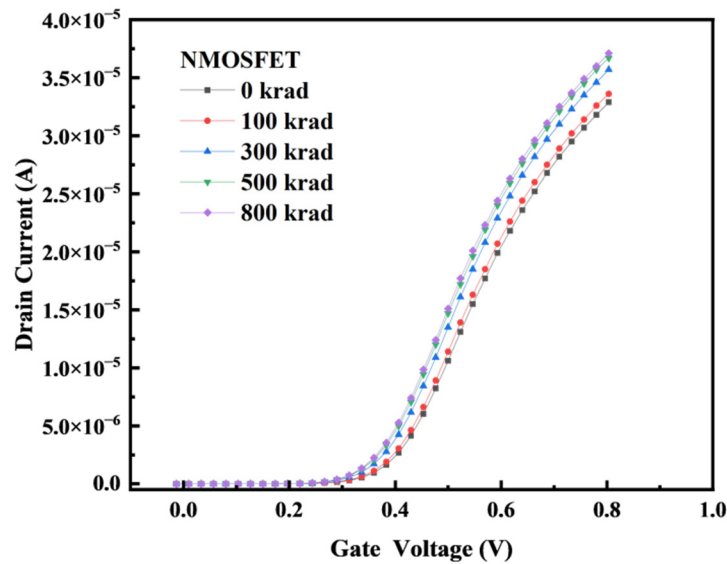


Figure 6. When simulating irradiation, the **bias** is set as $V_{ds} = 0.1V$. I-V curves are plotted before irradiation and at several TID steps (gray curves) up to 800k rad (Si).

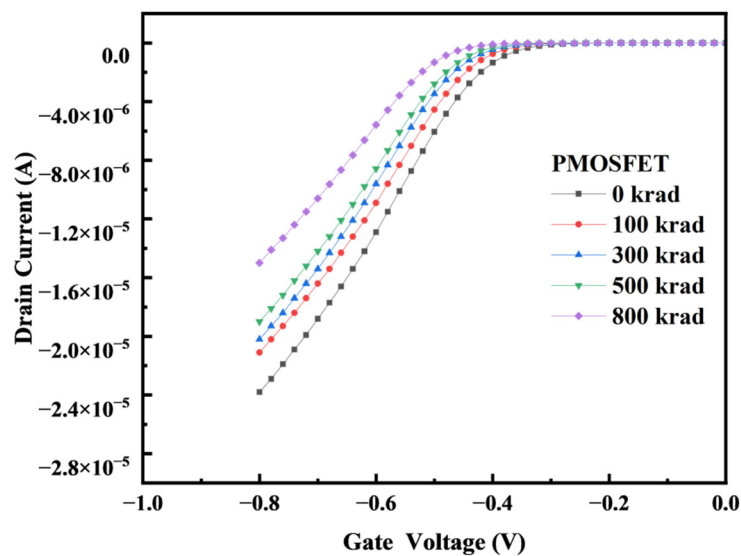


Figure 7. When simulating irradiation, the bias is set as $V_{ds} = -0.1V$. I-V curves are plotted before irradiation and at several TID steps (gray curves) up to 800k rad (Si).

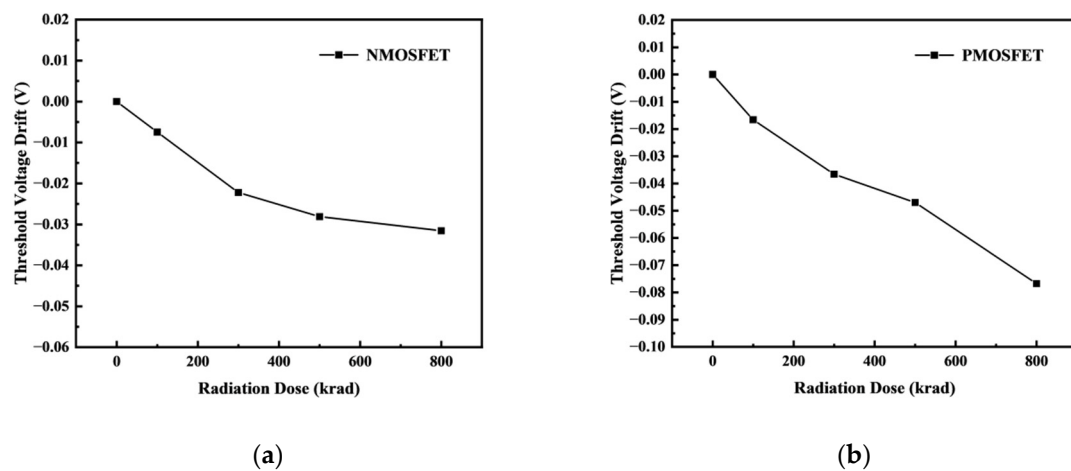


Figure 8. Variation in threshold voltage drift of (a) NMOS and (b) PMOS under different irradiation doses.

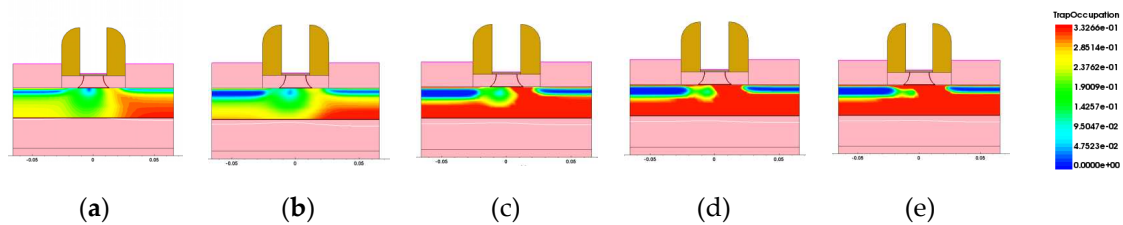


Figure 9. The distribution of trapped charge in the BOX layer of NMOS devices after (a) 100 krad (b) 300 krad (c) 500 krad (d) 700 krad (e) 1 Mrad (Si) dose irradiation.

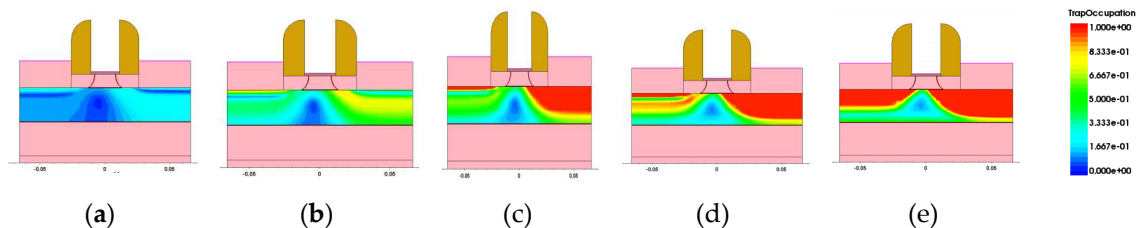


Figure 10. The distribution of the trapped charge in BOX layer of PMOS devices after (a) 100 krad (b) 300 krad (c) 500 krad (d) 700 krad (e) 1 Mrad (Si) dose irradiation.

3.3. Experience Test

In order to verify the accuracy of the simulation model, the irradiation experiment relied on Co-60 γ -ray source from the Xinjiang Institute of Physical Chemistry to irradiate NMOSFET devices with a gate length of 22nm and a gate width of 160nm, as well as PMOSFET devices with a gate length of 22nm and a gate width of 220nm. Place the sample in a closed environment with an irradiation source, set the irradiation dose rate to 150 rad (Si)/s, and measure the electrical characteristics of MOSFETs at a total irradiation dose of 300 krad (Si), 500 krad (Si), and 800 krad (Si), respectively. This is used to compare and study the degradation degree of different dose devices and the accuracy of simulation models.

Due to the main impact of irradiation on the device, the electrical parameter is the threshold voltage, so it is necessary to test the transfer characteristic curve of MOS devices in the irradiation experiment, and the transfer characteristic curve testing conditions are as follows.

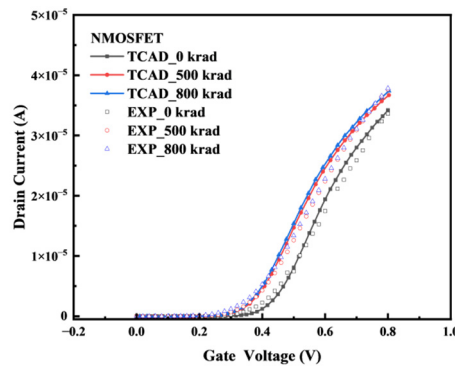
(1) NMOSFET

Maintain the drain voltage at 0.1V, scan the gate voltage (V_g) from 0 to 1V, ground the source, and test the change of drain current (I_d) with the gate voltage .

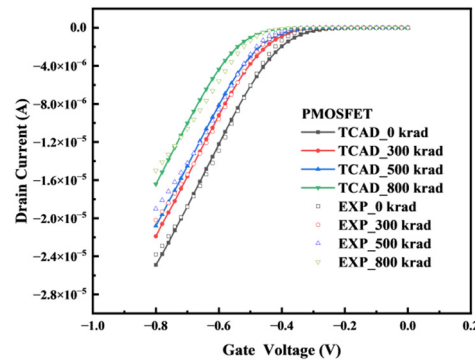
(2) PMOSFET

Maintain the drain voltage (V_d) at -0.1V, scan the gate voltage V_g from -1 to 0V, ground the source, and test the variation of the drain current (I_d) with the gate voltage.

Due to the degradation of the effect of irradiation dose on the device over time, the testing process of the sample MOSFET is carried out within one hour of the completion of the irradiation experiment when the irradiation dose reaches the pre-set dose point, and the same B1500 semiconductor tester is used for measurement. The TCAD simulation results and experimental testing results of the transfer characteristics changes of NFET devices and PFET devices under different irradiation doses are shown in Figure 11. To analyze the accuracy of the established device model and the total dose model, and compare the changes in electrical parameters under different irradiation doses, Further extract the variation of various electrical parameters of the device with irradiation dose using Matlab software, as shown in Figure 12 shows the validation of the threshold voltage parameters of the device. The maximum error of the NFET device simulation model compared to the actual test device's threshold voltage is 1.98%, and the PFET device simulation model compared to the actual test device's threshold voltage error is 9.92%. In summary, the electrical characteristic parameters of the built device simulation model meet the accuracy requirements.

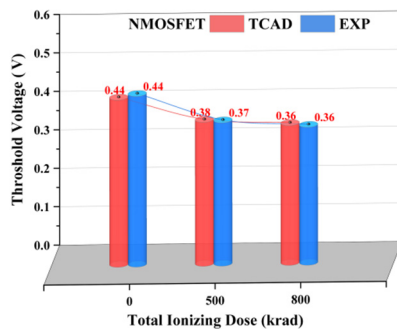


(a)

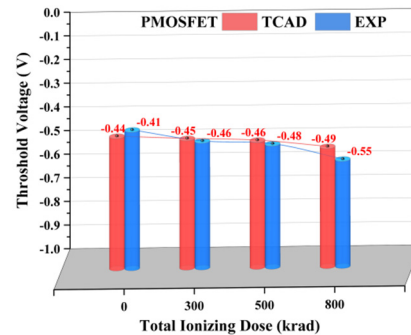


(b)

Figure 11. Transfer characteristic of Experiments and Simulations (a) NMOS and (b) PMOS.



(a)



(b)

Figure 12. Variation in threshold voltage of Experiments and Simulations (a) NMOS and (b) PMOS.

4. Influence of TID Effect on Inverter Circuits

The analysis in the third section shows that the threshold voltage of the NMOS device continuously drifts in the negative direction with the increase in radiation dose, and its voltage clamping ability becomes worse, which may cause false touch or even loss of switching characteristics in the circuit. The threshold voltage of the PMOS device also drifts in the negative direction with an increase in the radiation dose; that is, it requires a larger reverse voltage to turn on. These changes can lead to circuit dysfunction and failure.

Inverter circuits are widely used as the most basic CMOS circuit structures. Therefore, studying the total dose effect of CMOS circuits based on inverters is important [15]. Currently, the latest modeling method for research on circuit level total dose effects is to calibrate BSIM3 model parameters based on HSPICE software to replace irradiated device models, and based on this, simulate the impact of total dose effects on circuits at different irradiation doses [16]. Although the simulation speed of this method is fast, the accuracy of the BSIM3 simulation method needs to be improved because it is only aimed at conventional silicon based MOS devices and cannot be accurately used for the simulation of nanoscale FDSOI devices. In summary, this study is based on physical device modeling and uses a hybrid simulation method to simulate and analyze the TID effect of inverter circuits. It can comprehensively consider the impact of total amount effect on electrical parameters such as threshold voltage, mutual coupling capacitance, parasitic resistance, etc. of devices in the circuit, so as to conduct more accurate results analysis of logic threshold, noise tolerance, signal delay, and other parameters of inverter under irradiation conditions.

The inverter structure is shown in Figure 13. In the device structure, NMOS and PMOS are calibrated devices. Based on Sentaurus software, a hybrid mode simulation method was used to add an irradiation model to the circuit to simulate the total dose effect on the inverter. Figure 14 and Figure 15 show the voltage-transfer curve (VTC) and voltage gain curve of the inverter, respectively. The results show that the curve of VTC shifted to the left with an increase in the irradiation dose. To quantitatively analyze the influence of the total dose on the inverter circuit, we processed the data in the curve. Figure 16 shows the logic threshold (VM) for different radiation doses, where VM is the voltage value corresponding to the input and output points in the transmission characteristic curve. Noise tolerance of the logic high level (NMH) and low level (NML) refer to the tolerance range for the correct reception of logic high- and low-level signals, respectively. Figure 17 shows variation in the noise margins (NMH and NML) at different radiation doses. The results show that with an increase in the radiation dose, the logic threshold voltage of the inverter decreases, the high-level noise tolerance range increases, and the low-level noise tolerance range decreases. This is due to the traps generated by irradiation in the BOX layer, which capture holes at the Si-SiO₂ interface and form positive trap charges. Thus, it affects the potential of the top silicon and causes the threshold voltage of the NMOS device to decrease with an increase in irradiation dose. Similarly, the absolute value of the threshold voltage of the PMOS device increases with increase in irradiation dose. This is also the reason for the negative drift of the voltage transmission curve of the inverter and reduction in the logic threshold. The results show that the logic threshold shift of the inverter was approximately 0.052 V when the irradiation dose was 400 krad (Si).

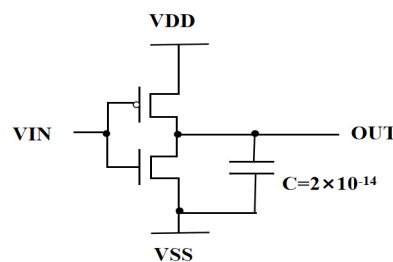


Figure 13. The inverter structure.

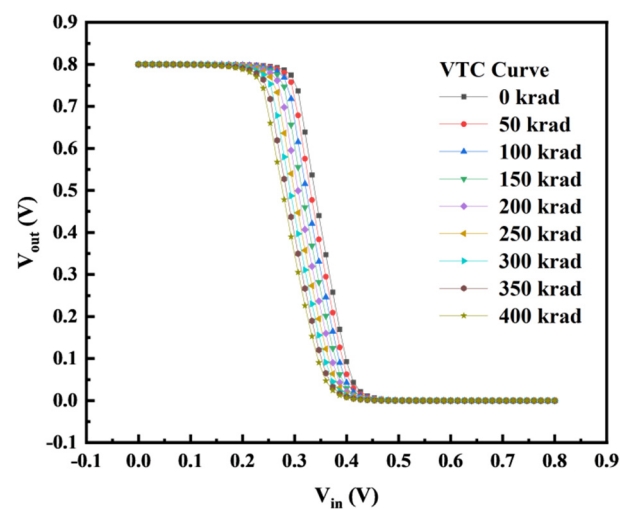


Figure 14. Voltage transfer curve (VTC) of inverter for different total ionizing doses.

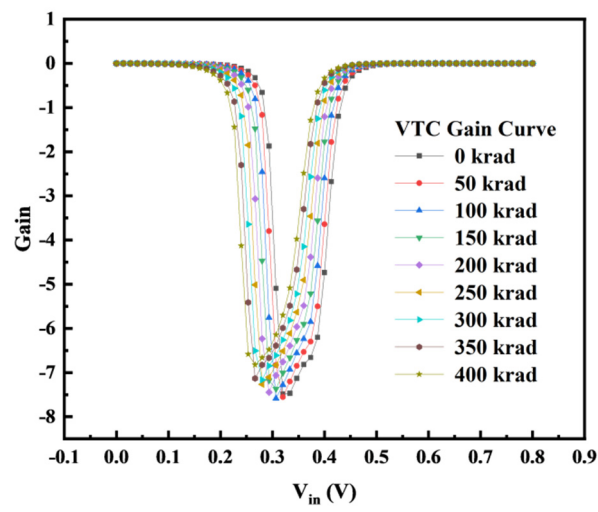


Figure 15. The voltage gain curve of the inverter for different total ionizing dose.

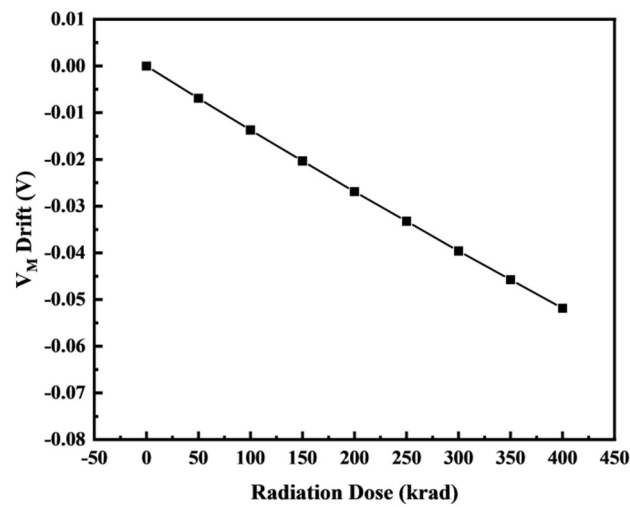


Figure 16. The logic threshold (V_M) of the inverter for different total ionizing dose.

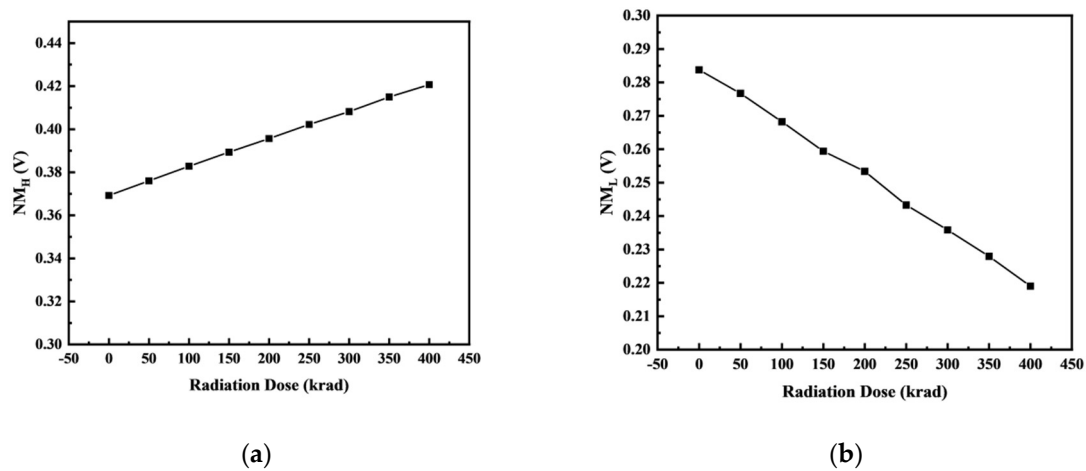


Figure 17. Noise tolerance of (a) logic high level (N_{MH}) and (b) low level (N_{ML}) of the inverter for different total ionizing doses.

5. Conclusions

Because of the pursuit of the development of Moore's Law, the traditional bulk silicon process found meeting the requirements of small devices difficult. The FDSOI technology has achieved full dielectric isolation and has greater advantages in terms of speed, integration, and radiation resistance[17]. Therefore, FDSOI technology, which is the basic device process of integrated circuits, has attracted increasing attention in many fields, particularly in aviation and other fields. Its radiation resistance performance has also received increasing attention. Therefore, the study of inverter circuits based on FDSOI CMOS devices is significant for the subsequent application of FDSOI technology in integrated circuits.

The total ionizing dose effect was found to change the threshold voltage of the MOS devices. With an increase in the radiation dose, the threshold voltage of the NMOS decreases, and the absolute threshold voltage of the PMOS devices increases. In particular, when the irradiation dose was 300 krad, the threshold voltage drift rate of the NMOS device reached 11.72%, which exceeded 10%, and the device was judged to have failed. When the irradiation dose was 700 krad, the threshold voltage

drift rate of the PMOS device reached 10.87%, which exceeded 10%, and the device was judged to have failed.

In addition, a simulation of the total ionizing dose effect of the inverter was performed. With an increase in the radiation dose, the voltage transmission curve of the inverter drifted negatively, the logic threshold value decreased, the high-level noise tolerance range increased, and the low-level noise tolerance range decreased. When the irradiation dose was 400 krad (Si), the logic threshold shift of the inverter was approximately 0.052V. Compared to the inverter input voltage of 0.8V, it generates a drift of 6.5%. The low level range of digital circuits is 10% of the high level signal, so the impact of irradiation dose on the inverter cannot be ignored.

Author Contributions: Conceptualization, T.G.; methodology, T.G.; software, T.G. and C.Y.Y.; validation, T.G., C.Y.Y. and Y.C.; formal analysis, T.G.; investigation, T.G. and C.Y.; resources, T.G.; data curation, T.G.; writing—original draft preparation, T.G.; writing—review and editing, T.G.; visualization, T.G.; supervision, H.L.; project administration, R.C.; funding acquisition, H.L. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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