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Article

# Investigation of Single Event Upset in Graphene Nano-Ribbon FET SRAM Cell

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**Abstract:** In recent years, graphene has received so much attention because of its superlative properties and its potential to revolutionize electronics especially in VLSI. This study analyzes the effect of single event upset (SEU) in SRAM cell which employs metal-oxide semiconductor type graphene nano-ribbon field effect transistor (MOS-GNRFET) and compares the results respectively with another SRAM cell designed in PTM 10nm FinFET node. Our simulation show there is a change in data stored in the SRAM after heavy ion strike. However, it recovers from radiation effects after 0.46 ns for GNRFET and 0.51 ns for FinFET. Since the degradation observed in  $Q$  and  $Q_b$  of GNRFET SRAM are 2.7X and 2.16X as compared to PTM nano-MOSFET, we can conclude that GNRFET is less robust to single effect upset. In addition, the stability of SRAM can be improved by increasing the supply voltage  $V_{DD}$ .

**Keywords:** graphene nano-ribbon FET; single event upset; SRAM; stability; FinFET

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## 1. Introduction

The reliability issue for electronic systems is gaining more attention because of advancement and scaling down of technology nodes. Continuous device shrinking, increased integration level, extremely low operating voltage, structural changes, high speeds etc. have caused semiconductor or other related devices 2D devices to be more sensitive to radiation, consequently leading to electronic system failures and mal function. Hence, the need to investigate radiation and its impacts on the reliability of VLSI design. SRAM is an essential building block of a memory unit, which is usually designed for high speed and low power applications. It is characterized with high integration capability, fast storage speed and compatible with CMOS. In a radiation environment such as space, radiation particle (e.g., alpha particles, protons, neutrons, or other heavy ions) causes a decrease in critical charge and capacitance of SRAM, thus more susceptible to Single Event Upset (SEU) [1]. An electron-hole pair is generated along the path of a charged particle in a semiconductor device, which results in collected charge ( $Q_{coll}$ ). The  $Q_{coll}$  can change the state of register, latch, memory cell or flip flops, if it exceeds the threshold value, critical charge ( $Q_{crit}$ ). Several research have been conducted to investigate the soft error caused by radiation effect. Li *et al.* and Mahyuddin *et al.* introduced a strike at the circuit node with a transient current source to emulate SEU [2]. Similarly, the SEU effect in III-V Hetero-junction TFET, III-V FinFET and Si FinFET are investigated using circuit simulation [3]. The soft error

performance before and after radiation in DG TFETs 6T SRAM cell are also studied. Xiang et al. showed the effect of single event transient (SET) in a phase locked loop and proposed SET-hardened structure to improve the irradiation resistance of PLL [4, 5]. Note that it has been shown theoretically and experimentally that graphene nano-ribbon FET (GNRFET) can potentially replace planar CMOS and FinFET [6]. GNR has a finite band gap with good semiconductor properties, GNR transistor exhibits low sub-threshold swing and high on/off ratio, which makes it suitable for logic and low power applications. A brief review and analyses of GNRFET will be discussed later in this work.

In this paper, we present device level characteristics of GNRFET, study and compare SRAM circuits made of MOS-GNRFETs and FinFETs and investigate their soft error performance.

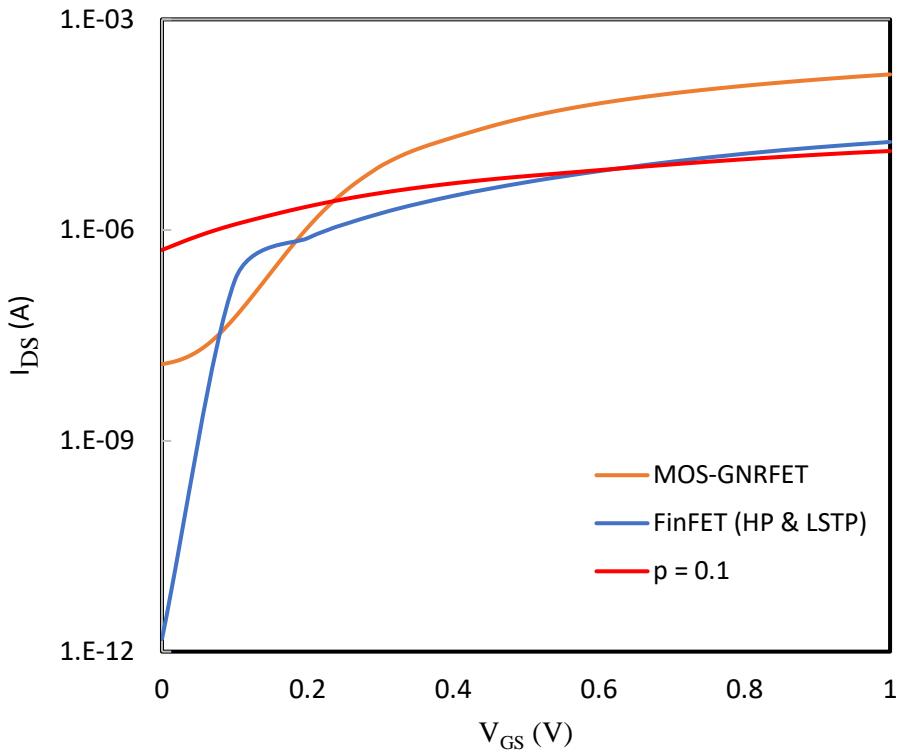
## 2. GNRFET Device Simulation and Characterization

Graphene nanoribbon (GNR) FET are made from GNRs which are 1D nano-sized graphite layers or strips of graphene with superlative electronic properties. Graphene, in its pristine condition, has no bandgap and causes poor on/off current ratio and subthreshold, thus it is not suitable for digital applications. However, its width can be patterned and modified to a few nanometers 1D GNR, thereby creating a finite gap which is required for a semiconductor. The width of GNR is inversely proportional to induced bandgap, GNRFET switch-ability can be improved by increasing the width of the nanoribbon. Certain variability and defects can emerge from oxide thickness, GNR width, line of edge roughness (LER) that affect the performance of GNRFET. The different planar structure and models of MOS-GNRFET and SB-GNRFET are already presented in ref.[7], we have chosen MOS-GNRFET in this work because of its high on/off current ratio. In addition, it is more robust to process variation, operates based on thermionic emission and will compare fairly with FinFET technology, monotonic I-V curves and no voltage shifting. Table 1 summarizes the HSPICE model of n-/p-type GNRFET.

Table1: Model and Device Parameter Definitions

Device Parameter	Description	Value Range
Lch	Channel length	~10 – 100 nm
Wch	Channel width	0.873 – 6.36 nm
nRib	Number of GNRs in the device	6 – 50
Tox	Oxide thickness	0.5 – 2.5 nm
dop	Doping fraction	0.001 – 0.0015
p	Edge roughness	0 – 20%
sp	Spacing between ribbons	1nm default

For the transistor level characteristics, MOS-GNRFET works well with a nominal  $V_{DD} = 0.5$  V. Figure 1 shows the curve of MOS-GNRFET and 10nm HP and LSTP Si-CMOS n-type transistors from PTM. For fairer comparison, we scaled the GNRFET model to match the PTM libraries. The minimum recommended nominal  $V_{DD} = 0.75$  V is chosen for PTM devices.



**Figure 1.**  $I_{DS}$  vs.  $V_{GS}$  for an ideal and non-ideal MOS-GNRFET, high performance and low stand-by power Si-CMOS.

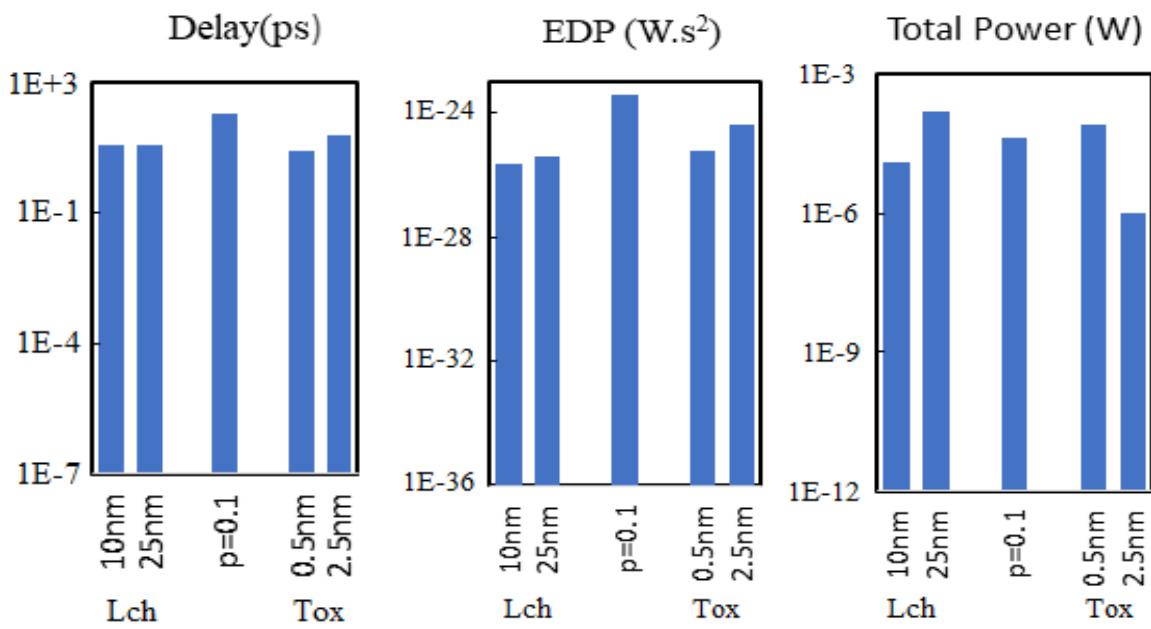
From the plot, the ideal MOS-GNRFET has the highest  $I_{on}$  while PTM nano-MOSFET Si-CMOS models have better  $I_{off}$ , and their current ratios are given in Table 2. As the edge roughness probability is increased to 10%, the I-V curve becomes worse in both  $I_{on}$  and  $I_{off}$ , which indicates a degradation in the performance of the device.

Table 2: Transistor Performance Comparison

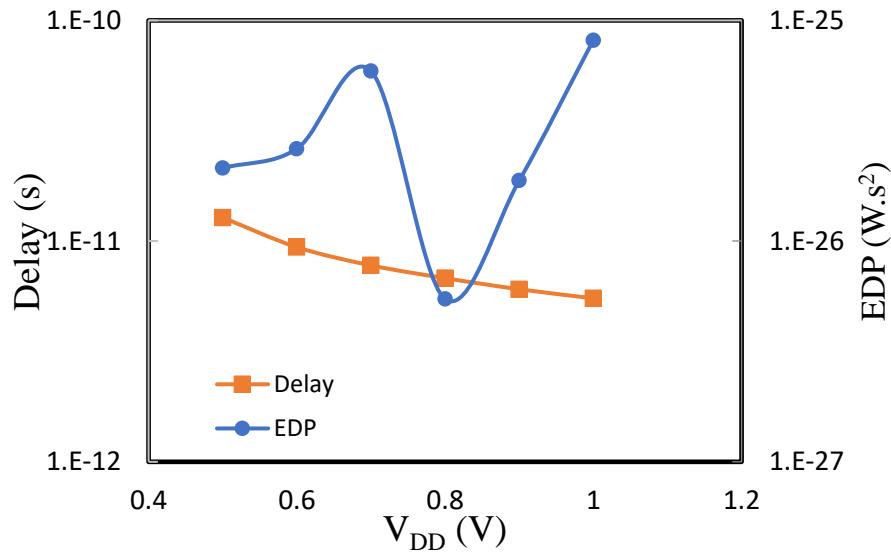
Device	pr	$I_{on}/I_{off}$	$V_{DD}$ (V)
GNRFET	0	1.33E+04	0.5
	0.1	2.59E+01	0.5
CMOS FinFET	-	1.1E+07	0.75

Here, we analyze the properties of an inverter designed with MOS-GNRFETs under  $V_{DD} = 0.5$  V. Graphene nanoribbon FET is sensitive to the major sources of variation e.g., process, voltage, and temperature (PVT) that affect its performance. It is, however, important to check our design for different corners. During fabrication of transistor device, the process variation such as oxide thickness, doping concentration can vary slightly from the target specification, thereby translates to faster or slower devices. Similarly, variation in supply voltage has effect on the current drivability, and temperature can also alter the resistance of the device. Figure 2 shows the impact of channel length, oxide thickness and line of edge roughness. Although delay increases slightly with  $L_{ch}$ ,  $Tox$  has more significant impact

on the speed of MOS-GNRFET. Similarly, a higher thick oxide reduces the gate leakage, and the total power is equally reduced.



**Figure 2.** Delay, EDP, and total power vs. Lch, Tox and p. Please note the device parameters of MOS-GNRFET are set to default values [7]. For Tox variation, Lch is set to 10nm while Tox is set to 0.5 nm for Lch variation.

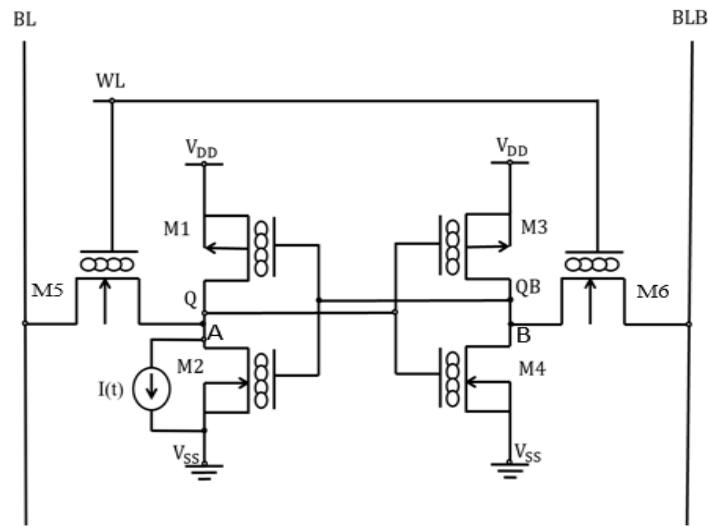


**Figure 3.** Delay and EDP vs. supply voltage.

The delay in Fig. 3 decreases with  $V_{DD}$  because the drive current increases which largely affects the rate at which the CMOS capacitive load are charged or discharged. Unlike delay, the EDP is non-monotonic which is in consistent with the model behavior [7]. Even though the current conduction in MOS-GNRFET model is both thermionic and BTBT (band-to-band-tunneling), its transistor properties are weakly dependent on temperature just as similar to tunnel field effect transistor.

### 3. Single Event Upset in SRAM Cell

In this work, we employed the conventional 6T SRAM cell topology in Fig. 4 which comprises of the storage or memory transistors (M1-M4) and access transistors ATs (M5-M6) constructed with n- and p-type MOS-GNRFET. Transistors M5 and M6 are sized optimally to improve read and write ability and access time.



**Figure 4.** 6T SRAM with single event upset.

$$CR = \frac{(W/L)_1}{(W/L)_5} = \frac{(W/L)_2}{(W/L)_6} = \frac{w_1}{w_5} = \frac{w_2}{w_6} \quad (1)$$

$$PR = \frac{(W/L)_1}{(W/L)_5} = \frac{(W/L)_2}{(W/L)_6} = \frac{w_1}{w_5} = \frac{w_2}{w_6} \quad (2)$$

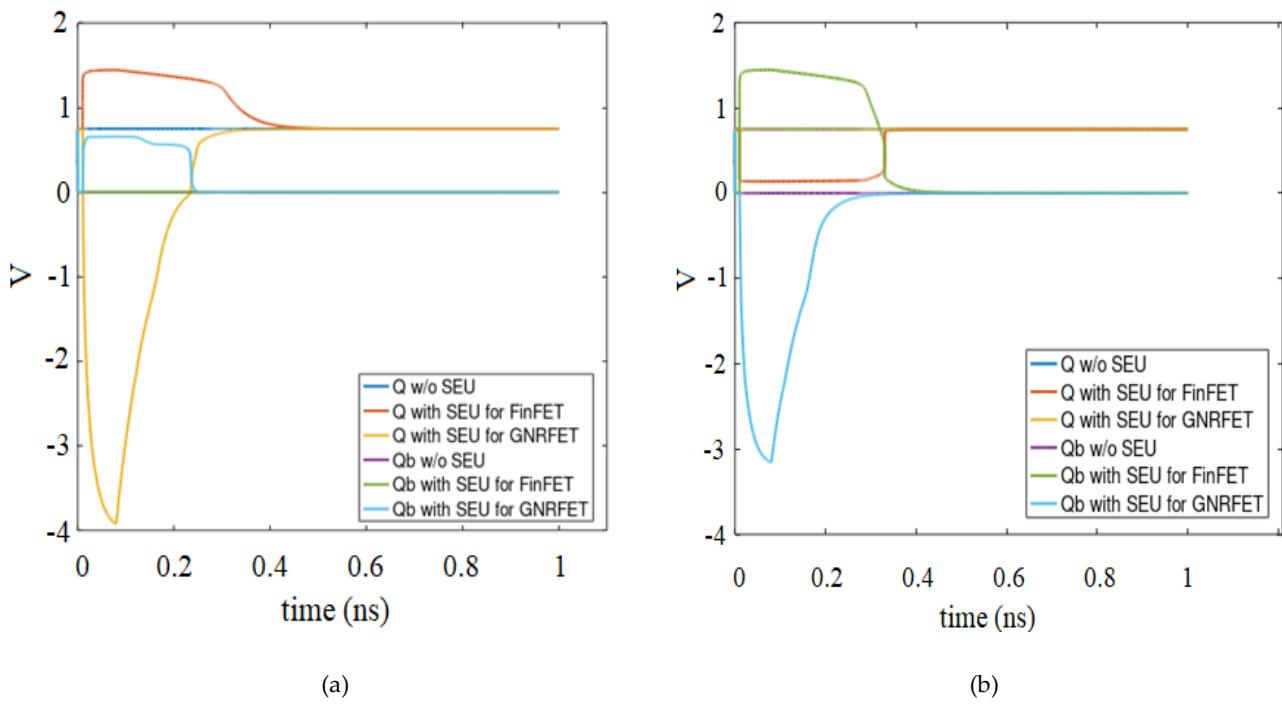
We adopted the strong drive transistors, medium access, and weak pull-up transistors whereby CR (drive to access transistor ratio) is set equal to PR (pull-up to access transistor ratio). WL denotes the control input signal applied to the gates of ATs while BL and BLB function as input or output lines depending on the mode of SRAM. Equation 3 represents the single event upset modelled with double exponential transient time current injected at sensitive nodes A and B, and the total charge collected is given as:

$$I(t) = I_0 \left[ \exp\left(\frac{-t}{\tau_\alpha}\right) - \exp\left(\frac{-t}{\tau_\beta}\right) \right] \quad (3)$$

$$Q_{\text{Coll.}} = \int_0^{T_{\text{Coll.}}} i_{\text{inj}}(t) dt \quad (4)$$

where the magnitude of pulse current,  $I_0 = 5\text{mA}$ ,  $\tau_\alpha = 20\text{ps}$  and  $\tau_\beta = 40\text{ps}$  are time constants,  $Q_{\text{Coll.}}$  and  $T_{\text{Coll.}}$  are collected charge and collection time, respectively.

In Fig. 5(a), the output Q of an ideal GNRFET recovers faster than FinFET after radiation strike and both align with Q without SEU after 0.46 ns and 0.51 ns, respectively. Unlike Qb degradation in GNRFET, FinFET Qb is unaffected and the degradation in Q for GNRFET is also  $\sim 2.7X$  which infers it is more sensitive to single event transient at node A.



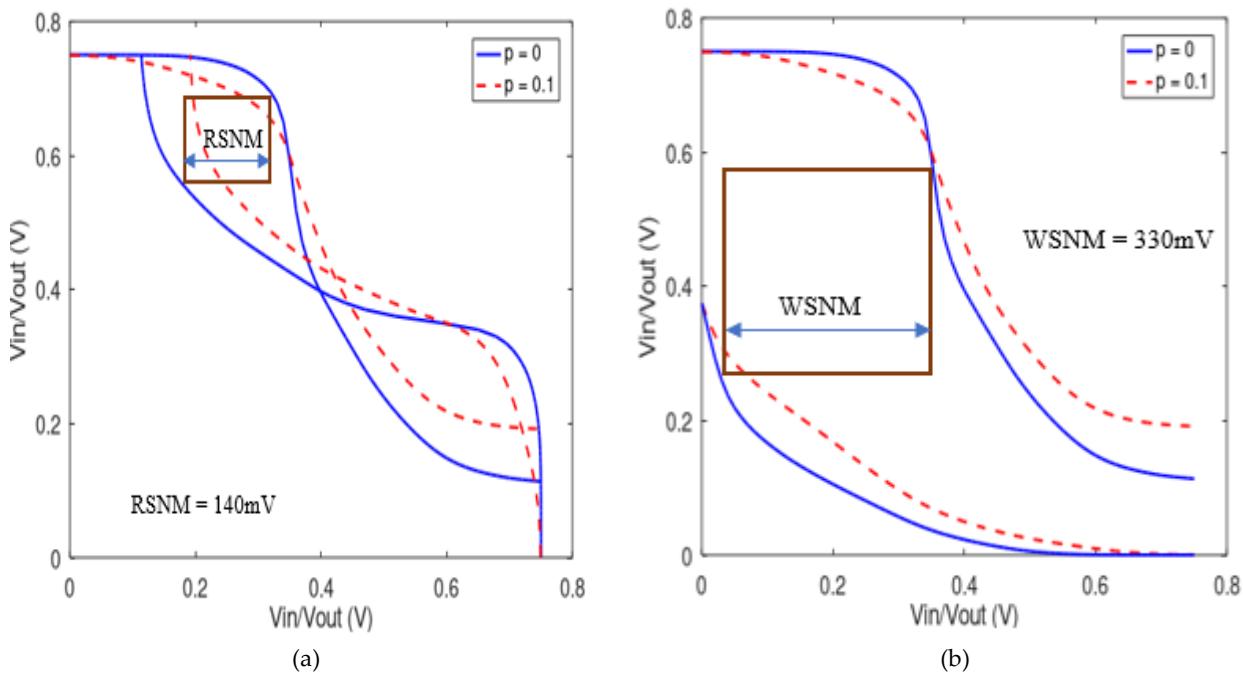
**Figure 5.** Timing diagram for SRAM with single event upset (a) Node A; (b) Node B.

On the contrary, both  $Q$  and  $Q_b$  of FinFET SRAM in Fig. 6 are largely affected by radiation effect at node B. The two outputs flip immediately the  $Q_{\text{coll.}}$  due to a charge particle strike exceeds  $Q_{\text{Crit.}}$ , but it is not enough to make the node to lose its recovering potential. There is, however, 2.16X degradation observed in  $Q_b$  of GNRFET SRAM. It is expected since technologies that operate with low voltage tend to be less resistant to radiation and have high soft error rate.

#### 4. Stability of Graphene Nano-Ribbon FET SRAM Cell

Because of aggressive  $V_{\text{DD}}$  scaling and increased intra-die variability, the two critical metrics read and write stability of SRAM cell are major concerns. The stability also known as static noise margin (SNM) is the minimum voltage noise that can change the state of SRAM at storage node. Although there are other methods of SNM measurements, butterfly plot is considered as one of the best ways to measure the stability. It is a voltage transfer curves of the storage cell or two inverter circuitry superimposed on each other. We employed the test benches in ref. [8] for measurements and the results are presented in Fig. 6. The read and write SNM are higher than when 10% edge roughness is introduced i.e., the robustness of SRAM is reduced with LER.

We equally investigated how SNM varies with transistor channel length or technology node and supply voltage  $V_{\text{DD}}$ . An increase of  $L_{\text{ch}}$  from 10 nm to 25 nm results in 22.1% and 19.7% increase in read and write stability, respectively. Similarly, the change in  $V_{\text{DD}}$  from 0.5 V to 0.75 V improves the read SNM by 45 mV and write SNM by 120 mV.



**Figure 7.** Static noise margin for SRAM (a) Read and, (b) Write.

## 5. Conclusion

In this work, transistor level properties of MOS-GNRFET and PTM nano-MOSFET models are analyzed, the impact of level of edge roughness on the performance of GNRFET is also examined. Delay, power and EDP are evaluated for different values of  $L_{ch}$ ,  $Tox$  and probability of edge roughness  $p_r$ . Subsequently, the response of the single effect upset on both 6T MOS-GNRFET and FinFET SRAMs is investigated. By using circuit simulation, a transient current is injected at the drains of M2 and M4, successively, and the outputs of SRAM flip due to primary and secondary interactions caused by charged particles. However, both Q and  $Q_b$  recover from the strike and the recovery time for GNRFET was estimated and compared with FinFET. More so, it is shown that the SNM of inverter can be improved by increasing the transistor channel length and/or  $V_{DD}$ . The static noise margin of SRAM during the read operation is lower than the write SNM which concludes that SRAM is more vulnerable to flip state or data at the read mode.

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**Conflicts of Interest:** The author declares no conflict of interest.

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