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Article

Layout Dependence Stress Investigation in through Glass via Interposer Architecture Using Submodeling Simulation Technique and Factorial Design Approach

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Abstract: Multi-chiplet technique is expected to be a promising solution to achieve high-density system integration with low power consumption and high usage ratio. This technique can be integrated with glass interposer to accomplish a competitive low fabrication cost compared with the silicon-based interposer architecture. In this study, process-oriented stress simulation is performed by the element activation and de activation technique in finite element analysis architecture. Submodeling technique is also utilized to mainly conquer the scale mismatch and difficulty in mesh gridding design. It is used as well to analyze the thermomechanical responses of glass interposer with chiplet arrangement and capped epoxy molding compound (EMC) during curing. A three-factor, three-level full factorial design is applied using the analysis of variance method to explore the significance of various structural design parameters on stress generation. Analytic results reveal that the maximum first principal stresses of 130.75 and 17.18 MPa are introduced on the sidewall of Cu-filled via and the bottom of glass interposer, respectively. Moreover, the EMC thickness and through glass via pitch are the dominant factors in the adopted vehicle. They significantly influence the stress magnitude during heating and cooling.

Keywords: multi-chiplet; TGV; finite element analysis; submodeling technique; analysis of variance

1. Introduction

The concept of three-dimensional integration of advanced electronic packaging has been widely developed and adopted in the semiconductor industries, and corresponding solutions on interconnect system are becoming a key technique. From the viewpoint of interconnect system, vertical stacked structure is considered the promising solution to achieve integration density and multiple functionality. Accordingly, the interposer architecture is demonstrated with silicon (Si) and glass material system for the performance requirement of ultrafine pitch features. Glass-based interposer has been regarded as a superior alternative of Si-based interposer architecture because of its thermal and electrical properties and low cost [1,2]. Glass interposer is targeted to reduce the cost on high-density integration and compatibility to the large pan size (450–700 mm) procedure [1]. However, the low yield of glass interposer with through glass via (TGV) is still unconquered, especially the cracking behavior and electrical degradation under thermal cycling loading [2]. Adjustable coefficient of thermal expansion (CTE) is an effective solution to manage the thermomechanical responses of glass interposer structure, and a combination of thin sputtered layer with electroless plating metal layer is demonstrated as a viable method to form TGV with high aspect ratios [3]. Among all the possible material systems of interposer, the overall characteristics of glass are better than those of other materials to accomplish more frequency bands, smaller form factors,

and lower power consumption [4]. A handling procedure of glass wafer on Si handle is demonstrated with polymer-free temporary bonding process [5], and the present handle approach is validated at 400 °C without outgassing and significantly improves the reliability during handle. Helium hermeticity reliability of copper (Cu)-filled TGV wafer is tested under different harsh environmental conditions, including thermal shock, high-temperature storage, and highly accelerated temperature and humidity stress test [6]. Thermomechanical reliability issues of glass interposer are investigated, and several glass interposers with different material characteristics are adopted to minimize the thermomechanical responses of temperature-related process [7,8]. Laser-induced deep etching technology is used to achieve the high-aspect ratio features close to 1:100 and prevent the significant internal and superficial defect [9]. Finite element analysis (FEA) simulation is utilized to estimate the stress and warpage effect on interposer generated from annealing and single- and double-side processing [10]. Failure mechanism and optimization rule of TGV interposer architecture are systematically investigated [11–19]. Tensile radial and circumferential stresses are attributed to the origin of the circumferential cracks and the formation of radial cracks, respectively [11,13,14]. Different annealing procedures are designed to study their influence on Cu protrusion mechanism [12,15], and Cu protrusion is observed to saturate after a dwell time of 4 h with an annealing temperature of 400 °C. Irreversible Cu protrusion of Cu-filled TGV is generated after thermal cycling loading and is attributed to the plastic deformation and creep mechanism of Cu [16]. Different layout designs, such as fully filled via and conformal via, are demonstrated and investigated in terms of their thermomechanical reliability [17]. Interfacial delamination between glass interposer and filled Cu is explored, and the corresponding energy release rate is proportional to the via diameter and the thermal mismatch strain, which is highly dependent on the layout design parameters [18]. A metallization process filled with Ag-paste composite solution is presented, and its effectiveness is compared with that of general Cu electroplating process; the analytical results reveal that the aforementioned metallization process will introduce different cracking behaviors [19]. The analytical model and FEA simulation approach are widely adopted to reduce the consuming experimental work due to the cost of semiconductor fabrication process [20–22]. An analytical model is derived to estimate the thermal stress and warpage in terms of different geometrical parameters and material selections [20,21]. Heating temperature, dwell time, gap width, and surface tension are interpolated in the derived analytical model, and they influence the reflow speed [22]. Glass reflow mechanism and corresponding thermomechanical stress generated in glass–Si composite interposer are explored [23]. Specific shrinkage phenomenon in epoxy molding compound (EMC) and substrate material during assembly reflow process is demonstrated and validated by warpage profile comparison [24]. Selection of EMC material significantly influences the packaging warpage and solder joint fatigue life [25,26]. From the viewpoint of electron packaging application, the design concept of chiplet arrangement is proposed to improve the yield with lower product cost [27,28]. A dual-chiplet interposer-based system-in-package architecture is demonstrated to establish a high-performance computing processor design, and the data rate of up to 8 Gb/s with relatively low power and area overhead is explored [29]. The development and manufacturing cost of AMD's 32 core CPU is reduced by 40% because of the chiplet design; this performance reveals its advantage in cost reduction [30]. Cost and yield tradeoff of chiplet and monolithic chip integration are analyzed with possible uncertainly parameters; the results show that the overall cost of chiplet design is lower than that of the monolithic chip in 5-year business planning [31]. The integrated fan-out (FO) on substrate solution is demonstrated by TSMC to achieve advanced chiplet integration; the mechanical reliability and fatigue risk of the present vehicle under temperature and humidity test are assessed [32]. In the chiplet integration design, the microbump, through via, and redistribution layer (RDL) are still regarded as the major interconnection components in 2.5D integration technology [33]. Multilayer RDL interposer packaging is regarded as the promising solution for heterogeneous integration platform; six-layer interconnection is provided for design flexibility of chiplets and high bandwidth integration in this solution [34]. In view of the thermomechanical concerns, chiplet arrangement design is harmful to the stability of electron packaging architecture because of the lower stiffness of separated chiplet than that of the single chip. Moreover, the spacing between chiplets is filled by EMC

and the overall deformation of electronic packaging vehicle is aggravated due to CTE mismatch and EMC chemical shrinkage. Chip-last process-based FO multi-chiplet integration design is developed, and its process-induced warpage and RDL stress issues are analyzed [35]. The ring- and cavity-type heat spreaders are designed to improve the warpage behavior of the concerned vehicle by the high stiffness of the heat spreader. A design concept of glass panel embedding technology is proposed; it embeds the concerned chip in the glass substrates with plated RDL and TGV to achieve a trace below 2 μm by adopting polymer RDL, and it provides a solution for warpage control [36]. Cu bridge design is improved from conformal Cu-filled via structure and has superior reliability against thermal stress [37].

The stress-induced failure in chiplet application is costly and unbearable because the failure of a single die would cause failure of the monolithic chip [30], but current studies are focused on the warpage behavior investigation of multi-chiplet systems [32,35]. Accordingly, the stress generation mechanism during fabrication of chiplet integration vehicle needs to be explored and the induced stress needs to be managed to improve long-term reliability. In this study, the FEA-based submodeling technique integrated with equivalent material approach is used to simulate the process-oriented thermomechanical responses of glass interposer architecture integrated with multi-chiplet; the difficulty in prediction accuracy and computing resource of glass interposer model is conquered with fine pitch TGV array (Figure 1). The process-oriented simulation is enabled by the element activation and deactivation technique and used to explore the stress generation mechanism of TGV interposer with chiplet arrangement during curing. Moreover, the analysis of variance (ANOVA) is utilized to reveal the significance of different structural layout design parameters, namely, TGV via diameters, TGV pitch, and EMC thickness, on stress generation in the concerned glass interposer.

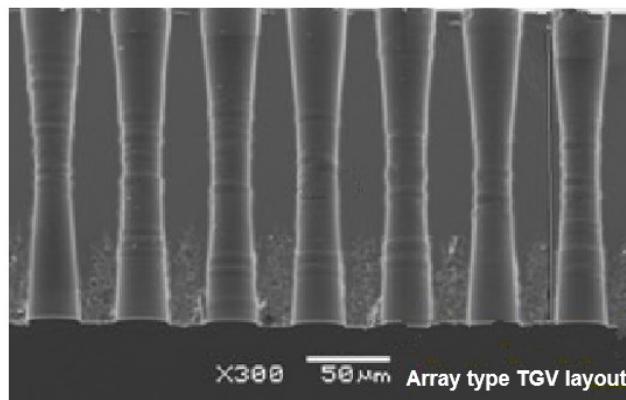


Figure 1. Cross-sectional view of array-type TGV layout in glass interposer architecture.

2. Structural layout design and fabrication process of glass interposer architecture with Cu-filled TGV array

As illustrated in Figure 2, the utilized glass interposer vehicle has 100 mm \times 100 mm area and eight chips including four Si chips with 10 mm \times 10 mm area and four Si chips with 10 mm \times 20 mm area. The gap between each chip is 15 mm. The thicknesses of the Si chip, glass interposer, and EMC are designed as 0.2, 0.5, and 0.5 mm, respectively. The considered structural layout parameters of TGV, namely, via diameter and via pitch, are defined as 28 μm and 1 mm, respectively, for the baseline design. The detailed fabrication process has been demonstrated in the previous study [38]. The process steps are described as follows. Eight Si chips are mounted on the Cu metallization layer surface at room temperature. The glass interposer is fixed at the vacuum platform to prevent sliding during subsequent curing and cooling. The chamber is preheated up to 130 °C, which is designed as the curing process temperature. A compressive loading of 5.5 kgf/cm² (0.539 MPa) is subsequently loaded to complete the curing process of the utilized EMC. The loaded compression load is removed, and the glass interposer vehicle is cooled down to room temperature to complete the entire fabrication process. Notably, the specific material characteristic of the adopted EMC, that is, chemical shrinkage, is 0.1083% under fully cured condition.

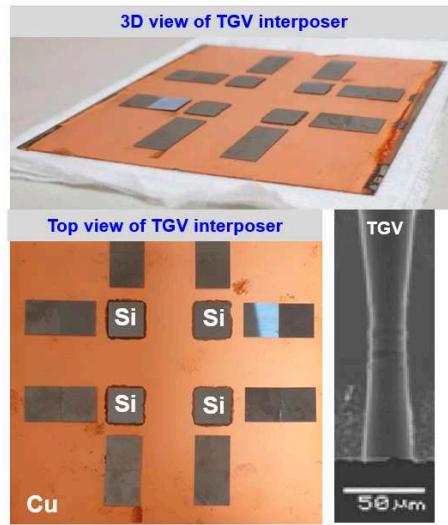


Figure 2. Optical and SEM image of the utilized glass interposer vehicle with multi-chiplet arrangement design.

3. Utilization of equivalent material approach and submodeling technique on stress generation mechanism estimation of glass interposer architecture with multi-chiplet arrangement

3.1. Equivalent material test approach for the equivalent mechanical property extraction of glass interposer with TGV array

The equivalent material test approach is utilized in this study to conquer the mesh gridding and numerical convergence issue of FEA modeling with over thousands Cu-filled TGV. Three types of material tests, namely, temperature change, uniaxial tension, and shear tests, are performed to extract the corresponding CTE, Young's modulus, and shear modulus of single unit of TGV array, as illustrated in Figure 3. As shown in Figure 3(a), the single unit TGV is composed of glass interposer, Cu-filled via, and Cu RDL layer. This TGV unit can be regarded as the representative volume element in the entire TGV array and is used to simplify the difficulty in FEA modeling construction by utilizing equivalent material test approach. The material properties utilized in the present simulation work are listed in Table 1. The material characteristics of glass and Cu are adopted into the extraction of equivalent material properties of TGV unit cell. The CTE behavior is the critical property to estimate the thermomechanical response of the present vehicle. It can be extracted by the deformation of TGV unit cell under given temperature change ΔT [Figure 3(b)]. The corresponding strain along each axis is expressed as follows:

$$\varepsilon_x = \alpha_x \Delta T, \quad \varepsilon_y = \alpha_y \Delta T, \quad \varepsilon_z = \alpha_z \Delta T \quad (1)$$

where ε denotes the induced strain under given temperature change, and α is the CTE characteristic.

The equivalent Young's modulus along each axis can be extracted in accordance with the ratio relationship of applied normal stress divided by the corresponding induced strain [Figure 3(c)]. Notably, all the displacement degrees of freedom (DOFs) on central point of TGV unit cell are fixed to prevent the rigid body motion during the uniaxial tension test. The equivalent Young's modulus is separately extracted by the tension test along different axes, and the equivalent Poisson's ratio can also be calculated by the ratio of strain amplitude between any two orthogonal axes. The detailed expressions of equivalent Young's modulus and Poission's ratio estimation are

$$\sigma_x = E_{eq_x} \varepsilon_x, \quad \sigma_y = E_{eq_y} \varepsilon_y, \quad \sigma_z = E_{eq_z} \varepsilon_z \quad (2)$$

$$\nu_{eq_xy} = -\frac{\varepsilon_y}{\varepsilon_x}, \quad \nu_{eq_xz} = -\frac{\varepsilon_z}{\varepsilon_x}, \quad \nu_{eq_yz} = -\frac{\varepsilon_y}{\varepsilon_z} \quad (3)$$

where σ , E , and ν represent the applied normal stress, Young's modulus, and Poission's ratio, respectively.

The equivalent shear test is performed to extract the corresponding shear modulus of TGV unit cell. As illustrated in Figure 3(d), the displacement DOF on the bottom surface of the TGV unit cell is

fixed. An external constant displacement is subsequently applied to the opposite surface. Under the assumption of a small deformation, the shear strain is determined by the ratio of given displacement/height of TGV unit cell. Moreover, the reacting force on the bottom surface of TGV unit cell is induced while the foregoing constant displacement is exerted. Accordingly, the equivalent shear modulus can be calculated by

$$\tau_{xz} = G_{eq_xz} \gamma_{xz}, \quad \tau_{xy} = G_{eq_xy} \gamma_{xy}, \quad \tau_{yz} = G_{eq_yz} \gamma_{yz} \quad (4)$$

where τ , G , and γ denote the shear stress, shear modulus, and shear strain in the shear test. The structural dimension dependence of TGV unit cell can be effectively estimated using the aforementioned equivalent material tests. The corresponding equivalent material properties under different TGV diameters and pitches are extracted and summarized in Table 2. These properties are utilized in the following FEA simulation work with various TGV layout parameters.

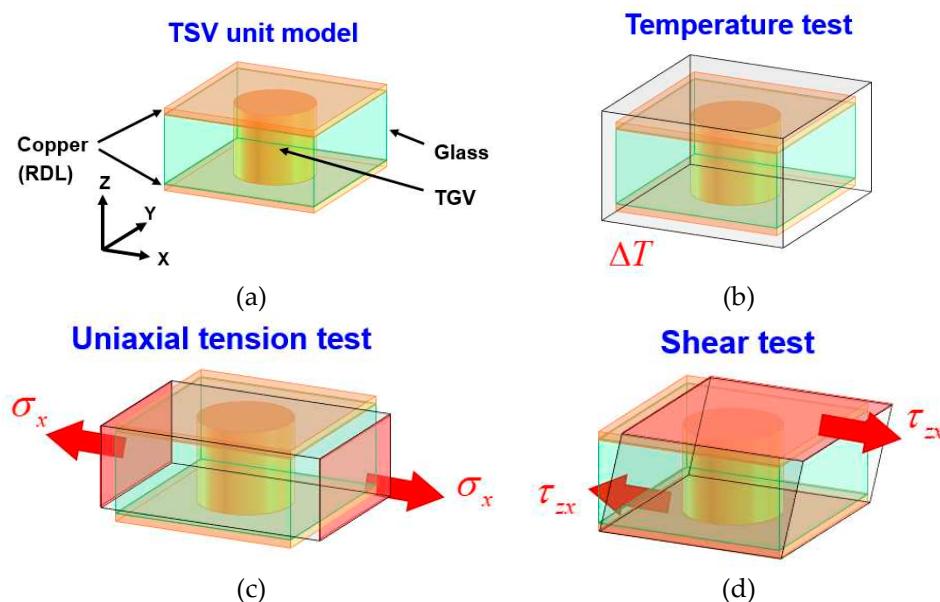


Figure 3. Graphical explanation of equivalent material property extraction on glass interposer: (a) Representative TGV unit cell; (b) Schematic of temperature test; (c) Schematic of uniaxial tension test; (d) Schematic of shear test.

Table 1. Material properties utilized in the FEA stress simulation of the present glass interposer with chiplet arrangement.

Components	E (GPa)	ν	CTE (ppm/K)
EMC	8	0.30	8.5
Si chip	169	0.30	3
Glass interposer	73	0.16	0.52
Cu	115	0.34	18

Table 2. Structural dimension dependence of TGV unit cell under different TGV diameters and pitches.

TGV parameters		E (GPa)		G (GPa)		Poisson's ratio	CTE (ppm/K)	
Diameter	60 μm	X	85.4389	XY	34.7356	XY	0.230	X 7.96
		Y	85.4389	YZ	34.7336	YZ	0.215	Y 7.96
Pitch	0.5 mm	Z	81.9116	XZ	34.7336	XZ	0.215	Z 6.12
Diameter	44 μm	X	85.3156	XY	34.6976	XY	0.230	X 7.90
		Y	85.3156	YZ	34.6964	YZ	0.214	Y 7.90
Pitch	0.5 mm	Z	81.7130	XZ	34.6964	XZ	0.214	Z 6.01
Diameter	28 μm	X	85.2308	XY	34.6713	XY	0.229	X 7.85
		Y	85.2308	YZ	34.6708	YZ	0.214	Y 7.85
Pitch	0.5 mm	Z	81.5743	XZ	34.6708	XZ	0.214	Z 5.93
Diameter	60 μm	X	85.2397	XY	34.6740	XY	0.229	X 7.85
		Y	85.2397	YZ	34.6735	YZ	0.214	Y 7.85
Pitch	1 mm	Z	81.5870	XZ	34.6735	XZ	0.214	Z 5.94
Diameter	44 μm	X	85.2090	XY	34.6645	XY	0.229	X 7.84
		Y	85.2090	YZ	34.6643	YZ	0.213	Y 7.84
Pitch	1 mm	Z	81.5374	XZ	34.6643	XZ	0.213	Z 5.91
Diameter	28 μm	X	85.1878	XY	34.6580	XY	0.229	X 7.83
		Y	85.1878	YZ	34.6579	YZ	0.213	Y 7.83
Pitch	1 mm	Z	81.5027	XZ	34.6579	XZ	0.213	Z 5.89
Diameter	60 μm	X	85.1900	XY	34.6587	XY	0.229	X 7.83
		Y	85.1900	YZ	34.6585	YZ	0.213	Y 7.83
Pitch	2 mm	Z	81.8059	XZ	34.6585	XZ	0.213	Z 5.89
Diameter	44 μm	X	85.1823	XY	34.6563	XY	0.229	X 7.82
		Y	85.1823	YZ	34.6562	YZ	0.213	Y 7.82
Pitch	2 mm	Z	81.4934	XZ	34.6562	XZ	0.213	Z 5.89
Diameter	28 μm	X	85.1770	XY	34.6546	XY	0.229	X 7.82
		Y	85.1770	YZ	34.6546	YZ	0.213	Y 7.82
Pitch	2 mm	Z	81.4848	XZ	34.6546	XZ	0.213	Z 5.88

3.2. FEA modeling of glass interposer with multi-chiplet arrangement

The utilized glass interposer architecture in this study comprises a 100 mm \times 100 mm interposer and array-type Cu-filled TGV with a via diameter of 28 μm and a TGV pitch of 1 mm. Multiple-chiplet arrangement design is further attached on the glass interposer unlike the original vehicle utilized in the previous study [38]. As shown in Figure 4, a one-quarter FEA model of an entire glass interposer vehicle is built in accordance with the symmetry of structure design. The boundary condition of the constructed model is described as follows. The inner side planes are set as symmetric plane based on the symmetry of utilized glass interposer vehicle. All the displacement DOFs on the bottom of the central axis are fixed to prevent movement of the rigid body during the mechanical response simulation. The concerned region is regarded as the local model and constructed with detailed components: Si chip, glass interposer, Cu metallization layer, and molded EMC. In the simulation work, the submodeling technique is utilized and integrated with equivalent material approach to further overcome the difficulty in mesh gridding and convergence issues. The displacement field generated from the thermocompression process of the global glass interposer model is extracted and subsequently interpolated into the local model as the boundary conditions. The thermocompression process-induced mechanical responses are introduced in the concerned region. The accuracy and stability of the prediction are also validated, which indicates that at least a 4 \times 4 TGV array needs to be constructed in the local model to gain a stable and reliable simulation result.

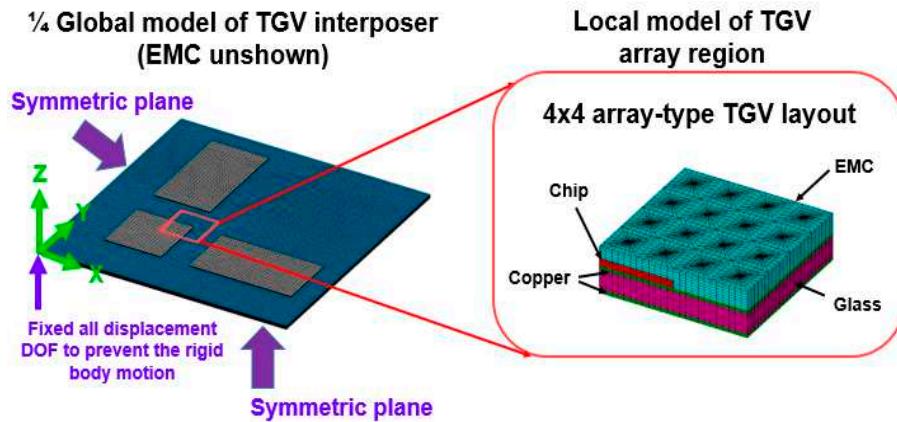


Figure 4. Fabrication process diagram of glass interposer with array-type and process conditions and material components.

3.3. Thermomechanical stress distribution and generation mechanism of glass interposer with multi-chiplet arrangement under the thermocompression process loading

To explore the critical stress location in curing, the simulated stress contour of glass interposer with Cu-filled TGV array during the curing temperature of 130 °C is shown in Figure 5. A maximum first principal stress of 130.75 MPa is observed, and it is not generated on the external surface of TGV interposer but is detected in the TGV array region. Detailed stress contour of TGV array region is extracted and the cross-sectional stress contour through A-A' line reveals that the curing process-induced stress is concentrated at the sidewall region of TGV via. This stress generation mechanism can be explained by the CTE mismatch phenomenon between major components in the present vehicle, namely, Cu, glass interposer, and capped EMC. From the viewpoint of solid mechanics, the stress in temperature-related process is generated by the CTE mismatch and corresponding thermal deformation difference. The CTE characteristics of the three components above are 18, 0.52, and 8.5 ppm/K, respectively. Under the temperature loading, the CTE mismatch between Cu/glass and glass/EMC are estimated to be different by 34.61 and 16.35 times. Accordingly, larger CTE mismatch-induced deformation is generated at Cu/glass interface than that at the glass/EMC interface. The potential cracking might occur in glass interposer or the bonded interface between glass interposer and Cu-filled via. These phenomena are also explored in Okoro's work [13,14]. The aforementioned literature mentions that the radial cohesive crack might form in the glass during heating, and the Cu metallization thickness dependence stress generated in glass substrate is estimated. The maximum stress of glass interposer under 130 °C temperature loading presented in the current study is comparable to the results revealed in Okoro's work [13]. However, the other TGV-related structural layout designs, including TGV via diameter and TGV pitch, are not discussed in the literature. A parametric study considering the aforementioned structural layout parameters is performed and the significance of each parameter is analyzed by ANOVA to explore the influences of foregoing layout parameters on stress generation in TGV interposer.

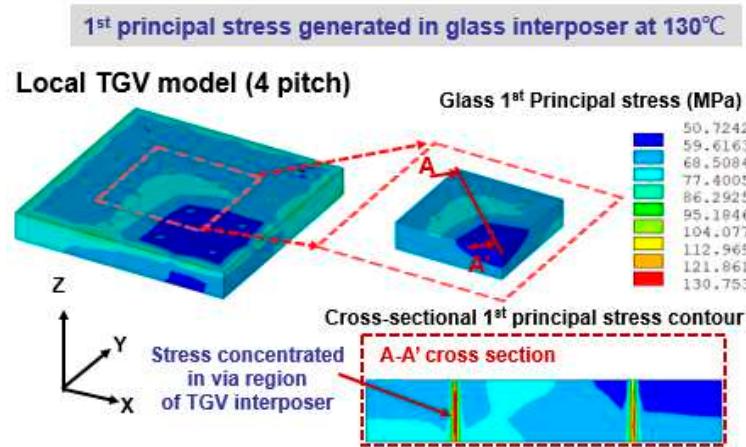


Figure 5. Simulated first principal stress contour of 4×4 TGV array region under the temperature loading of 130 °C during curing.

Stress introduced during cooling might cause the circumferential-type cracking in TGV architecture [13,14]. For this reason, stress contour of glass interposer structure is also extracted to investigate the stress distribution and magnitude generated by the cooling procedure. As shown in Figure 6, the critical stress location is revealed as bottom plane of TGV interposer. This phenomenon is attributed to the chemical shrinkage deformation of EMC generated by the curing procedure. For the EMC component utilized in this study, the chemical shrinkage amount is considered to be 0.1083% under fully cured conditions. The foregoing shrinkage deformation compresses the chip and Cu metallization layer and generates a concave-type bending profile on glass interposer. Accordingly, the stress distribution of TGV interposer is similar to the general bending stress distribution and the maximum first principal stress is introduced on the bottom plane of glass substrate. This shrinkage deformation dominates the stress distribution of the entire vehicle rather than the CTE mismatch mechanism between each component, which is due to that the CTE mismatch during room temperature is limited. The chemical shrinkage-induced stress in TGV interposer architecture after cooling is significantly lower than the stress level generated from the curing procedure. However, the concave bending profile might cause the misalignment issue and affect the stability of the concerned vehicle in subsequent assembly or reliability test. Accordingly, a parametric study is also performed to estimate the stress generated in concerned TGV interposer after cooling.

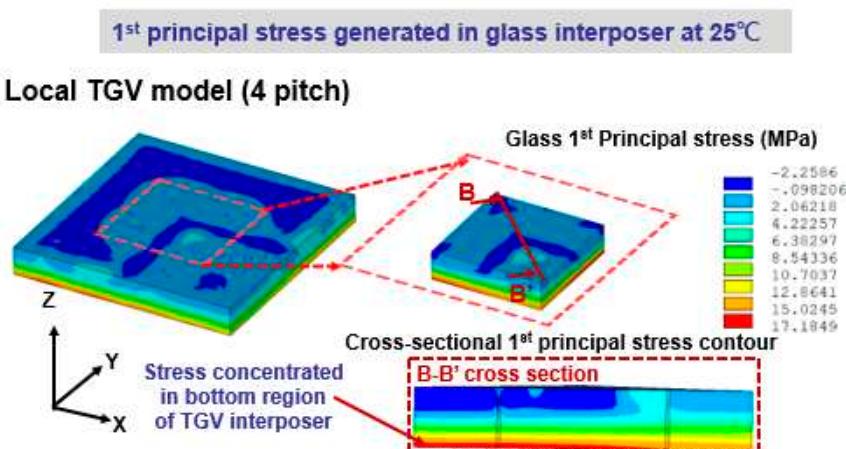


Figure 6. Simulated first principal stress contour of 4×4 TGV array region after the TGV interposer vehicle cooling down to the room temperature of 25 °C.

3.4. Sensitivity analysis of different structural parameters of TGV array on stress generation of glass interposer

A three-factor, three-level full factorial design is used based on ANOVA to explore the significance of several layout design parameters on stress generation. In this analysis, structural design factors, namely, TGV via diameter, TGV pitch, and EMC thickness, are utilized to check their effect on the induced first principal stress of glass interposer. The low, medium, and high levels of TGV via diameter and pitch are considered to be 28, 44, and 60 μm and 0.5, 1, and 2 mm, respectively. The three levels of designed EMC thickness are 250, 375, and 500 μm , respectively. The half-normal probability plots of first principal stress generation during curing at 130 $^{\circ}\text{C}$ and subsequent cooling process are illustrated in Figures 7(a) and 7(b). In Figure 7, the factor mark away from the fitting line represents its significance on first principal stress generation. From Figure 7(a), the induced stress during curing is mainly dominated by the design factor B (TGV pitch), followed by the designed EMC thickness. The interaction effect between designed factors, namely, AB (TGV diameter and pitch) and BC (TGV pitch and EMC thickness), slightly influences the first principal stress introduced in glass interposer. Similar to the trend revealed in Figure 7(a), the stress-induced significance from cooling is also illustrated in Figure 7(b). It is dominated by the EMC thickness, followed by the TGV pitch. However, the interaction effect between design factors is nearly negligible. This phenomenon is attributed to that the shrinkage deformation amount depends on EMC thickness, and the TGV pitch is the major factor that affects the overall stiffness of Cu-filled TGV interposer because of the higher stiffness of Cu than that of glass. The detailed discussion on stress generation mechanism and related design rule exploration is described in the following section.

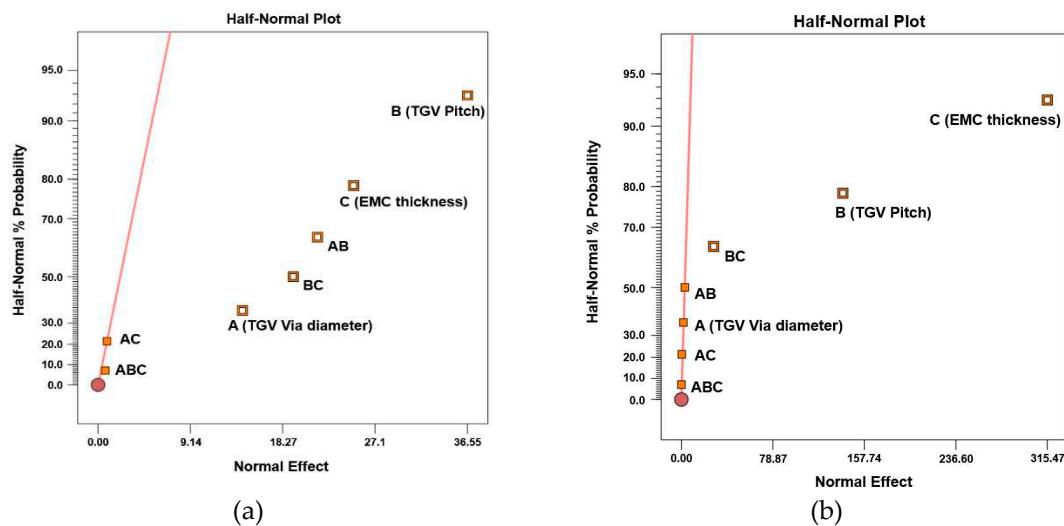


Figure 7. Half-normal probability plot of stress magnitude generated in TGV interposer architecture: (a) During curing at 130 $^{\circ}\text{C}$; (b) After cooling down to room temperature.

4. Results and discussion

4.1. Stress generation on glass interposer during high-temperature curing with various structural layout design parameters

The layout dependence first principal stress generated in the designed TGV interposer during curing at 130 $^{\circ}\text{C}$ is illustrated in Figure 8. Multiple stress trends on glass interposer can be observed under the integrated influence of EMC thickness, TGV diameter, and TGV pitch design. The introduced first principal stress is proportional to the decrease in EMC thickness. The curing process-induced stress on glass interposer is increased from 130.8 MPa to 132.6 MPa when the EMC thickness is decreased from 500 μm to 250 μm . Notably, the TGV diameter and pitch are fixed at the baseline designs of 28 μm and 1 mm, respectively. The aforementioned phenomenon can be attributed to that the thinned EMC thickness decreases the rigidity of EMC, and the foregoing EMC will be constrained by the Cu layer above the glass interposer. In other words, the Cu layer can be regarded as a buffer

layer to prevent the extrusion of glass under the thermal expansion of EMC at 130 °C. Moreover, the stress influence of varied EMC thickness is considered to insignificantly cooperate with other structural parameters, namely, TGV via diameter and TGV pitch. Therefore, the interactive effect on stress generation in TGV interposer architecture is mainly induced on the structural characteristics of TGV via, including via diameter and pitch design. The interactive effect of different TGV via diameters and pitch designs on first principal stress of glass interposer is also expressed in Figure 8. The generated first principal stress is relatively limited in the TGV pitch design of 1 μm, but higher stress values are observed at the pitch designs of 0.5 and 2 μm. The phenomenon might be explained by the rigidity change of TGV array in glass interposer architecture. The TGV array with a pitch design of 1 μm has a well-balanced rigidity that can handle the chemical shrinkage of EMC. It also has a decent flexibility to release partial stress through the deformation. The TGV array with a via pitch design of 0.5 μm has difficulty releasing the stress through its flexibility because the narrow via pitch of TGV array enhances its stiffness, and the TGV array with a via pitch design of 2 μm cannot separate the curing process-induced stress to multiple TGV via because of the large via pitch between each TGV via. Accordingly, the different EMC thickness design is regarded as manageable because of its linear influence on generated first principal stress of glass. However, the design of TGV via diameter and pitch should be explored carefully considering the interactive effect between foregoing structural parameters.

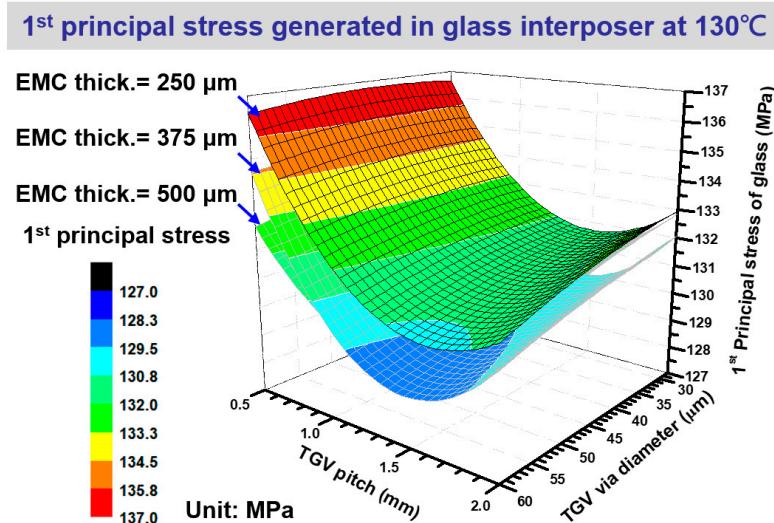


Figure 8. Comprehensive first principal stress influence on glass interposer with various EMC thicknesses, TGV via diameters, and TGV pitches during curing at 130 °C.

4.2. Stress generation on glass interposer during cooling with various structural layout design parameters

After the curing process with 130 °C temperature of EMC, the entire glass interposer is cooled down to the room temperature (25 °C in the present fabrication process). Moreover, the critical stress location is transferred from the sidewall of TGV via to the bottom of glass interposer. As illustrated in Figure 9, the first principal stress introduced in glass interposer is dominated by the designed EMC thickness, and it is slightly influenced by the TGV pitch. Notably, the TGV diameter is observed with an approximately zero effect on the induced first principal stress. Based on the stress generation mechanism revealed in Figure 6, the chemical shrinkage of EMC dominates the stress magnitude and distribution of glass interposer which is cooled down to room temperature. Accordingly, the concerned stress is enhanced from 11.47 MPa to 19.47 MPa when the EMC thickness is increased from 250 μm to 500 μm with the increased volume of EMC and enlarged corresponding chemical shrinkage amount. Moreover, the increased TGV pitch suppresses the concentrated stress on the bottom plane of glass interposer. This phenomenon is attributed to that the enlarged TGV pitch also decreases the density of TGV array and the corresponding stiffness. Accordingly, the glass interposer can release the suffered stress by the flexibility of glass interposer itself. From the abovementioned discussion,

the stress generation mechanism of glass interposer with multi-chiplet integration under thermocompression and curing process is investigated. The critical stress locations during heating and cooling are the sidewall of Cu-filled via and the bottom surface of glass interposer, respectively. The maximum simulated first principal stresses of glass interposer during curing and cooling are 132.60 and 19.47 MPa, respectively. The process-induced stress of glass interposer after cooling is relatively manageable compared with the stress introduced from the curing process. Accordingly, the critical process step in the present glass interposer architecture with multi-chiplet is explored as the curing procedure. The corresponding process parameters will be an important issue to be addressed for subsequently improving the mechanical reliability of glass interposer structure. The arrangement design of multi-chiplet integration will also be a notable factor when the dense and specific chiplet arrangement with different overall stiffness and volume proportions of capped EMC are considered in the future.

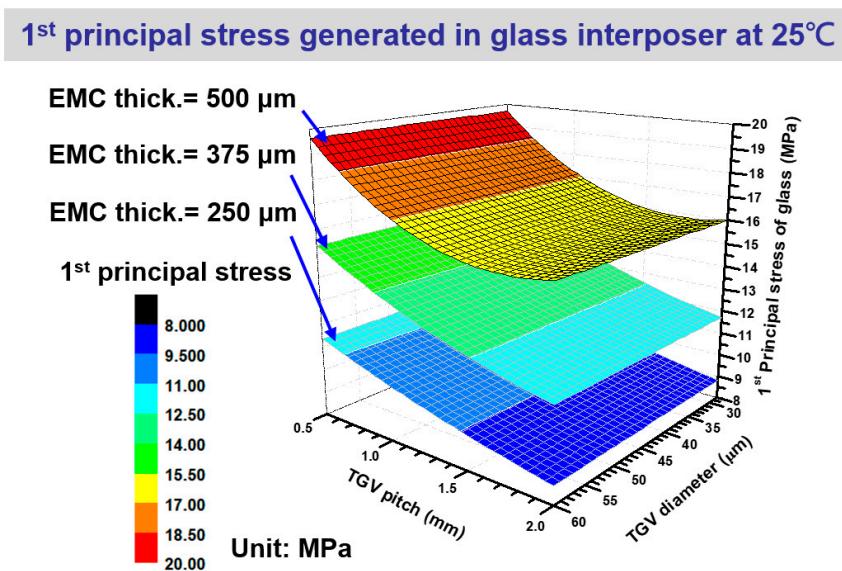


Figure 9. Comprehensive first principal stress influence of glass interposer with various EMC thicknesses, TGV via diameters, and TGV pitches after curing and cooling down to room temperature.

5. Conclusions

In this study, the comprehensive stress influence of glass interposer integrated with multi-chiplet arrangement is investigated by the FEA-based process-oriented stress simulation and submodeling technique. The curing process is explored as the critical process with high potential cracking risk because the harsh stress is observed on the sidewall of Cu-filled via region among glass interposer with multi-chiplet. A three-factor, three-level full factorial design analysis is performed based on ANOVA to explore the dominant design factor of process-induced stress generation. The design factors of TGV pitches and EMC thicknesses are the dominant factors on introduced stress magnitude during curing and cooling, respectively, and the interaction effect between each design factor is insignificant. Notably, a decent trade-off on the designed EMC thickness is needed to balance the induced stress magnitude in the fabrication process of TGV interposer architecture. From the stress induced by curing process with a temperature loading of 130 °C, the introduced first principal stress is up to approximately 130 MPa and might cause the brittle cracking phenomenon on the glass interposer itself. This study contributes to literature by exploring the design rules on thermomechanical stress management of glass interposer architecture with Cu-filled TGV structure of chiplet arrangement design.

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