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# High static gain DC-DC Double Boost Quadratic Converter

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*Article*

# High Static Gain DC-DC Double Boost Quadratic Converter

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**Abstract:** This paper presents a comprehensive study and the analysis of a topology of a no isolated DC-DC intituled Double Quadratic Boost converter with high static gain. This converter has the main advantage of high static gain and low voltage stress on its switches. The article will first present the theoretical analysis of the converter operating in an open loop. The objective of the work is the mathematical modeling and the control strategy of the converter, as well as the validation through closed-loop experimental results. Besides, we presented the practice test results to demonstrate the operation of the converter, such as the static gain experimental curve, the practice efficiency of the converter, and the control of the output voltage, as well as the capacitor voltage balance control. The authors designed a prototype for 1 kW, with a switching frequency of $f_s = 50\ kHz$, with FPGA-based command and modulation.

**Keywords:** DC-DC converter; high static gain; control strategy; FPGA

## 1. Introduction

Currently, concern for the environment has increased with the use of new sustainable practices. In the field of energy generation, clean and renewable sources have been made available, and with that, equipment such as power converters has been required more frequently. In that regard, renewable power generation has been increasing the use of DC-DC converters in such as photovoltaic systems, as presented in [1,2], both on-grid and off-grid, [3]. To optimize the use of solar energy, it is common to use an MPPT controller (Maximum Power Point Tracking), [4]. The DC-DC converters are also used in applications with fuel cells, electric or hybrid vehicles, as in [5,6], as well as in aeronautics, [7], or even space applications, [8], in addition to uninterruptible power systems, or even powered systems by batteries that require the conversion stage. Thus, recent research study the development of low cost, high power density DC-DC converters for microgeneration applications, as presented in [9]. However, the applications of power converters are not restricted to continuous conduction, as shown by [10], which demonstrates the importance of these energy converters.

In general, one can cite the various studies in the literature on high static gain DC-DC topologies, as shown in [11–13], especially as showed in [14], in which the author proposed one of the first high static gain converters. In [16], presented the switching cell of quadratic DC-DC converters. Subsequently, the authors analyzed the converter in continuous, critical, and discontinuous conduction modes, according cited in [17]. The article [18] presented the quadratic boost converter. However, since it is a high static gain converter, the topology presented in the work mentioned, presented the disadvantage of applying the total output bus voltage to its single switch. To minimize the voltage stresses in the switch, besides presenting the study of the optimization of switching losses [19], the quasi-resonant converter was shown [20]. To gather several topologies of the high static gain DC-DC converters, in [21], it was performed a bibliographic review. New converters based on [16,17] were introduced in [22,23], thus highlighting the importance of studying new high gain DC-DC converters

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topologies. Among the various works we can mention the boost converter applied in renewable energy sources, as presented in [24].

Despite the various structures present in the literature, this paper presents a distinct topology for a high static gain converter based on the boost converter. The proposed topology has the objective of reducing semiconductor efforts through the use of two switches to support the total output bus voltage, besides having high efficiency and simple structure when compared to the other mentioned topologies, considering its symmetrical characteristic. The converter presented is called Double Boost Quadratic Converter [15].

For the theoretical analysis, presents the operating stages and waveforms of the converter operating in continuous, critical, and discontinuous conduction mode. Besides, shown the mathematical model as well as for the experimental tests, to the converter operating in continuous conduction mode. It developed dynamic modeling using a state-space model to obtain the transfer function of current and voltage plants. Also, present the experimental results for the open-loop and closed-loop converter. It is also essential to highlight the evaluation of the output capacitor voltage balance, and such characteristics may not occur naturally, with unbalanced load. Thus, it presents a control strategy aiming at equalizing these voltages.

## 2. Converter Topology

The Double Quadratic Boost Converter characterized by having a high static gain and low voltage efforts in its switches. Figure 1 shows the topology of the proposed converter. In this structure, the voltages on the $S_1$ and $S_2$ switches are equal to half of the total output voltage, $(V_0/2)$.

An interesting question that simplifies the analysis of this converter is its symmetry since the behavior of the electrical variables in the components of the upper part of the power circuit has the same conduct of the elements in the lower part, so this converter becomes multiport converter. In this section, we will present the analyzes of the converter operating in continuous, critical, and discontinuous conduction mode.

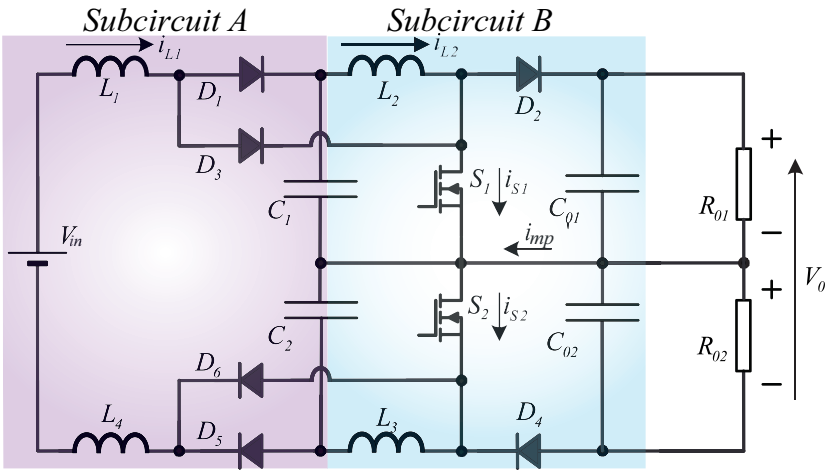


**Figure 1.** Double Boost Quadratic Converter, represented in two subcircuits called 'A' and 'B'.

### *2.1. Operation in Continuous Conduction Mode (CCM)*

In this section are shown the analysis of the operating stages, the waveforms, and the static gain curve of the proposed converter for continuous conduction mode6. Figure 2 shows the operating stages of the converter in continuous conduction mode, considering the command pulses of the simultaneous switches and duty cycle of 50%.

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2.1.1. First Stage: ($t_0$, $t_1$)

At this stage, are turned ON the switches $S_1$ and $S_2$ . The $V_{in}$ voltage source in series with the $L_1$ inductor, and the $C_1$ intermediate capacitor in series with the $L_2$ inductor, are considered as current sources. The diodes $D_2$ and $D_4$ are directly polarized, isolating the output from the input source. The current $i_{S1}$ equals the sum of $i_{L1}$ with $i_{L2}$, and the current $i_{D1}$ is null.

2.1.2. Second Stage: ($t_1$, $t_2$)

At this stage the switches $S_1$ and $S_2$ are turned OFF. The diodes $D_2$ and $D_4$ go into conduction and the current sources $I_{L1}$ and $I_{L2}$ begin to release power to the output. In this stage, the currents $i_{S1}$ and $i_{S2}$ are null, $i_{D1} = I_{L1}$ and $i_{D2} = I_{L2}$.

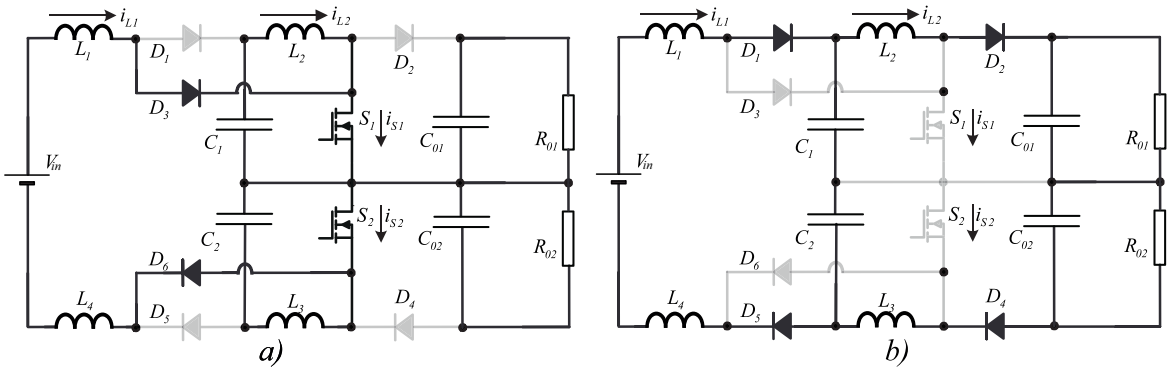


**Figure 2.** Operating stages of the converter in continuous conduction mode: (a) First stage; b) Second stage.

According to the described operating stages, Figure 3a illustrates the waveforms of the converter, with their respective time intervals corresponding to each stage. This Figure shows the $S_1$ and $S_2$ switch current, which is equal to the sum of the currents in the $L_1$ and $L_2$ inductors. The voltage on the switches $S_1$ and $S_2$ is equal to the total output voltage divided by two.

For the elaboration of the ideal static gain curve, the source $V_{in}$ and the inductor $L_1$ are considered a constant current source $I_{L1}$. The energy applied by the source in a period of operation is given by (1).

$$E_{Vin} = V_{in}.I_{L1}.T_S \tag{1}$$

The energy received by capacitor $C_1$ in the second stage of the operation is given by (2).

$$E_{VC1} = V_{C1}.I_{L1}.\triangle_{t2} \tag{2}$$

Considering the converter an ideal system, in a period of operation, all energy applied by the source $V_{in}$ is received by the intermediate capacitor $C_1$. Thus, solving (1) and (2), supply the ideal static gain for the subcircuit A of the converter, shown in (3).

$$\frac{V_{C1}}{V_{in}/2} = \frac{1}{1-D} \tag{3}$$

The same analysis is developed for the subcircuit B of the converter, considering the intermediate capacitor voltage $C_1$, as the input voltage and the capacitor voltage $C_{01}$, as the output voltage.

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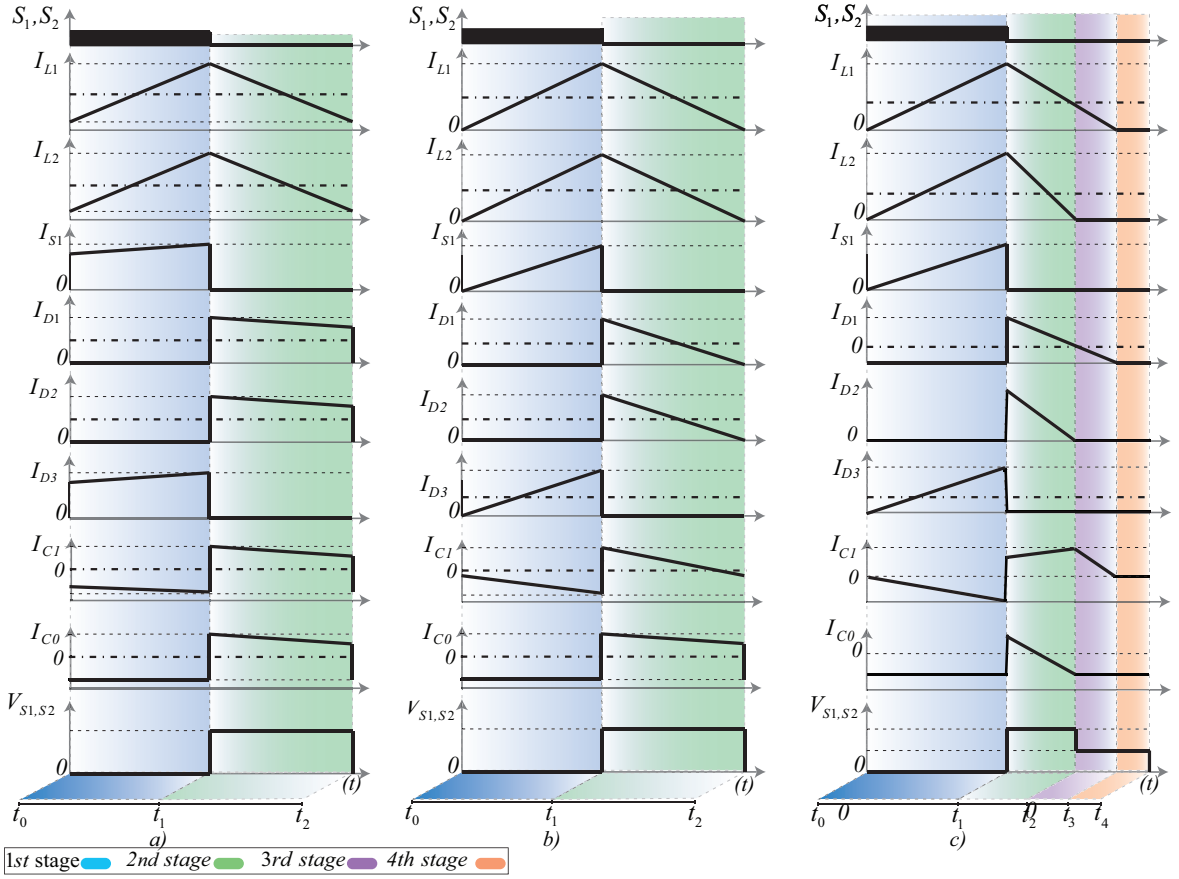


**Figure 3.** Quadratic Double Boost Converter waveforms operating in conduction mode: a) Continuous; b) Critical and c) Discontinuous.

Using the superposition principle, for the subcircuits A and B of the proposed converter, according to (3), one gets the ideal static gain of the Double Boost Quadratic Converter as a function of the output voltage by input voltage, as (4):

$$\frac{V_0}{V_{in}} = \frac{1}{(1-D)^2} \tag{4}$$

Figure 4 shows the ideal static gain as a function of the duty cycle for the Double Boost Quadratic Converter compared to the static gain of the conventional boost converter. This comparison shows the high static gain of the proposed converter, resulting from the quadratic term in the denominator of the expression (4).

For the actual static gain of the converter the non-idealities of the components due to copper in the inductor windings are included, according to the analysis shown in [25]. The voltage drops in the semiconductors are considered not relevant for the survey of the converter's actual static gain curve, and are not taken into account. Thus, through the developed analysis, similar to the analysis for the survey of the ideal static gain curve, the real static gain equation is developed, that is, considering in this case the losses in the components, as shown in Equation (5).

$$\frac{V_0}{V_{in}} = \left[\left(\frac{1}{D^*}\right) \cdot \left(\frac{1}{1+\frac{R_L}{R.D^{*2}}}\right)\right]^2 \tag{5}$$

where: $(D^* = D - 1)$.

The authors obtain actual static gain for the various ratios between inductors resistances $R_L$ and load resistance $R$. It is considered the influence of the inductor resistance value on the converter static

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gain curve, which coincides with the ideal curve when $R_L = 0$. However, the concern with minimizing the inductor resistance value of the Double Boost Quadratic Converter is greater since for values of $R_L \neq 0$, the static gain curve has a maximum value. Thus, any duty cycle increment from this maximum point of the curve may bring the output voltage to zero, as shown in Figure 4.

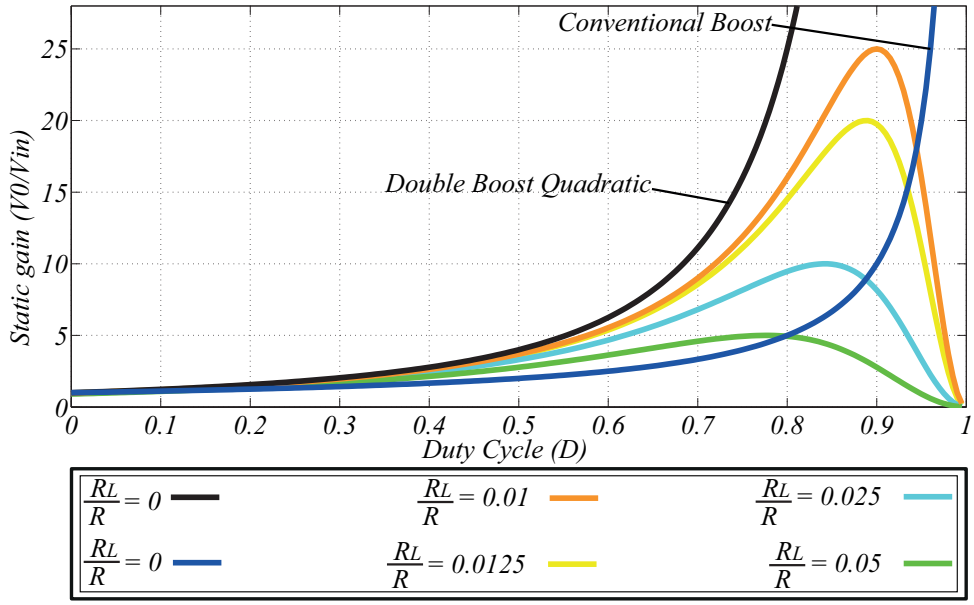


**Figure 4.** Ideal and real static gain of Double Boost Quadratic Converter for various values of $R_L/R$.

2.1.3. Current Ripple in Inductors $L_1$ and $L_2$

Starting from the voltage analysis in the $L_1$ inductor for the 1st operation stage, analyzing the subcircuit A of the converter, is obtained the current ripple in the $L_1$ inductor, as shown in Equation (6):

$$\triangle i_{L1} = V_i . \frac{D}{L_1 . f_s} \tag{6}$$

where: $V_i = V_{in}/2$

Knowing that $\triangle i_{L1} = I_{\max L1} - I_{\min L1}$, it is possible to calculate the maximum and minimum current values on the $L_1$ inductor. The average output current of the converter subcircuit A (current in the intermediate capacitors ($C_1$ and $C_2$), can be called intermediate current $I_C$, is given by $I_C = I_{D1\_avg}$:

$$I_{D1\_avg} = I_{L1\_avg} . \triangle_{t_2} \tag{7}$$

$$I_C = \frac{(I_{\min L1} + I_{\max L1})}{2} . (1 - D) \tag{8}$$

Rewriting the equation regarding the current variation of the $\triangle i_{L1}$ inductor as a function of the maximum current $I_{\max L1}$, it is obtained:

$$I_{\max L1} = \triangle i_{L1} + I_{\min L1} \tag{9}$$

Substituting Equation (6) in 9 and Equation (9) in 8, it is obtained:

$$I_C = \frac{1}{2} \cdot \left( I_{\min L1} + V_i . \frac{D}{L_1 . f_s} + I_{\min L1} \right) \cdot (1 - D) \tag{10}$$

Therefore, the maximum and minimum values of the inductor current $L_1$ are given as a function of the current of the intermediate capacitor $I_C$:

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$$I_{\max\_\min\_L1} = \frac{I_C}{(1-D)} \pm V_i . \frac{D}{2.L_1.f_s} \tag{11}$$

Repeating the analysis of inductor $L_1$, for inductor $L_2$, referring to subcircuit B of the converter. Again, from the analysis of the voltage in the inductor, for the 1st stage of operation, the current ripple in the inductor $L_2$ is obtained, as shown in Equation (12).

$$\triangle i_{L2} = V_{C1} . \frac{D}{L_2.f_s} \tag{12}$$

From the current ripple in the inductor $\triangle i_{L2} = I_{\max L2} - I_{\min L2}$, it is possible to calculate the maximum and minimum current values in the inductor $L_2$. The average output current $I_0$, is given by $I_0 = I_{D2\_avg}$:

$$I_{D2\_avg} = I_{L2\_avg} . \triangle_{t_2} \tag{13}$$

$$I_0 = \frac{(I_{\min L2} + I_{\max L2})}{2} . (1-D) \tag{14}$$

Rewriting the equation for current variation in the $\triangle i_{L2}$ inductor as a function of the maximum current $I_{\max L2}$, it is obtained:

$$I_{\max L2} = \triangle i_{L2} + I_{\min L2} \tag{15}$$

Substituting Equation (12) in 15, and Equation (15) in 14, it is obtained:

$$I_0 = \frac{1}{2} . \left( I_{\min L2} + V_{C1} . \frac{D}{L_1.f_s} + I_{\min L2} \right) . (1-D) \tag{16}$$

Therefore, the maximum and minimum values of the inductor current $L_2$ as a function of the output current $I_0$, are given by:

$$I_{\max\_\min\_L2} = \frac{I_0}{(1-D)} \pm V_{C1} . \frac{D}{2.L_2.f_s} \tag{17}$$

#### 2.1.4. Converter Component Design

Considering the principle of volt-second balance in the inductor and knowing that the Equation (11) defines the maximum and minimum values for the $L_1$ inductor, and still that the current ripple in the inductor is given as shown in Equation (9), the value of the $L_1$ inductor is calculated by isolating it in the Equation (6) and considering the 1st stage of operation of the converter. Again, based on the volt-second balance principle for the $L_2$ inductor, and considering that Equation (17) defines the maximum and minimum values for the $L_2$ inductor, the same is calculated by isolating it in Equation (12) and considering the 1st stage of operation of the converter, as shown in Table 1 respectively.

Due to the symmetry of the converter topology, the values of the inductors $L_3$ and $L_4$ are given by: $L_3 = L_2$ and $L_4 = L_1$. Considering the topology of the symmetrical converter, the other components located in the lower region of the converter will not be present during the design, because they have their respective dual dimensioned.

Considering the charge balance in the intermediate capacitor, and also its voltage ripple, the capacitance value is calculated so that the capacitor is charged and discharged linearly at each operating period. Thus, the intermediate capacitor is calculated using the expression presented in Table 1. Similar to the analysis performed for the calculation of the intermediate capacitor, the output capacitor is calculated using the expression shown in Table 1. Finally, the load resistance is calculated using the power expression, as shown in Table 1.

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**Table 1.** Converter Component Design.

| Component | Calculation to obtain parameters |
|---|---|
| Inductor $L_1$ | $L_1 = \frac{V_i.D.T_s}{\triangle i_{L1}}$ |
| Inductor $L_2$ | $L_2 = \frac{V_{C1}.D.T_s}{\triangle i_{L2}}$ |
| Intermediate Capacitor $C_1$ | $C_1 = \frac{(I_C - I_0).D.T_s}{\triangle V_{C1}}$ |
| Output Capacitor $C_{01}$ | $C_{01} = \frac{I_0.D.T_s}{\triangle V_0}$ |
| Load Resistance $R$ | $R_0 = \frac{V_0^2}{P_0}$ |

After the component design, it is possible to calculate the efforts on the converter components for the continuous conduction mode, as shown in Table 2.

**Table 2.** Calculation of Efforts on Components of the Converter operating in CCM.

| Component | Description | Equating efforts |
|---|---|---|
| Switch $S_1$ | Average Current | $I_{S1\_avg} = \frac{1}{T_s}.\left[\frac{(I_{\min L1}+I_{\max L1})}{2} + \frac{(I_{\min L2}+I_{\max L2})}{2}\right].D.T_s$ |
| | RMS current | $I_{S1\_rms} = \sqrt{\frac{1}{T_s}.\left[\int_0^{D.T_s}\left(\frac{V_i}{L_1}.t\right)^2 dt + \int_0^{D.T_s}\left(\frac{V_{C1}}{L_2}.t\right)^2 dt\right]}$ |
| | Maximum Current | $I_{S1\_max} = I_{\max L1} + I_{\max L2}$ |
| | Maximum voltage | $V_{S1\_max} = V_{C01}$ |
| Diode $D_1$ | Average Current | $I_{D1\_avg} = \frac{1}{T_s}.\frac{(I_{\min L1}+I_{\max L1})}{2}.(1-D).T_s$ |
| | RMS current | $I_{D1\_rms} = \sqrt{\frac{1}{T_s}.\int_0^{(1-D).T_s}\left[I_{\max L1} + \left(\frac{V_i - V_{C1}}{L_1}\right).t\right]^2 dt}$ |
| | Maximum Current | $I_{D1\_max} = I_{\max L1}$ |
| | Maximum voltage | $V_{D1\_max} = V_{C1}$ |
| Diode $D_2$ | Average Current | $I_{D2\_avg} = \frac{1}{T_s}.\frac{(I_{\min L2}+I_{\max L2})}{2}.(1-D).T_s$ |
| | RMS current | $I_{D2\_rms} = \sqrt{\frac{1}{T_s}.\int_0^{(1-D).T_s}\left[I_{\max L2} + \left(\frac{V_{C1} - V_{C01}}{L_2}\right).t\right]^2 dt}$ |
| | Maximum Current | $I_{D2\_max} = I_{\max L2}$ |
| | Maximum voltage | $V_{D2\_max} = V_{C01}$ |
| Diode $D_3$ | Average Current | $I_{D3\_avg} = \frac{1}{T_s}.\frac{(I_{\min L1}+I_{\max L1})}{2}.D.T_s$ |
| | RMS current | $I_{D3\_rms} = \sqrt{\frac{1}{T_s}.\int_0^{D.T_s}\left(\frac{V_i}{L_1}.t\right)^2 dt}$ |
| | Maximum Current | $I_{D3\_max} = I_{\max L1}$ |
| | Maximum voltage | $V_{D3\_max} = V_{C1}$ |
| Inductor $L_1$ | Average Current | $I_{L1\_avg} = \frac{1}{T_s}.\left[\frac{(I_{\min L1}+I_{\max L1})}{2}.D.T_s + \frac{(I_{\min L1}+I_{\max L1})}{2}.(1-D).T_s\right]$ |
| | RMS current | $I_{L1\_rms} = \sqrt{\frac{1}{T_s}.\left\{\int_0^{D.T_s}\left(\frac{V_i}{L_1}.t\right)^2 dt + \int_0^{(1-D).T_s}\left[I_{\max L1} + \left(\frac{V_i - V_{C1}}{L_1}\right).t\right]^2 dt\right\}}$ |
| | Maximum Current | $I_{L1\_max} = I_{\max L1}$ |
| | Maximum voltage | $V_{L1\_max} = V_i$ |
| Inductor $L_2$ | Average Current | $I_{L2\_avg} = \frac{1}{T_s}.\left[\frac{(I_{\min L2}+I_{\max L2})}{2}.D.T_s + \frac{(I_{\min L2}+I_{\max L2})}{2}.(1-D).T_s\right]$ |
| | RMS current | $I_{L2\_rms} = \sqrt{\frac{1}{T_s}.\left\{\int_0^{D.T_s}\left(\frac{V_{C1}}{L_2}.t\right)^2 dt + \int_0^{(1-D).T_s}\left[I_{\max L2} + \left(\frac{V_{C1} - V_{C01}}{L_2}\right).t\right]^2 dt\right\}}$ |
| | Maximum Current | $I_{L2\_max} = I_{\max L2}$ |
| | Maximum voltage | $V_{L2\_max} = V_{C1}$ |
| Capacitor $C_1$ | Average Current | $I_{C1\_avg} = 0$ |
| | RMS current | $I_{C1\_rms} = \sqrt{\frac{1}{T_s}.\left\{\int_0^{D.T_s}\left[\left(\frac{V_{C1}}{L_2}\right).t\right]^2 dt + \int_{D.T_s}^{(1-D).T_s}\left[I_{\max L2} + \left(\frac{V_{C1} - V_{C01}}{L_2}\right).t\right]^2 dt\right\}}$ |
| Capacitor $C_{01}$ | Average Current | $I_{C01\_avg} = 0$ |
| | RMS current | $I_{C01\_rms} = \sqrt{\frac{1}{T_s}.\left\{\int_0^{D.T_s}(-I_{C01})^2 dt + \int_0^{(1-D).T_s}\left[(I_{\max L2} - I_{C01}) + \left(\frac{V_{C1} - V_{C01}}{L_2}\right).t\right]^2 dt\right\}}$ |

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### 2.2. Operation in Critical Conduction Mode

In this mode of operation, the currents in inductors $L_1$ and $L_2$ are initially zero and return to this value precisely at the end of the converter operate period. Figure 3b show the waveforms of the converter operating in critical conduction mode, with the respective time intervals corresponding to each stage.

The calculation of the critical inductances $L_1$ and $L_2$ is developed by analyzing the current ripple in the inductors. The average input current $I_{in}$ is equal to the average diode current $D_1$, and the output current $I_0$ is the average diode current $D_2$.

Through from the maximum and minimum values obtained from the input current $I_{L1\_max}$ and $I_{L1\_min}$ as a function of capacitor current $C_1$ for continuous conduction $I_C$, the critical inductance is determined by setting the value of current $I_{L1\_min}$ to zero.

$$L_{1\_CR} = \frac{V_{in}}{2.f_s.I_C}.D.(1-D) \tag{18}$$

Repeating the same analysis for the $L_2$ inductor, given the maximum and minimum values for the input current $I_{L2\_max}$ and $I_{L2\_min}$ as a function of capacitor output current to the subcircuit B ($I_0$), in continuous conduction mode, it is determined the critical inductance by setting the value of current $I_{L2\_min}$ to zero. In this case, the input voltage becomes the voltage on the intermediate capacitors ($V_C$).

$$L_{2\_CR} = \frac{V_C}{2.f_s.I_0}.D.(1-D) \tag{19}$$

### 2.3. Operation in Discontinuous Conduction Mode

This converter presents consider two situations that operate in discontinuous conduction mode. The first occurs when only the current $I_{L2}$ is in discontinuous mode, characterized in the third operation stage. Thus, in this situation, the converter operates in the first, second, and third stages of operation.

The second situation presenting the discontinuous conduction mode occurs when the currents $I_{L1}$ and $I_{L2}$ have discontinuity during the same interval, thus characterizing the fourth stage of operation. Therefore, only in this situation does the converter operate in the first, second, third, and fourth stages.

The following describes the operating stages in discontinuous conduction mode. The first and second operating stages are identical at continuous conduction mode, so they will not be described again.

#### 2.3.1. Three Stage: ($t_2$, $t_3$)

This stage transfer all energy stored in $L_2$ to the load. Therefore, the diode $D_2$ blocks, and the capacitors $C_{01}$ and $C_{02}$ maintain the voltage of the load. The $L_1$ inductor continues to supply power to the $C_1$ and $C_2$ capacitors.

#### 2.3.2. Fourth Stage: ($t_3$, $t_4$)

This last stage, all energy stored in the $L_1$ inductor is transferred, and the $D_1$ diode is blocked. In this stage only the capacitors $C_{01}$ and $C_{02}$ feed the load. Figures 5 and 3c show the operating stages and the main waveforms of the converter, respectively. As shown in Figure 3c, the voltage value at switch $S_1$ in the third and fourth operating stages is equal to half of the total output voltage less diode voltage $D_2$.

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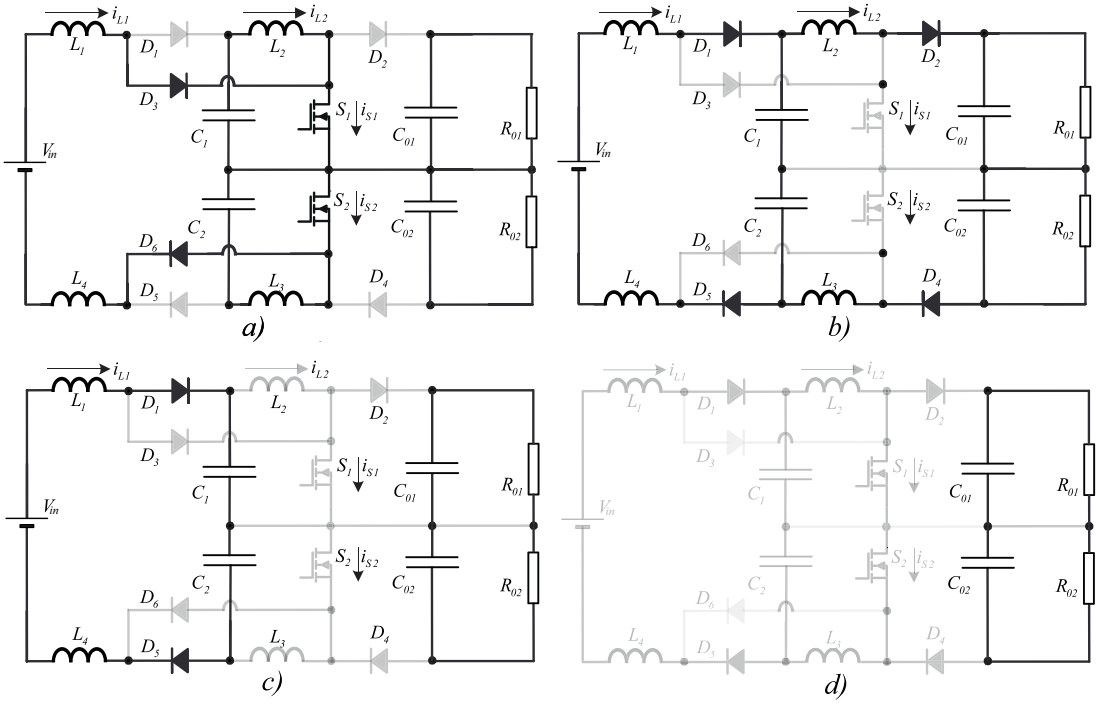


**Figure 5.** Operating stages in discontinuous conduction mode: (a) First stage; b) Second stage; c) Third stage; d) Fourth stage.

To analyze the static gain, in discontinuous conduction mode, the current ripple of inductor $L_1$ is considered. By analyzing the inductor currents $L_1$ and diode $D_1$ for the subcircuit A of the converter as shown in Figure 5, one can obtain (20).

$$I_{L1\_avg} - I_{D1\_avg} = \frac{I_{L1\_\max}}{2}.D \tag{20}$$

Assuming that the input power of the converter is equal to the sum of the powers in the intermediate capacitors, it is shown (21) for the ideal static gain and belonging to the subcircuit A:

$$\frac{V_C}{V_{in}} = 1 + \frac{V_{in}.D^2}{2.I_C.L_{1\_Dis}.f_s} \tag{21}$$

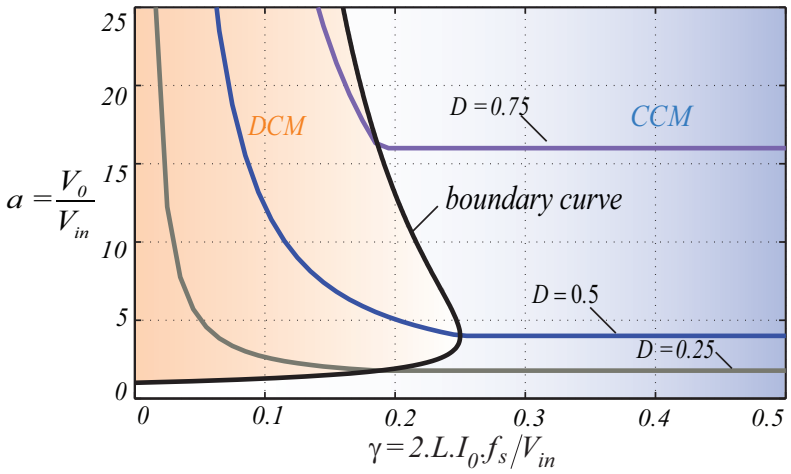


**Figure 6.** External characteristic of the proposed converter showing the boundary of the curve between CCM and DCM.

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To develop the total ideal static gain of the converter, the is used superposition principle, it is added the Equation (21) for the subcircuit A and the Equation (23) referring to the subcircuit B, getting the Equation (24). For simplicity, $L_{Dis} = L_{1\_Dis} = L_{2\_Dis}$ is also considered:

$$\frac{V_0}{V_{in}} = \left(1 + \frac{V_{in}.D^2}{2.I_0.L_{Dis}.f_s}\right)^2 \tag{22}$$

In the discontinuous conduction mode, the equations for the design can be obtained through the waveforms in each component of the circuit or by making $I_{minL1} = 0$ and $I_{minL2} = 0$, in the equations for design in continuous conduction mode.

Repeating the $L_1$ analysis for the $L_2$ inductor its obtains the ideal static gain equation for the subcircuit B:

$$\frac{V_0}{V_C} = 1 + \frac{V_{in}.D^2}{2.I_0.L_{2\_Dis}.f_s} \tag{23}$$

To develop the total ideal static gain of the converter, the is used superposition principle, it is added the Equation (21) for the subcircuit A and the Equation (23) referring to the subcircuit B, getting the Equation (24). For simplicity, $L_{Dis} = L_{1\_Dis} = L_{2\_Dis}$ is also considered:

$$\frac{V_0}{V_{in}} = \left(1 + \frac{V_{in}.D^2}{2.I_0.L_{Dis}.f_s}\right)^2 \tag{24}$$

In the discontinuous conduction mode, the equations for the design can be obtained through the waveforms in each component of the circuit or by making $I_{minL1} = 0$ and $I_{minL2} = 0$, in the equations for design in continuous conduction mode.

## 3. Dynamic Modeling and Converter Control

The authors obtained the mathematical model of systems with multiple inputs and outputs employing the state-space modeling, achieving more accurate mathematical models and representing the system precisely, as presented in [25,26]. The system can then be described by input and output equations, as shown in (25).

$$\begin{cases} \mathbf{K}\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \\ \mathbf{y} = \mathbf{C}\mathbf{x} \end{cases} \tag{25}$$

where:

$$\begin{aligned} \mathbf{x} &= \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & V_{C1}(t) & V_{C01}(t) \end{bmatrix}^T; \\ \mathbf{K} &= \text{diag}(L_1, L_2, C_1, C_{01}); \\ \mathbf{u} &= V_{in}(t). \end{aligned} \tag{26}$$

For the dynamic modeling of small signals by the state space method of the Double Boost Quadratic Converter takes into account the operating stages, converter symmetry and continuous conduction mode, as follows:

### *3.1. First Stage: $(D.T_s)$*

Through the analysis of Figure 2a, one can obtain the state matrix that determines the capacitor voltage and the current in the inductors, as shown in (27).

### *3.2. Second Stage: $(1 - D).T_s$*

The circuit illustrated in Figure 2b represents the converter operation during this stage, as shown in (27). The $C$ and $E$ arrays vary depending on the choice of output variable.

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$$\begin{cases} \mathbf{K}\dot{\mathbf{x}} = \mathbf{A}_n\mathbf{x} + \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix}^T [V_{in}(t)] \\ \mathbf{y} = \mathbf{I}_4\mathbf{x} \end{cases}, \quad n = \{1,2\} \tag{27}$$

where:

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{R} \end{bmatrix}; \quad \mathbf{A}_2 = \begin{bmatrix} 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & -1 & 0 & 0 \\ 0 & 1 & 0 & -\frac{1}{R} \end{bmatrix}.$$

The next step is to obtain the equation that determines the average model of smalls signals for the two stages of the converter. The average matrix $\mathbf{A}$ is given by:

$$\mathbf{A} = D\mathbf{A}_1 + (1-D)\,\mathbf{A}_2 \tag{28}$$

Similarly, we can find the value of the matrix $B$. With the values of the DC components, we can define the smalls signals AC model:

$$\begin{aligned} \mathbf{K}\frac{d}{dt}\hat{x} =& \mathbf{A}\hat{x}(t) + \mathbf{B}\hat{u}(t) \\ &+ \left((\mathbf{A}_1 - \mathbf{A}_2)\,\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\,\mathbf{U}\right)\hat{d}(t) \end{aligned} \tag{29}$$

where: $\hat{x}(t)$ and $\hat{u}(t)$, are small variations on the point of operation and $\mathbf{X}$ and $\mathbf{U}$ are the values of states and input in steady state.

By obtaining the matrices of the first and second stages of operation, as well as the equations that define the state-space system, the circuit transfer function is accomplished through mathematical software [27]. Through the functions of transferring the input current by the duty cycle and the output voltage by the input current obtain the mathematical model of the converter. Therefore, Equation (30) shows the transfer functions of plants to the current and voltage control loops, respectively.

$$G_{i_{L1}}(s) = \frac{\hat{i}_{L1}(s)}{\hat{d}(s)}, \quad G_{v_0}(s) = \frac{\hat{v}_0(s)}{\hat{i}_L(s)} \tag{30}$$

Besides, for the converter to be able to reject variations in output voltage and input current peaks at instants of load variations, the controllers in the voltage and current loops are designed, as presented in [28]. For the internal control of the current loop, the linear controller (PI + pole) is used to clear the error in steady state, meeting the following specifications:

The higher the compensator zero, the faster the transient response. However, the phase margin decreases, bringing the system closer to instability. The compensator pole serves to reduce the effect of the switching frequency on the current loop. It is usually positioned at half the switching frequency. Compensator gain is set to ensure the specified zero-crossing frequency (usually limited to a decade below the switching frequency). Equation (31), presents the transfer function current compensator [29]. The block diagram illustrating the projected loops is shown in Figure 7.

$$C_i(s) = k_i\frac{s + z_i}{s\,(s + p_i)} \tag{31}$$

where:

$p_i$- is positioned at half the switching frequency;

$z_i$- is positioned a decade below the crossover frequency, in other words, a decade below the switching frequency;

$k_i$- is designed so that the system has a low phase margin (higher than 45° and less than 90°) at the crossover frequency.

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For control of the external voltage loop, it adds an integral proportional compensator (PI). In first-order systems, it is usual to position the zero of the compensator PI over the plant pole, canceling it. Thus, the feedback system presents the first-order behavior.

It set the compensator gain to ensure the specified zero-crossing frequency, around 30 Hz. Typically, the voltage loop crossing frequency in DC-DC converters is related to the frequency of the drained pulsed current by the load, if an inverter is used as a load. Since this pulsed current is 120 Hz, it defines that the voltage loop crossing frequency is 1/4 of the value of this frequency. The reference (32) shows the transfer function of the projected voltage control.

$$C_v(s) = k_v \frac{s + z_v}{s} \tag{32}$$

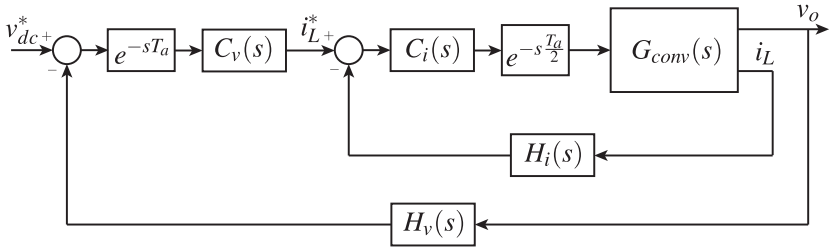


**Figure 7.** Block Diagram representing the internal current loop and the external voltage loop - $G_{conv}(s)$ represents the complete converter model, ${v_{dc}}^*$ is the reference voltage and ${i_L}^*$ represents the reference current. The $v_o$ and $i_L$ variables refer to the converter control variables.

As shown in Figure 7, in addition to the controllers employed in the current and voltage loops, a discrete control system typically includes a delay resulting basically from the sum of two parcel, the signal sampling delay and the computational delay, totaling in this project a sampling period and a half, represented by $e^{-\frac{3}{2}T_a s}$.

The internal loop current signal conditioning transfer function, $H_i(s)$, equals the association of the current sensor gain ($H_{si}$), the ADC gain ($H_{ADC}$) and the gain of the instrumentation circuits ($H_{gi}$), as expressed in (33). Voltage conditioning is equivalent, represented by the transfer function $H_v(s)$, and given by (33). In the instrumentation circuits, a low pass 1st order filter with cutoff frequency was used, being half of the switching frequency, $f_c = f_s/2 = 25\ kHz$.

$$H_x = H_{sx} \cdot H_{gx} \cdot H_{ADC}, \quad x = \{v, i\} \tag{33}$$

Finally, the ADC gain is represented by the number of discrete ADC levels divided by the maximum ADC excursion value, in this case, given by:

$$H_{ADC} = \frac{2^{12} - 1}{ADC_{\max}} \tag{34}$$

In the converter model considered the inclusion of the PWM modulator given by the maximum value of excursion of signal of analogic digital converter $(AD_{max})$ divided by a value representing the peak of the triangular carrier, in others words, dividing the frequency of operation of the FPGA $(f_{FPGA})$ by the sampling frequency, $(f_a = 2f_s)$. The Equation (35) represent the transfer function of the PWM modulator.

$$G_{PWM} = AD_{\max} \frac{2f_s}{f_{FPGA}} \tag{35}$$

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## 4. Voltage Equilibrium on the Output capacitors

Due to the converter multiports [30], the studied converter has advantages for application in photovoltaic systems, or in situations where the output voltage bus must be bipolar. In this configuration, it is possible, among others, to reduce the stresses of the switches, making it possible to couple a particular load with total bus voltage by joining two loads, each with half of the total required voltage [31,32].

Thus, when the voltage balance in the output capacitors is necessary, the voltage-balancing technique of these capacitors with a shared loop can be used, that is, the midpoint current can be controlled independently of the input current control. Thus, in addition to full control of the output voltage loop, the system features control of the voltage loop responsible for keeping the midpoint balanced, [33]. The technique is based on rejecting slight variations in output voltage, so as not to overload one of the capacitors that can assume higher voltage values or total voltage the bus while the voltage of the other capacitor becomes zero.

The main difference between the loops with separated voltage control and shared voltage control is that the latter uses control for the full voltage loop of the converter and a second control for the voltage loop of one of the capacitors to ensure the voltage balance at the midpoint. Figure 8 shows, in block diagram, the voltage balance control of the output capacitors. The blocks presented in the schematic of Figure 8 follow the similar model for the current and voltage loops shown in Figure 7.

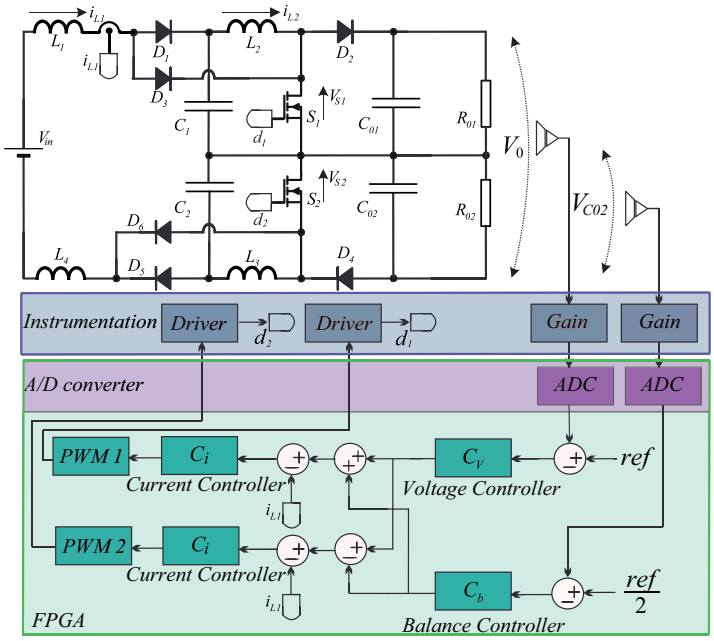


**Figure 8.** Schematic of the Double Boost Quadratic Converter with voltage balance loops, on output capacitors, and total.

The technique with shared voltage control loops has as its primary function to quickly correct the load disturbance at the transient instant. For this, it is used the characteristic that the total output voltage does not present high ripples. Therefore, the voltage loop that regulates the midpoint between the output capacitors must have relatively slow dynamics, and with a cut-off frequency much lower than the cut-off frequency of voltage control with separate loops.

The transfer function required for midpoint voltage control is obtained through the state space model by analyzing (27) for the first and second operating stages. When the converter has its load balanced, its midpoint current is zero. However, when the load is unbalanced, the midpoint current is responsible for the output voltage balance.

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## 5. Experimental Results

In this section, the authors present the experimental results of the Double Boost Quadratic converter. Table 3 shows the parameters and values of the components used in the implementation of the converter. Laboratory tests were performed with a 1 kW power prototype, as shown in Figure 9. The current and voltage sensor models used were the LTSR-25-NP and the LV-25NP from LEM.

In the development of the experimental tests was used the Altera development kit, model $BeMicroMax10$, [34]. This Kit features a $10M08DAF484$ FPGA chip, which contains an intrinsic ADC block with 18 channels, and 12 bits resolution with up to 1 MHz sampling rate. Converter digital control has been implemented in the FPGA employing the VHDL hardware description language (VHSIC HDL - Very High-Speed Integrated Circuit Hardware Description Language).

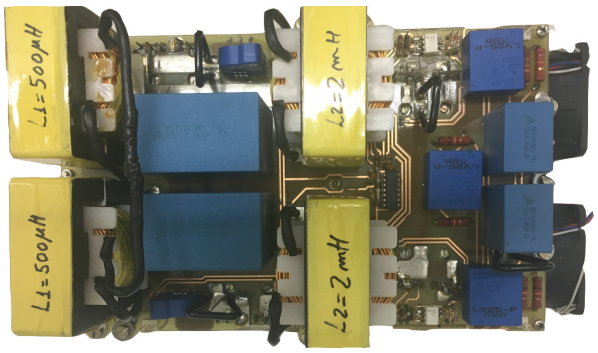


**Figure 9.** Double Boost Quadratic Converter Prototype, power 1 kW.

The FPGA has some advantages such as the real-time processing feature and high processing density, in addition it is different from microcontrollers because it has a large number of PWM outputs, but the main difference is the parallel processing feature, in other words, it is possible to process digital signals simultaneously without interaction with other processes, [34,35]. The flowchart in Figure 10 shows the parallel processing adopted for the control of the Double Quadratic Boost Converter. Each block represents a code responsible for generating the hardware description. Thus, several processes with distinct functions work simultaneously.

In this work, the FPGA does the acquisition, filtering, and processing of data, in addition to modulation and protection of the circuit. As presented in the Figure 10, the hardware description was divided and organized in different logic blocks interconnected by a flag responsible for synchronism. Data collection happens when there is no switching, in order to avoid noise. Subsequently, the reading data are filtered and sent to the control loop. Finally, they are available for use in the logic block responsible for modulation.

**Table 3.** Parameters used in the prototype of $1kW$.

| Description | Parameters |
|---|---|
| Output Voltage | $V_0 = 400V$ |
| Input Voltage | $V_{in} = 100V$ |
| Intermediate Capacitor | $C_1, C_2 = 50uF$ |
| Output Capacitor | $C_{01}, C_{02} = 12.5uF$ |
| Load Resistance | $R = 160ohms$ |
| Switching Frequency | $f_s = 50kHz$ |
| Duty Cycle $S_1, S_2$ | $D = 0.5$ |
| Input Inductance | $L_1, L_4 = 0.5mH$ |
| Intermediate Inductance | $L_2, L_3 = 2mH$ |
| Switch Models (*Mosfets*)- $S_1, S_2$ | $SPW24N60C3$ |
| Diodes Models (*Ultrafast*) - $D_1$ *a* $D_6$ | $HFA15TB60$ |

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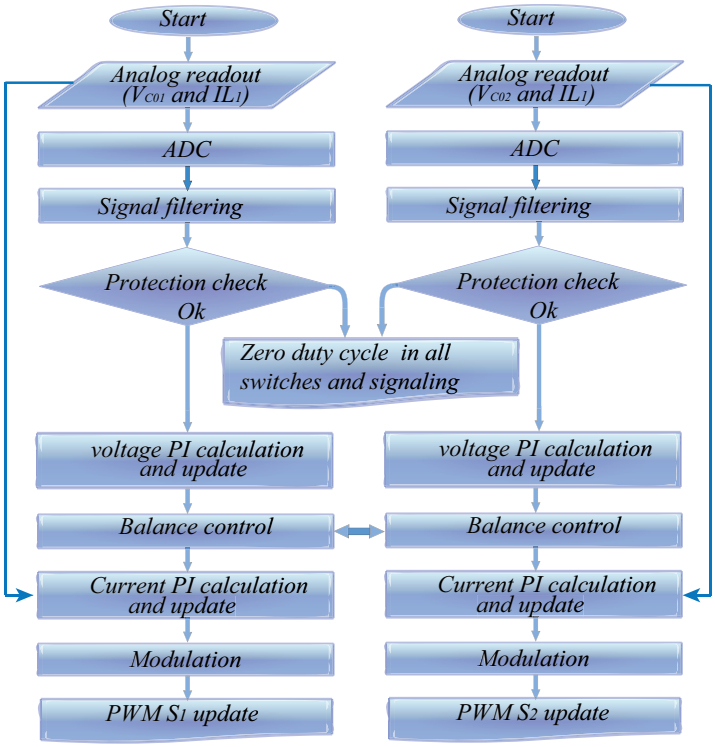


**Figure 10.** Digital control flowchart.

*5.1. Converter Operating Open Loop*

Figure 11a shows input and output voltages and Figure 11b it is observed that the voltage at the switches is halved compared to similar topologies in the literature [19].

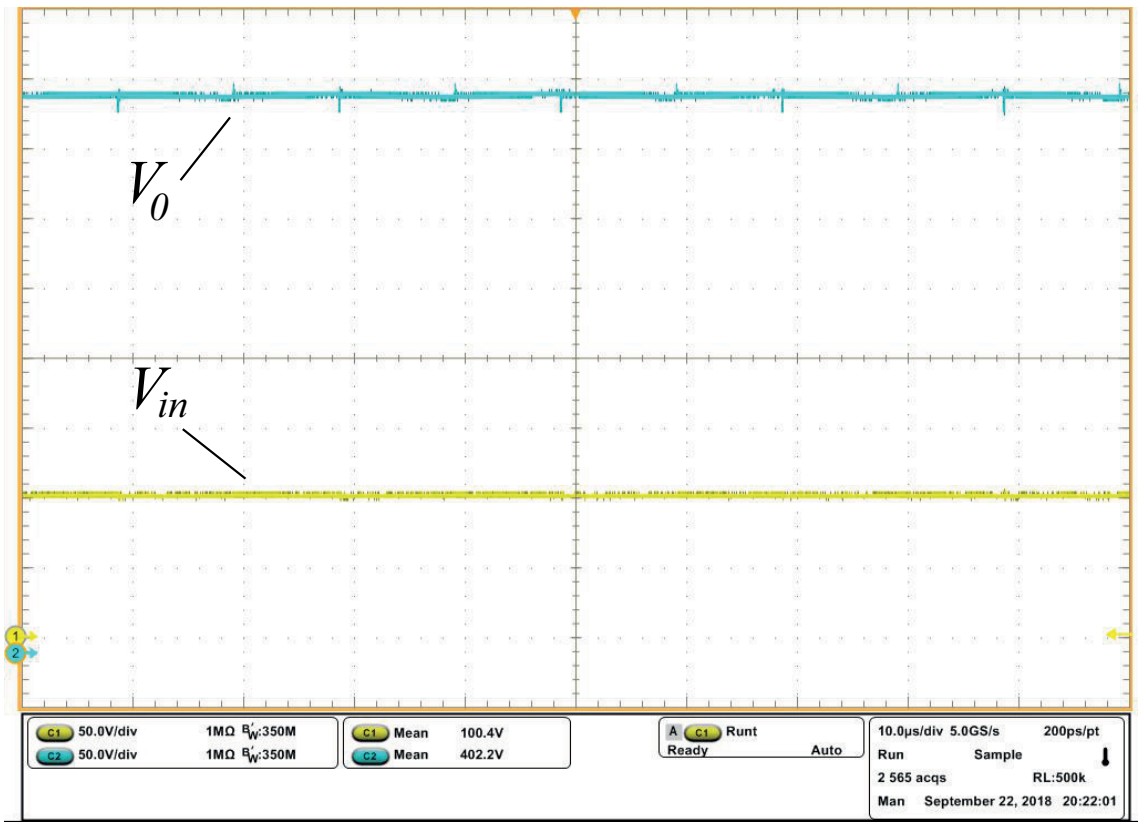


**Figure 11.** *Cont.*

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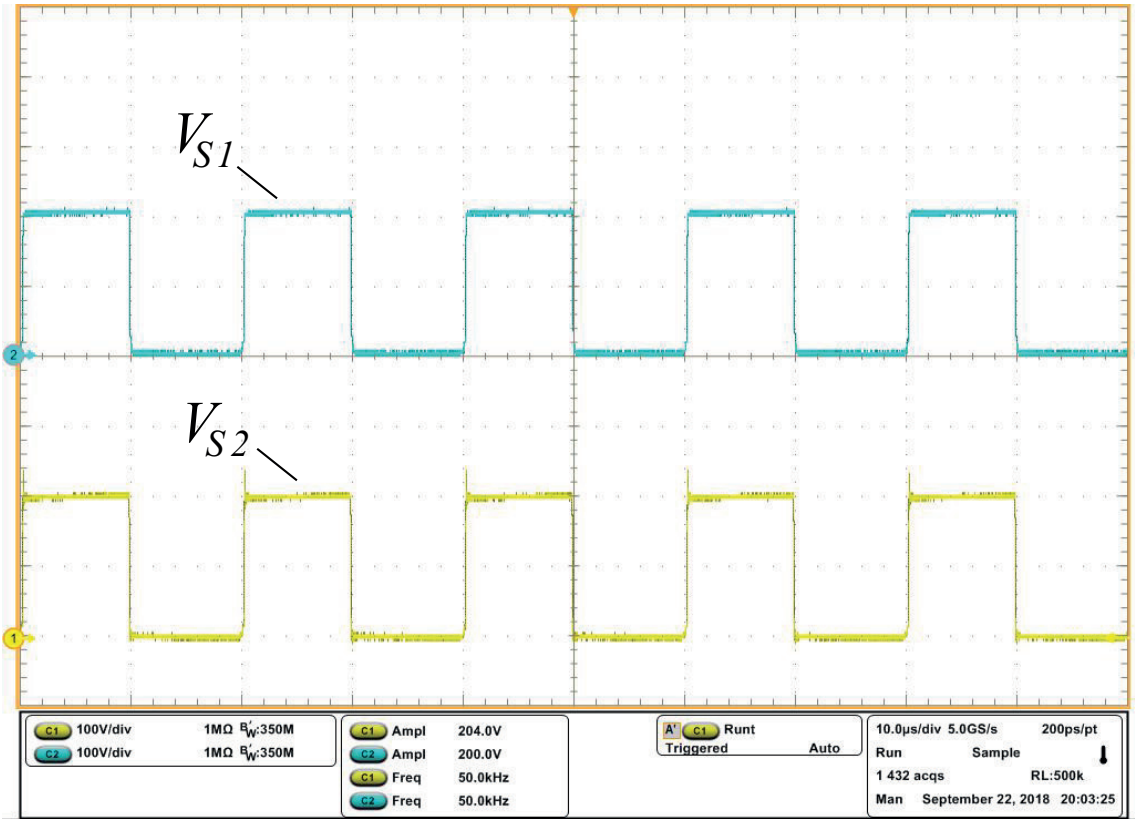


**Figure 11.** (**a**) Input voltage ($V_{in} = 100V$) and total output voltage ($V_0 = 400V$). (**b**) Voltage at switches $V_{S1}$ and $V_{S2}$, using $D = 0.5$ and a scale of $100V$ by division.

Comparing the experimental waveforms of the total output voltage $V_0$ and the input voltage $V_{in}$, it verifies the high static gain of the converter (four times for $D = 0.5$). Although the experimental results are presented only for the total output voltage $V_0$, these results can be obtained by summing the voltage of the output capacitors $V_{C01}$ and $V_{C02}$.

The current in the inductors is significant in the analysis of the converter operating mode. However, it developed the theoretical analysis for continuous, critical, and discontinuous conduction modes; the practical implementation was performed only in continuous driving mode, where these converters generally operate in most applications because of its presented lower current peaks in their semiconductors. The currents in the $L_1$ and $L_2$ inductors are shown in Figure 12. The current ripple in the $L_1$ inductor is greater than in the $L_2$ inductor as designed. The project considered a ripple of 10% in the value of their respective nominal currents.

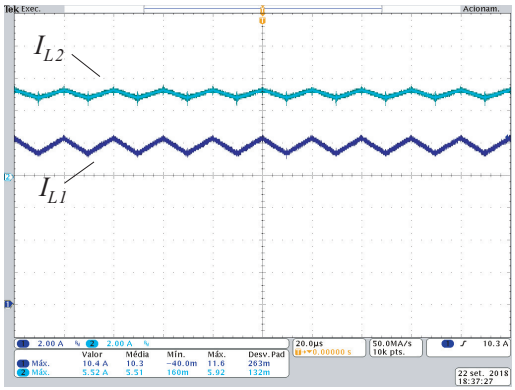


**Figure 12.** Current in inductors $I_{L_1}$ and $I_{L_2}$, in scale $2A$ per division. Average values: $I_{L1} = 10.3A$ e $I_{L2} = 5.51A$, with current ripple of 10%.

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Converter efficiency is an important parameter and must be taken into consideration. Therefore, Figure 13 presents the comparison of the converter performance obtained via simulation in PSIM, using the Device Database Editor tool through the semiconductor models specified in Table 3 and the efficiency obtained through the experimental tests, in this case, the power analyzer, Yokogawa wt500, was used. Therefore, it is seen in Figure 13, that the proposed converter has high efficiency, proven through simulation and experimental tests.

Moreover, as presented in the theoretical analysis through Equations (4) and (5), the Double Boost Quadratic converter has a high static gain. Figure 14 shows the static gain curve obtained by simulation using the Matlab software compared to the experimental curve. For the experimental tests, it was possible to vary the duty cycle $D$ ($0$ - $0.85$). This value was limited by the power at which the converter was designed and built, according to Table 3. It chose low power value, allowing for a greater range of the duty cycle.

As shown in Figure 14, the static converter gain reached the ratio of 12 times of output voltage to the input voltage, as proposed in the theoretical analysis. For the tests, limited the input inductor current $i_{L1}$ was in the function of the design current. It performed the test at 15% of the rated power of the converter.

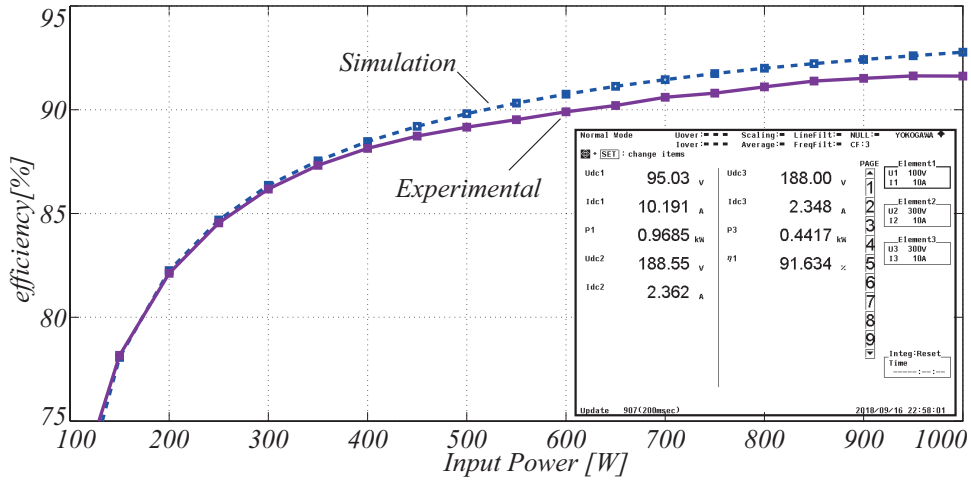


**Figure 13.** Converter efficiency: simulation result compared to the experimental result.

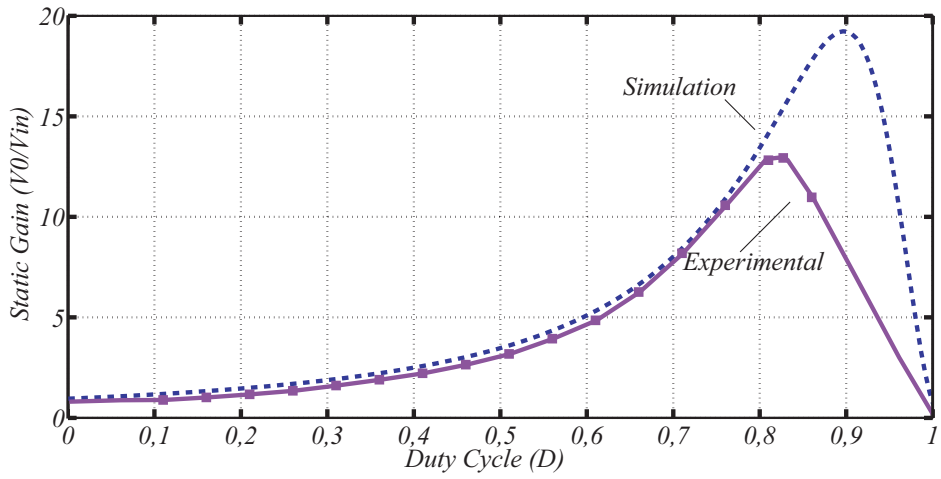


**Figure 14.** Real static gain: simulation result (dashed) compared to experimental result.

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*5.2. Converter Operating in Closed Loop*

Considering the converter operating in the closed-loop with current, voltage, and voltage balance control on the output capacitors, Figure 15 presents the input current, midpoint current, and output capacitor voltages. It develops the tests for a load step of 50% of rated power to 75% of rated power. It noticed that at the moment of load variation to the input current increase ($I_{in}$) is proportional to the power variation, as shown in Figure 15, and in this case the overshoot of one of the output capacitors is similar, but with the opposite signal, characterizing their balance control.

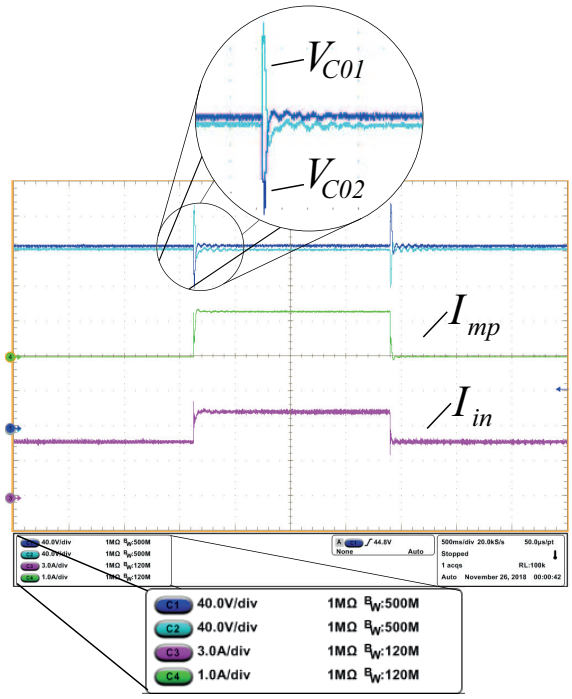


**Figure 15.** Input current $I_{in}$, midpoint current $I_{mp}$ and voltage on output capacitors $V_{C01}$ and $V_{C02}$, at times of charge variation (50%  75%).

In order to complement the load variation test shown in Figures 15 and 16a presents the same waveforms, replacing the input current with the total output voltage. In this case, despite the variation of the input current shown in Figure 15, there is no variation of the output capacitor voltage $V_{C01}$ and $V_{C02}$ just than a small overshoot at the time the load steps occurred.

In Figure 16a, it is noticed that the over voltage at the $V_0$ total voltage is lower when compared to the over voltage at the output capacitors $V_{C01}$ and $V_{C02}$, proving that the balance control can balance the voltage values in the capacitors, even with load imbalance. To keep the voltage on the output capacitors unchanged despite load imbalance, the midpoint current $I_{mp}$ is responsible for absorbing this imbalance through this current variation.

In order to introduce the operation of the converter against the imbalances in the output capacitor voltages, besides the load variation, Figure 16b presents the midpoint current, the output capacitor voltages and the total output voltage at four different times: a) In $t_1$ load imbalance ($R_{01}$); b) In $t_2$ total load disturbance (50%); c) In $t_3$ load disturbance (removal of 50% total load); d) In $t_4$ removal of load imbalance ($R_{01}$).

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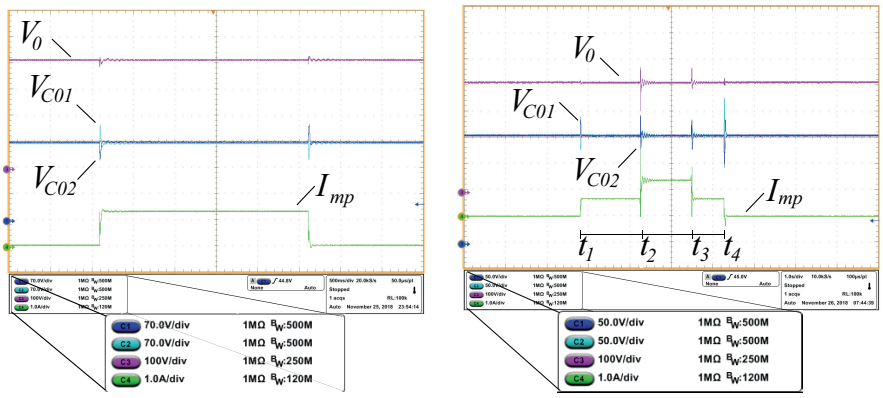


Load variation time (50% - 75%). Instants of imbalance and load variation.

**Figure 16.** Midpoint current $I_{mp}$, voltage at output capacitors $V_{C01}$, $V_{C02}$ and total output voltage $V_0$.

## 6. Discussion

It verifies that the control of the output capacitors voltage balance presents a good response in the instant of capacitors voltage unbalance and in the moment of load variation. While the output voltage remains unchanged, except for a small transient at these times, allowing compensation for this variation. Finally, the midpoint current has significantly varied at times of load imbalance, as expected in the voltage balance control of the output capacitor, because it is through the current midpoint variation that capacitors voltages are balanced.

## 7. Conclusions

Considering that energy generation is fundamental for world economic development, combined with care for the environment and sustainable practices, the generation of energy through renewable sources plays an important role. Thus, research related to applications in the field of electricity is fundamental to technological development.

Therefore, thinking about optimizing power converters for these applications, in this work was presented the study of a new non-isolated high static gain converter DC-DC. The operating stages and waveforms of the converter have been shown for continuous, critical, and discontinuous conduction mode in addition to the ideal static gain curves, actual static gain for the various load resistance values, and the curve representing the boundary between the conduction modes. For the development of the dynamic mathematical model, the state space technique was used.

Due to the symmetry of the converter, it was possible to reduce the stresses on the switches. Moreover, its symmetry also simplified its mathematical model, as presented in the paper, in which an eighth-order system can be simplified by a fourth-order system, making it easier to obtain its transfer function. In this configuration, this converter can be used, for example, in conjunction with a multi-level inverter coupled to its output for photovoltaic generation, grid-connected applications, or coupled to AC loads requiring low harmonic distortion rates.

The experimental results were presented confirming the theoretical analysis. Thus, it was possible to verify the high static gain (greater than twelve times) experimentally through the practical tests of the duty cycle variation, where the results were obtained as expected. Also, it was possible to verify the reduced voltage efforts on the converter switches when compared to existing converters in the literature. As it is an important parameter, the efficiency curve of the converter was presented in the experimental results, proving the high efficiency of the proposed converter.

Finally, the results show that this converter has a great natural potential for application in renewable energies, being this an excellent option in the conditioning of power generation through photovoltaic panels.

**Author Contributions:** Conceptualization, D.R. and S.A.; methodology, S.A.; software, F.L.; validation, F.L.; formal analysis, F.L.; investigation, F.L. and C.D.; resources, F.L. and C.D.; data curation, F.L.; writing original draft

preparation, F.L. and C.D.; writing review and editing, F.L. and W.S.; visualization, F.L. and W.S.; supervision, S.A.; project administration, S.A. All authors have read and agreed to the published version of the manuscript.

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