



Article

A Comparison Study of Time-Domain Computation Methods for Piecewise Smooth Fractional-Order Circuit Systems

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Abstract: The role of fractional calculus in circuit systems has received increased attention in recent years. In order to evaluate the effectiveness of time-domain calculation methods in the analysis of fractional-order piecewise smooth circuit systems, an experimental prototype is developed and the effects of three typical calculation methods in different test scenarios are compared and studied in this paper. It is proved that Oustaloup's rational approximation method usually overestimates the peak-to-peak current and brings in pulse-voltage phenomenon in piecewise smooth test scenarios, while the results of two iterative recurrence-form numerical methods are in good agreement with the experimental results. The study results are dedicated to provide a reference for efficiently deploying calculation methods in fractional-order piecewise smooth circuit systems. Some quantitative analysis results are concluded in this paper.

Keywords: Fractional calculus; piece-wise smooth circuit systems; calculation methods

0. Introduction

In recent decades, the concepts of fractional calculus and the related techniques have been gaining momentum in circuit system fields [1–3]. It has been confirmed that, exploring the potential fractional-order characteristics of electronic components is helpful for both the condition monitoring of components and the reliability design of circuit systems [7–11]. An increasing body of evidence suggests that fractional-order characteristic is widely distributed in electronic components [4–6], such as ultracapacitors (UCs), lithium batteries, and non-solid electrolytic capacitors. Moreover, introducing fractional-order elements (or constant phase elements, CPEs) to traditional circuit and control systems can enhance the design flexibility [12–14].

In order to better describe the characteristics of circuit systems with fractional-order components, it is of necessity to develop a set of reliable calculation and analysis methods. Basically, the lumped parameter model with fractional-order differential equations is a well-established approach to quantify the characteristics of fractional-order circuit systems, and a number of calculation and analysis works have been proposed for such systems, definition-based methods [15], rational approximation methods [16–18], and numerical methods [19–21], to name but a few. The methods listed above have been applied to the modeling and analysis of a wide variety of fractional-order circuit systems [22–24].

However, to the best of the authors' knowledge, most existing calculation and analysis methods are applied only to continuous fractional-order circuit systems, but rarely to piecewise smooth ones [25–27]. In practice, the piecewise-smooth characteristic is common in circuit systems, especially for those with semiconductor switching devices, and such characteristic may bring in effects on the accuracy of numerical methods. Therefore, it is worthwhile to compare and evaluate the effectiveness of existing methods in analyzing piecewise smooth fractional-order systems.

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In allusion to state-of-the-art, this work tries to unfold the applicability of three typical calculation methods for piecewise smooth fractional-order circuit systems. The rest of the work is organized as follows: test scenarios are established in Section 1, in which a non-solid aluminum electrolytic capacitor is employed in the test bench, since this kind of components have been confirmed to have frequency-related fractional-order characteristics in a wide frequency band [6]. Section III deduces the solutions of the test scenarios by different approaches. Section IV compares and discusses the results of different approaches, while section V concludes the work.

1. Test Bench Settings and Mathematical Model

1.1. Test Bench Settings

In a previous work, it has been confirm that, the electrode surface in the capacitor has an infinite self-similar structure, and the particle distribution law in it has a long-tail effect under the electric field, which is suitable to be described by the fractional equivalent impedance model [6]. The internal structure and fractional-order equivalent impedance circuit in Figure 1:

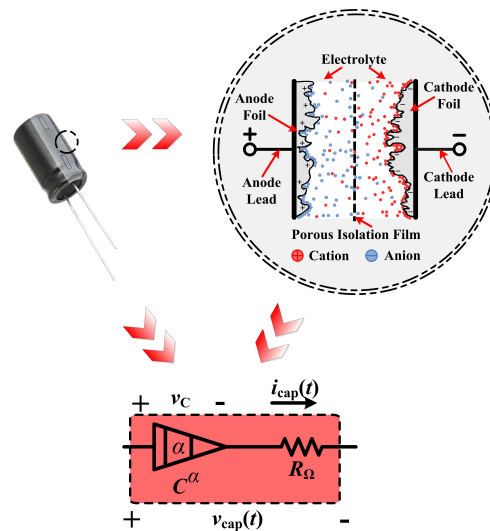


Figure 1. Internal structure and fractional-order equivalent impedance circuit model of non-solid aluminum electrolytic capacitors.

In the above figure, the symbol C is the nominal capacitance of the capacitor, while the symbol α is an estimated fractional order of 0 to 1, and the symbol R_Ω is the equivalent series resistance of the capacitor. Then, a test bench is established in this section, which contains such a capacitor. The schematic of this test bench is displayed is depicted in Figure 2.

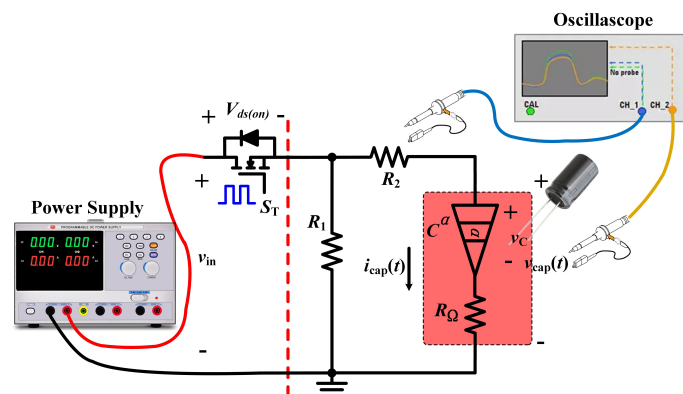


Figure 2. Schematic of the test bench.

The design of the test bench refers to the previous work [28], in which a type GPS-3303C 3-channel isolated dc power supply is adopted to provide power, and an oscilloscope is employed to record the data. In the platform, a type STP80NF70 power MOSFET S_T is adopted, the gate-source voltage of which is controlled by a driving circuit. As a result, the test bench will work in charging and discharging cycle working mode, so the circuit can be deemed as a piecewise smooth circuit system. On the right side of the red dash line in Figure 3, the resistor $R_1 = 5\Omega$ provides a discharging path for the capacitor, while $R_2 = 10\Omega$ is mainly used as the current sensing and limiting resistor. The circuit in the box with red background is the fractional-order equivalent circuit of a $10\mu F$ Rubycon PX series non-solid aluminum electrolytic capacitor. The voltage and the current of the capacitor are $v_{cap}(t)$ and $i_{cap}(t)$, respectively, and two probes of the oscilloscope are used to observe them. In addition, the voltage of the equivalent CPE is assumed to be $v_c(t)$. A glimpse of the experimental scene is as Figure 3.

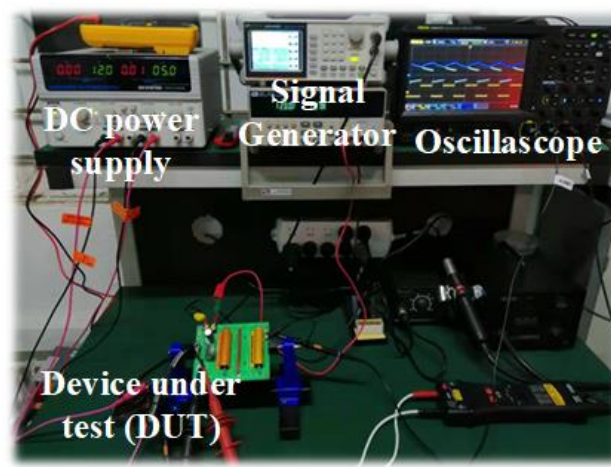


Figure 3. A glimpse of the experimental scene.

1.2. Mathematical Model

The test platform can be regarded as a charge-discharge circuit for the non-solid aluminum electrolytic capacitor. One can find that, there is only one energy-storage component in the platform, so the interferences and errors are minimized compared with the schemes with rational approximation methods or those with magnetic elements. In the following parts, the test platform will be operated in two test scenarios to verify the applicability of different calculation and analysis methods.

According to the fractional-order equivalent impedance circuit of the capacitor in Figure 1, the current $i_{cap}(t)$ and the voltage $v_{cap}(t)$ of the capacitor satisfy the following relationships,

$$\begin{cases} i_{cap}(t) = C \cdot \frac{d^\alpha v_c(t)}{dt^\alpha} \\ v_{cap}(t) = v_c(t) + R_\Omega \cdot C \cdot \frac{d^\alpha v_c(t)}{dt^\alpha}, \end{cases} \quad (1)$$

It is noteworthy that the nominal capacitance C is $10\mu F$ in this work, while R_Ω and the fractional order α relate to the fractional-order characteristics of the capacitor can be identified by using the method proposed in a previous work [6], and in this work, their values are 0.8852, 1.2629Ω , respectively.

In order to validate different methods, we established two groups of test scenarios, the basic and the advanced. In basic test group, we consider two operating modes, the first one is sinusoidal mode, where the power supply is a single phase AC power supply with a pre-determined frequency. The second one is step mode, where a DC power supply

is employed as the source and the power MOSFET S_T is turned on at time $t = 0$ with a constant forward voltage drop $V_{ds(on)} = 0.7V$.

- The state of the sinusoidal mode can be governed by:

$$v_c(t) + (R_2 + R_\Omega) \cdot C \cdot \frac{d^\alpha v_c(t)}{dt^\alpha} = v_{in}(t) - V_{ds(on)}, \quad (2)$$

where $v_{in}(t) = K \cdot \sin(\omega t)$ is a sinusoidal function. K is the predetermined magnitude of the signal, $\omega = 2\pi f_s$ is the angular frequency, and f_s is the frequency of the sinusoidal function.

- The state of the step mode can be governed by:

$$v_c(t) + (R_2 + R_\Omega) \cdot C \cdot \frac{d^\alpha v_c(t)}{dt^\alpha} = V_{in} - V_{ds(on)}, \quad (3)$$

in which V_{in} is a predetermined constant value.

In the first group of test scenarios, the test bench works under continuous mode or step response mode. This group are used to assess the feasibility of different calculation methods.

In the second group of test scenario, the power MOSFET S_T is controlled by a periodic square waveform with a duty ratio $D = 0.5$ and a variable frequency f_s from 100Hz to 1kHz. The performances of the circuit under test in one steady-state cycle T_s can be governed by:

- Charge performance in $t \in [kT_s, kT_s + DT_s]$ is:

$$v_{cap}(t) = V_{in} - V_{ds(on)} - R_2 \cdot i_{cap}(t), \quad (4)$$

where k is the k -th switching cycle, T_s is the switching period, and

$$\begin{aligned} V_{in} - V_{ds(on)} &= v_{cap}(t) + R_2 \cdot i_{cap}(t) \\ &= v_c(t) + (R_2 + R_\Omega) \cdot C \cdot \frac{d^\alpha v_c(t)}{dt^\alpha}. \end{aligned} \quad (5)$$

- Discharge performance in $t \in [kT_s + DT_s, (k+1)T_s]$ is:

$$v_{cap}(t) = -(R_1 + R_2) \cdot i_{cap}(t), \quad (6)$$

and

$$\begin{aligned} 0 &= v_{cap}(t) + (R_1 + R_2) \cdot i_{cap}(t) \\ &= v_c(t) + (R_1 + R_2 + R_\Omega) \cdot C \cdot \frac{d^\alpha v_c(t)}{dt^\alpha}. \end{aligned} \quad (7)$$

In the second group of test scenarios, the capacitor of the test bench will be charged and discharged cycle by cycle, thus the circuit under test is a typical piecewise smooth circuit system.

One can find that, to reveal the time-domain performances of these two scenarios, the voltage v_c should be calculated. However, this voltage is an equivalent quantity of the CPE, thus one cannot probe it directly and has to solve fractional-order differential equations 2 to 7, which are all fractional-order differential equations with constant coefficients. Rewrite these equations to the following generalized form:

$$a_{1i} \cdot \frac{d^\alpha x}{dt^\alpha} + a_{0i} \cdot x = u_i, \quad (8)$$

where $i = 1, 2, 3, 4$, $x = v_C$ is the only state variable of the circuit, and the coefficients are: $a_{11} = a_{12} = a_{13} = (R_2 + R_\Omega)C$, $a_{14} = (R_1 + R_2 + R_\Omega)C$, $a_{01} = a_{02} = a_{03} = a_{04} = 1$, $u_1 = K \cdot \sin(\omega t) - V_{ds(on)}$, $u_2 = u_3 = V_{in} - V_{ds(on)}$, and $u_4 = 0$.

All the coefficients are predetermined in their own time intervals. Meanwhile, the initial conditions of Equation 8 are continuous in their own domains of definition, hence according to theorem 3.2 of literature [29], fractional-order differential Equation 8 have uniqueness solutions. At this time, the initial values problem of fractional-order differential equations arises.

2. Computation Approaches

In this section, the principles of some related techniques are introduced first. Then three different approaches will be applied to calculate equations 2 to 7, and the results will be adopted for validation and comparison. The first calculation method is a numerical calculation method, that is the fractional Adams-Bashforth-Moulton typed method (F-ABM) [21]. The second calculation method is based on Grünwald-Letnikov (G-L) definition [15]. To obtain solutions by using the first and the second methods, the stroboscopic map technique should be applied [30]. The third calculation method is Oustaloup's rational approximation method [16], which will be conducted by using the state-space averaging (SSA) technique [31].

2.1. Preliminaries: Principles of Some Related Techniques

2.1.1. Stroboscopic map technique

One can always apply most calculation approaches to calculate fractional-order differential equations in continuous cases directly. But in discontinuous cases, or the piecewise smooth case discussed in this work, one may have to face a different situation. For example, the sign function of $f(x) = \text{sign}(x)$, which has the value of 1 for all $x > 0$ and the value of -1 for all $x < 0$.

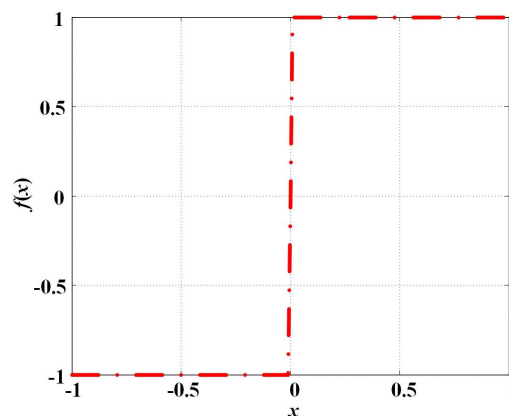


Figure 4. A graph of typical $\text{sign}(x)$ function.

The sign function of $f(x) = \text{sign}(x)$ appears in a variety of piecewise smooth fractional systems, which creates the initial value problem at the discontinuous point $x = 0$, and one needs physically interpret initial conditions at this point.

In the step mode of the basic test scenario, the proposed test bench also experiences a similar situation like the sign function. In addition, in the advanced test scenario, the the capacitor experiences a recurrence of charging and discharging behaviors in each switching cycle, thus the test bench will be in continuous state switching. Along with the on- and off operations of the power MOSFET S_T , there are a set of discontinuous points. Accordingly, a technique called stroboscopic map should be employed in both analytical and numerical calculations. This technique has been widely adopted in the dynamic analysis of piecewise-smooth systems and switching power converters. By this technique, the dynamic behavior of the test circuit at each switching state S_n will be collected in one switching cycle, that

is, the solution x_n of the previous switching state at time t_n will be employed as the initial value of the next switching state, thus a cycle-by-cycle calculation can be carried out. The principle of is stroboscopic map technique depicted in Figure 5.

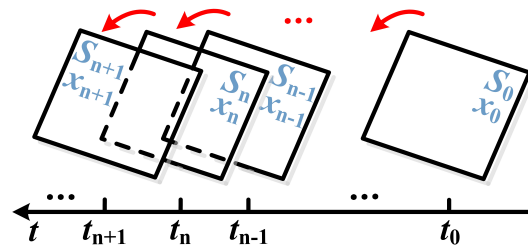


Figure 5. Principle of stroboscopic map technique.

2.1.2. State-space averaging (SSA) technique

In practice, some methods are difficult to be directly used in the advanced test scenario of this work. In allusion to this, the SSA technique can be exploited, by which the steady-state characteristic analysis can be achieved. By this technology, the average value of $v_c(t)$ in one switching cycle can be expressed by:

$$\langle v_c \rangle_{T_s} = \frac{1}{T_s} \int_{t_0}^{t_0+T_s} v_c(t) dt \quad (9)$$

Accordingly, in steady-state, when the low-frequency hypothesis and the small ripple hypothesis are satisfied, the test platform in discontinuous case can be governed by the following SSA model:

$$\begin{aligned} (R_2 + R_\Omega) \cdot C \cdot \frac{d^\alpha \langle v_c \rangle_{T_s}}{dt^\alpha} + \langle v_c \rangle_{T_s} \\ + [1 - d(t)] \cdot R_1 \cdot C \cdot \frac{d^\alpha \langle v_c \rangle_{T_s}}{dt^\alpha} = d(t) [V_{in} - V_{ds(on)}], \end{aligned} \quad (10)$$

in which the terms $\langle v_c \rangle_{T_s}$ and $d(t)$ can be decomposed into DC terms V_c and D , AC terms \hat{v}_c and \hat{d} like follows:

$$\begin{cases} \langle v_c \rangle_{T_s} = V_c + \hat{v}_c \\ d(t) = D + \hat{d} \end{cases} \quad (11)$$

2.2. Solutions of the Test Bench

2.2.1. Solutions obtained by G-L definition

According to G-L definition, the fractional-order derivative of state variable $x(t)$ can be written in the following discrete form [15]:

$$\begin{aligned} \frac{d^\alpha x(t)}{dt^\alpha} &\approx \frac{1}{h^\alpha} \sum_{j=0}^{t/h} p_j^\alpha x_{t-jh} \\ &= \frac{1}{h^\alpha} \left[x_t + \sum_{j=1}^{t/h} p_j^\alpha x_{t-jh} \right], \end{aligned} \quad (12)$$

where h is the predetermined discrete step size and p_j^α can be deduced by

$$p_0^\alpha = 1, p_j^\alpha = \left(1 - \frac{1+\alpha}{j}\right) p_{j-1}^\alpha. \quad (13)$$

Introducing Equation 13 into Equation 12 leads to the following recurrence form solution:

$$x_t = \frac{1}{a_{1i} + h^\alpha a_{0i}} \left[h^\alpha u_{i,t} - \sum_{j=1}^{t/h} p_j^\alpha x_{t-jh} \right]. \quad (14)$$

Then one can obtain G-L based solutions of Equation 8 by point-by-point iteration of Equation 14. In addition, the numerical solutions of charging and discharging state in the advanced test scenario will be collected in each switching cycle by the aforementioned stroboscopic map technique.

2.2.2. Solutions obtained by F-ABM method

In case of $-1 \leq \alpha \leq 1$, according to the definition of F-ABM method [19], the initial value problem of the fractional-order system of Equation 8 can be determined by:

$$x(n+1) = x(0) + \frac{h^\alpha}{\Gamma(2+\alpha)} f[t_{n+1}, x^P(n+1)] + \frac{h^\alpha}{\Gamma(2+\alpha)} \sum_{j=0}^n A_{j,n+1} f[t_j, x(j)], \quad (15)$$

where the term n is any integer and $A_{j,n+1}$ is

$$A_{j,n+1} = \begin{cases} = n^{\alpha+1} - (n-\alpha)(n+1)^\alpha, & j=0 \\ = (n-j+2)^{\alpha+1} + (n-j)^{\alpha+1} \\ - 2(n-j+1)^{\alpha+1}, & 1 \leq j \leq n \\ = 1, & j=n+1 \end{cases} \quad (16)$$

The predictor $x^P(n+1)$ in Equation 15 is

$$x^P(n+1) = x_0 + \frac{1}{\Gamma(\alpha)} \sum_{j=0}^n B_{j,n+1} f[t_j, x(j)], \quad (17)$$

in which the term $B_{j,n+1}$ is

$$B_{j,n+1} = \frac{h^\alpha}{\alpha} \left[(n+1-j)^\alpha - (n-j)^\alpha \right]. \quad (18)$$

Then the numerical solutions of Equation 8 can be obtained by Equation 15. Additionally, the numerical solutions of charging and discharging state in the advanced test scenario will be collected in each switching cycle by the aforementioned stroboscopic map technique.

2.2.3. Solutions obtained by Oustaloup's rational approximation method

By Oustaloup's rational approximation method, a continuous filter can be designed in frequency domain to achieve fractional-order calculus operations approximately. More specifically, by Laplace transform, the fractional-order operation $\frac{d^\alpha}{dt^\alpha}$ can be transformed to an s-domain term s^α , then the frequency domain characteristics of s^α can be approximated in the pre-defined frequency interval $[\omega_L, \omega_H]$ by an s-domain rational fraction function

$$\frac{d^\alpha}{dt^\alpha} \Rightarrow K \prod_{i=-n}^n \frac{s+z_i}{s+p_i}, \quad (19)$$

where the gain K , zeros z_i , and poles p_i are

$$\begin{cases} K = (0.9 \cdot \omega_H)^\alpha \\ z_i = -\omega_L \cdot \mu^{((i+N+0.5-0.5\cdot\alpha)/(2\cdot N+1))} \\ p_i = -\omega_L \cdot \mu^{((k+N+0.5+0.5\cdot\alpha)/(2\cdot N+1))}, \end{cases} \quad (20)$$

respectively. The coefficient μ is

$$\mu = \frac{\omega_H}{\omega_L}. \quad (21)$$

Then the numerical solutions of Equation 8 can be obtained by encapsulating Equation 19 to a module in MATLAB/Simulink, like those introduced in literature [16–18]. In addition, the Equation 10 of SSA technique should be applied. The block diagrams of the basic test scenario and the advanced test scenario are provided in Figure 6, where the block $s^{-\alpha}$ with red background is encapsulated according to equation 18.

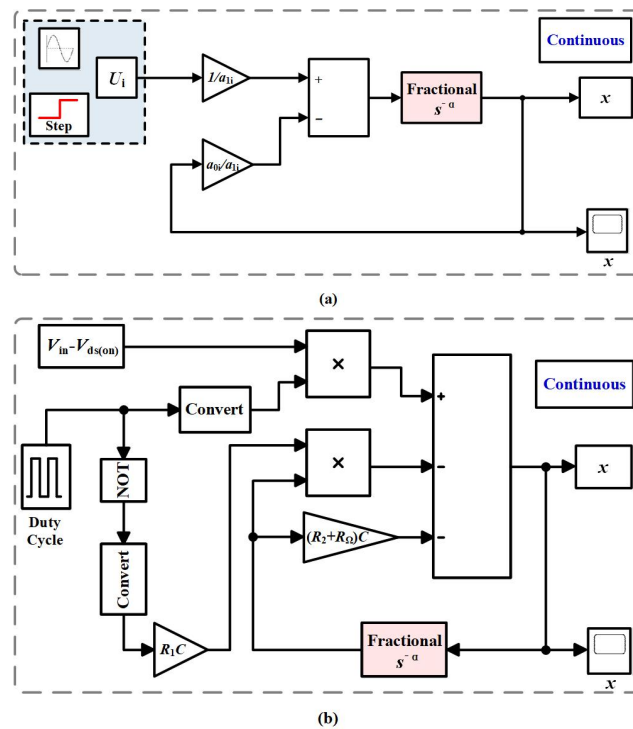


Figure 6. Principle block diagrams: (a) Basic test scenario, (b) Advanced test scenario.

3. Results Comparison and Evaluation

According to the scenario settings and the related derivation, comparative works are carried out in this section, numerical results are obtained by F-ABM method, G-L definition, and Oustaloup's method and are collected in groups. In addition, experiment waveforms are provided as reference.

3.1. Results of Calculation and Simulation

The first group of results are from the basic test scenario, by using the aforementioned three approaches, one can obtain numerical simulation results, as depicted in Figure 7. The second group of results are from the advanced test scenario, simulation results are as Figure 8, In both cases, the blue solid line represents the voltage of power supply, while the red dash-and-dot line corresponds to the results of Oustaloup's rational approximation method, the black dash line corresponds to the results of G-L definition, and the green solid line corresponds to the results of the F-ABM method.

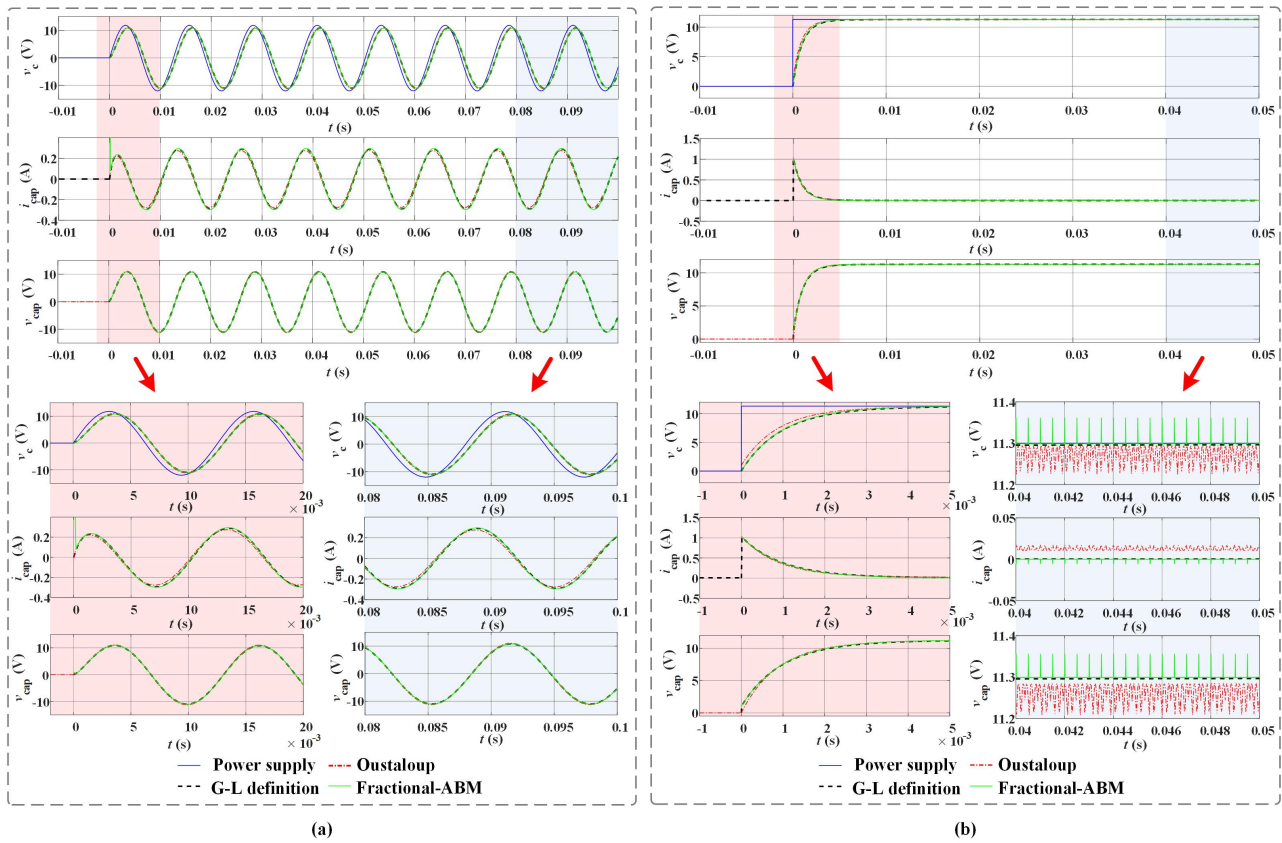


Figure 7. Comparison of basic test scenarios: (a) sinusoidal case, (b) step case.

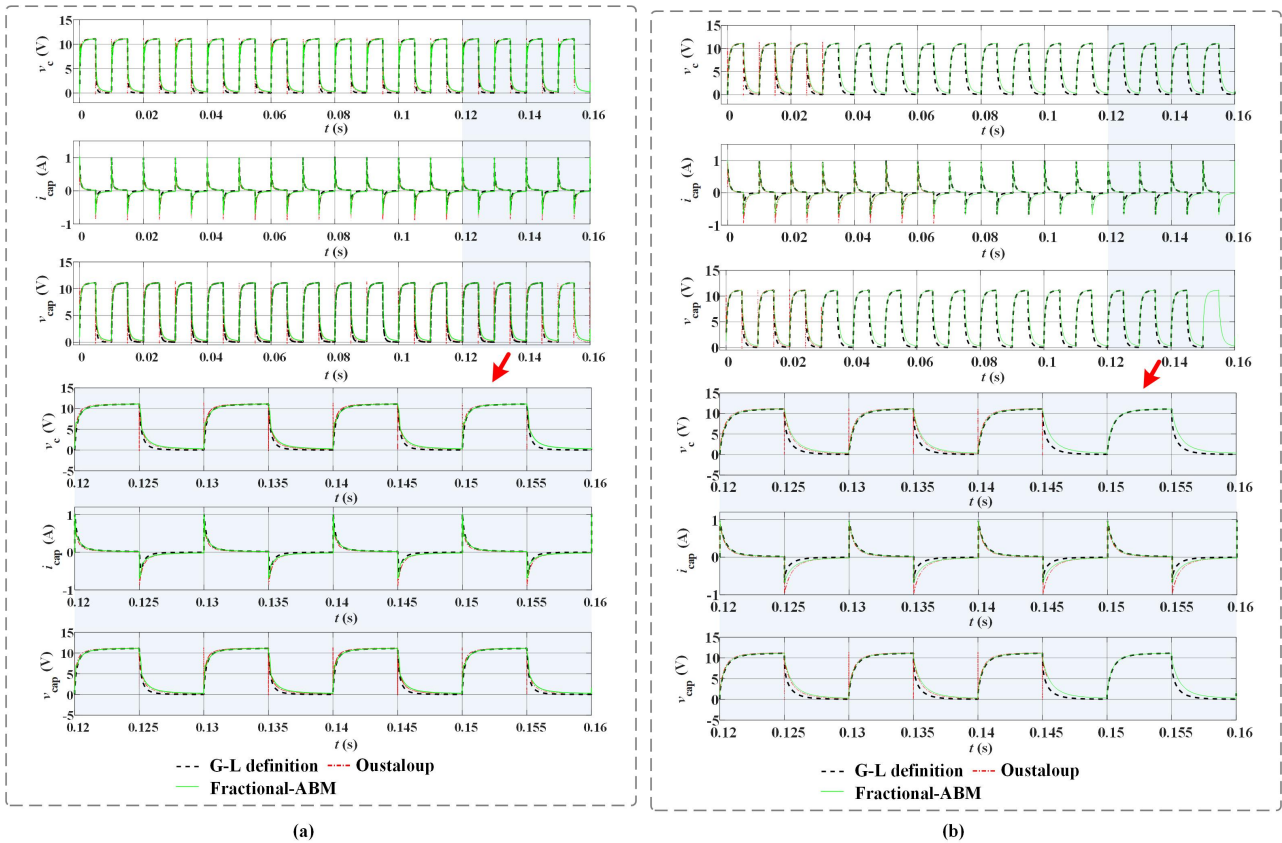


Figure 8. Comparison of advanced test scenarios: (a) advanced scenario with $f_s = 100\text{Hz}$, (b) advanced scenario with $f_s = 200\text{Hz}$.

In the above two figures, the sub-graphs with red and blue backgrounds refer to the enlarged parts.

In sinusoidal case, It can be seen that, the results of three methods mesh well with each other in steady-state. There is a lag of around $0.5ms$ between the voltage $v_c(t)$ and the voltage of power supply, which is determined by the capacitance $C = 10\mu F$ and the fractional order $\alpha = 0.8852$ of the equivalent impedance model of the capacitor.

In step case, it can be seen that at the discontinuous point, the peak currents obtained by three methods are almost the same, the value is around $1.0395A$. But note that, the results obtained by three methods are slightly different at steady state. In specific, the steady-state voltage calculated by Oustaloup's method is about $0.1V$ lower than the results obtained by G-L definition and F-ABM method. In addition, the steady-state current calculated by Oustaloup's method is about $0.01A$ higher than the results obtained by G-L definition and F-ABM method.

In advanced test scenarios, it can be seen that, the results of three methods mesh well with each other. But note that, there are spikes of the voltages $v_c(t)$ and $v_{cap}(t)$ at discontinuous points if one uses Oustaloup's method. With the acceleration frequency f_s of charge-discharge state transition, this spike phenomenon becomes obvious. In addition, the steady-state current $i_{cap}(t)$ and the voltage $v_{cap}(t)$ calculated by the three methods are slightly different. With the acceleration frequency f_s of charge-discharge state transition, this difference becomes obvious.

3.2. Evaluation and discussion

In order to further validate the calculation results, experiment waveforms are provided in Figure 9 and Figure 10.

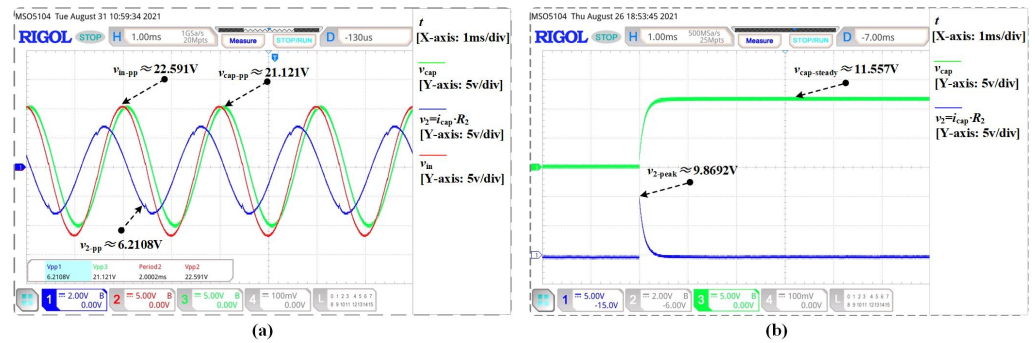


Figure 9. Experiment results of basic test scenarios: (a) sinusoidal case, (b) step case.

In Figure 9, the blue solid lines are the voltage $v_2(t)$ of the resistor R_2 . It can be regarded as the sampling for the current $i_{cap}(t)$ flowing through the capacitor. The red solid lines correspond to the voltage of power supply, the green solid line corresponds to the voltage $v_{cap}(t)$ of the capacitor.

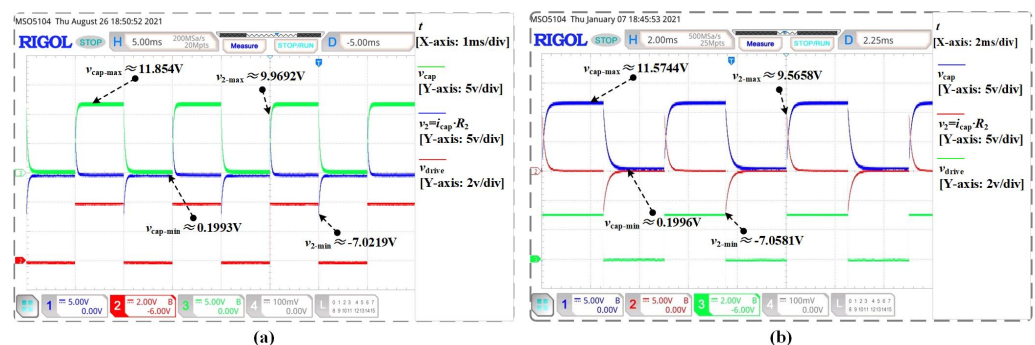


Figure 10. Experiment results of advanced test scenarios: (a) advanced scenario with $f_s = 100Hz$, (b) advanced scenario with $f_s = 200Hz$.

It can be found that experimental waveforms are very similar to the theoretical calculation and simulation results. In order to assess the results of calculation, statistical analysis was used to qualify different methods.

First of all, we compare the spike current i_{spike} , the averaged steady-state capacitor voltage \bar{v}_{cap} , and the averaged steady-state capacitor current \bar{i}_{cap} in step case in Table 1.

Table 1. Comparison of the spike current i_{spike} , the averaged steady-state capacitor voltage \bar{v}_{cap} , and the averaged steady-state capacitor current \bar{i}_{cap} in step case.

	\bar{v}_{cap}	\bar{i}_{cap}	i_{spike}
G-L definition	11.2894V	$\approx 1.29mA$	1.0012A
F-ABM	11.3025V	$\approx -0.2mA$	1.0308A
Oustaloup's	11.2816V	0.0110A	1.0379A
Experiments	11.5570V	$\approx 1mA$	0.9869A

From Table 1, it can be seen that the most calculation results of three methods have little deviation from experimental results in step case. However, compared with other results, the averaged current \bar{i}_{cap} obtained by Oustaloup's method is too large. This current value is unreasonable, because in both theory and practice, if the electric field applied to the capacitor is constant, the current of the capacitor should be in a trickle state.

Then, we compare the calculations results in sinusoidal case and advanced scenarios, and list the peak-to-peak values obtained by different ways in Table 2.

Table 2. Comparison of peak-to-peak values of capacitor voltage v_{cpp} and current i_{cpp} .

	In sinusoidal case	In advanced scenario with $f_s = 100Hz$	In advanced scenario with $f_s = 200Hz$
G-L definition	(0.5851A, 21.9082V)	(1.6848A, 11.0712V)	(1.6656A, 10.6078V)
F-ABM	(0.5908A, 21.9414V)	(1.6853A, 10.7952V)	(1.6686A, 10.0280V)
Oustaloup's	(0.5514A, 22.3235V)	(1.9266A, 11.6760V)	(1.9088A, 12.2848V)
Experiments	(0.6211A, 21.1210V)	(1.6991A, 11.6547V)	(1.6624A, 11.3748V)

From Table 2, it can be seen that the calculation results of three methods have little deviation from experimental results in sinusoidal case, it means that three methods are applicable for continuous situations.

However, compared with other results, the peak-to-peak current i_{pp} obtained by Oustaloup's method is larger in advanced scenarios. In addition, one can observe pulse voltage signals at some edge time points in the simulation results obtained by Oustaloup's method, which cannot be observed in both experiments and the results of other two methods. In principle, this pulse voltage phenomenon mainly occur at on- and off operation edges of the power MOSFET S_T . At these time points, the test circuit switches between charging and discharging states, just like the high-level and low-level signals of the sign function in Figure 6 undergo periodic switching. As a result, the state equation of the test circuit switches between Equation 5 and Equation 7, and the test bench is a typical piecewise smooth circuit system.

Basically, the expressions of most frequency-domain rational approximation methods are the approximation of the amplitude-frequency or phase-frequency characteristics of ideal fractional calculus operators in a predetermined frequency band, and usually considering the situation of continuously differentiable. However, at the boundary points of piecewise smooth scenarios, the state equation of the test bench is discontinuous and non-derivable. Therefore, the approximation results of rational approximation method are not that effective. This pulse-voltage phenomena can also be explained by the Fourier transform of a step function.

4. Conclusions

This paper compares the effectiveness of G-L definition based method, F-ABM method, and Oustaloup’s rational approximation method for fractional-order piecewise smooth circuit systems. A test platform for verification is developed, in which a fractional-order component, a non-solid electrolytic capacitor, is adopted. The test platform can be operated under basic and advanced test scenarios. The basic scenario contains a continuous sinusoidal case and a step case, while the advanced scenario is the periodic charging and discharging operation of the capacitor.

Three computational methods work well in basic test scenarios, especially in sinusoidal case, which indicates that these methods are effective in continuous situations. However, in step case, the averaged current obtained by Oustaloup’s method is too large. In advanced scenarios, the waveforms obtained by three methods are similar to experimental results. Two iterative numerical calculation methods, G-L definition method and F-ABM method, perform well in $f_s = 100\text{Hz}$ and $f_s = 200\text{Hz}$ advanced scenarios, the deviation between their calculation results and the experimental results is small. However, applying Oustaloup’s method in advanced scenarios leads to large calculation deviations. Moreover, if one employs Oustaloup’s method in advanced scenarios, there is pulse-voltage phenomenon when the circuit changes from charging state to discharging state, which cannot be observed in both experiments and the results of two iterative numerical calculation methods. The comparison and experimental verification results show that, G-L definition based method and F-ABM method are effective for fractional-order piecewise smooth circuit systems. The results provided by this research will provide more confidence for understanding the dynamics of real-world systems governed by fractional calculus.

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