Article

Near infrared efficiency enhancement of Silicon photodiodes by integration of metal nanostructures supporting surface plasmon polaritrons

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Abstract: Recently, the interest in silicon-based detectors capable of detecting single photons in the near-infrared is growing mainly due to LiDAR applications, autonomous driving in particular. Silicon single-photon avalanche diodes are one of the most interesting single-photon NIR technology available on the market, nevertheless, their efficiency is hindered by the low absorption coefficient of Si in the NIR. The idea is the integration of CMOS-compatible nanostructures, specifically, silver grating array supporting Surface Plasmons Polaritons (SPPs), to confine superficially the incoming NIR photons and therefore increase photons probability to generate an electron-hole pair. The plasmonic silver array is geometrically fine-tuned using time domain simulation software to achieve maximum detector performance at 950 nm. Then, the plasmonic silver array is integrated by means of the focused ion beam technique on the detector. Finally, the integrated detector is electro-optically characterized, demonstrating a quantum efficiency of 13 % at 950 nm, 2, 2 times more than the reference detector. This result suggests the production of a device capable of detecting single NIR photons, at a very low cost and compatible with CMOS, thus integrable on existing technology platforms.

Keywords: plasmonics; plasmonics photodetector; focused ion beam; silicon photodiode; near-infrared; LiDar.)

1. Introduction

Silicon-based photodetectors appeal of interest due to their convenient manufacturing cost, high efficiency, and complementary metal–oxide–semiconductor (CMOS) process compatibility, finding applications in many research and commercial fields. At the same time, near-infrared (NIR) wavelength is becoming more important, in many emerging applications such as quantum distribution key [1], time-correlated single photon counting [2,3] and light detection and ranging (LiDAR) with the well know autonomous driving [4]. Usually, in LiDAR applications a NIR laser is used as an output device to investigate the surrounding environment, with a characteristic wavelength in the range (900 - 1000) nm. The choice of wavelength is typically selected considering some constraints like human safety and the sun's background light filtration.
In addition, most of these applications are moving towards detectors that can provide single-photon resolution, leading to a growing demand for silicon-based single-photon avalanche diodes (SPADs) and Silicon Photomultipliers (SiPMs). SPADs are devices designed to operate above their avalanche breakdown voltage in the Geiger mode, where a single photon can be converted into a quantifiable electrical signal thanks to the avalanche generated via a phenomenon called impact ionization. Moreover, silicon-based SPADs rely on well-developed and known silicon technologies which lead to a lower fabrication cost.

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Other promising SPADs are based on III-V materials presenting a high photon detection but higher design and fabrication costs.

For design reasons, SPADs and SiPMs are typically fabricated on epitaxial substrates, with active thicknesses typically in the range of a few microns. Because of the low absorption coefficient of Si in the NIR, typically the Si SPAD and SiPM have a PDE of only a few percentage points in the NIR. The scientific community tried to solve the problem by using larger silicon thicknesses (around 10 µm). This resulted in PDE of 10 % at 950 nm [5], although this poses problems with design of SiPM and SPAD with small cells (less than 25 µm), and performance in terms of single photon temporal resolution.

Recently, other approaches have been proposed by the scientific community: i) light trapping (by means of nanotexturing) [6]; ii) integration with photonic structures (metalenses or metasurfaces) [7], or iii) integration with metal nanostructures supporting plasmonic resonances, [8]. Among the others, a proposed solution is the integration of thin photodetectors with a nanostructure supporting Surface Plasmon Polaritons (SPP) able to provide light confinement and a subsequent enhancement of the light absorption in subwavelength regions. In the last twenty years, many theoretical and experimental studies have explored the attractive optical properties of photonic and plasmonic nanostructures [9–12], especially in terms of light confinement for their advanced sensing.

The SPP integration solution shows a twofold advantage:: i) overcoming the technical issues introduced by the thickening of the device, ii) confining of incident photons and consequent increase in the light absorption.

The idea is the integration of CMOS-compatible nanostructures, specifically, metallic grating nanostructures supporting Surface Plasmons Polaritons (SPPs), to confine superficially the incoming NIR photons and therefore increase photons probability to generate an electron-hole pair.

The fabrication of the proposed idea needs to deal with the integration of the metallic array nanostructures on top of the device's active region. Typically it is also required that the metal structures lie very close to the active substrate (a few nanometers) to optimize the coupling between the resonant structures and the device. Contrary to the fabrication on inert substrates, this task faces several challenges: surface topography, materials inter-compatibility, thermal budget limitations, as well as side damages induced by the integration, which could degrade the performance of the sensor, thus the choice of a CMOS-compatible nanofabrication technique becomes crucial. The focused ion beam (FIB) nanofabrication technique is one of the most promising in terms of feasible geometries and rapid prototyping, however, the direct patterning by FIB could induce ions implantation in the substrate or defects in device materials due to the sputtering effect. Both of them can damage the sensor or affect its electrical performances [13–16].

In this work, we demonstrate the integration of metallic nanogratings supporting SPP, on the top of a thin Silicon photodiode produced with a CMOS-like process flow. The PD used in this work have been fabricated at Fondazione Bruno Kessler, by using a technological platform similar to the one used for the production of SiPMs (FBK NUV-HD SiPMs [17]). Si-PDs have an overall thickness of around 3 µm and a junction depth of around 300 nm, for Si-PD with this specification, the quantum efficiency (QE, i.e. the probability of generation and collection of an electro-hole pair per and absorbed incoming photon) at 950 nm is around 5 %.

In order to realise the proposed idea and thus ensure higher absorption of Si PD in the NIR, specifically at 950 nm, the geometry of the plasmonic metal array was tuned by exploiting Finite Difference Time domain (FDTD) simlations (Lumerical [18]) to achieve maximum diode performance at 950 nm through light confinement. Thereafter, the plasmonic metal array is integrated on the active area of a Si-PD (PD) by a finely-tuned FIB patterning process. Finally, the integrated PD is characterised in terms of electro-optical response to assess its functioning and the performance improvement at 950 nm as a result of the plasmonic metal array integrated.

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2. Materials and Methods

2.1. Detector design and simulations

The proposed sensor design is shown in Figure 1, in which both the 3D sketch and the cross-section are reported. The device consists of a silicon epitaxial substrate (n- on n+) with a and shallow planar p-n junction (in blue). The surface is protected by a thin layer of dielectric material (in green). A 1-dimensional metal array (in gray) is then placed just above the dielectric layer, close to the active p-n junction. Such a structure is well known in the literature to support SPP modes at the metal/dielectric interface, along the sensor surface, in a direction perpendicular to the slits (as represented by the black arrows) [19]. These SPPs have also the characteristics to be strongly confined along the direction perpendicular to the sensor surface.
The periphery of the device is passivated by thick SiO_2 film, the bias voltage (V_{bias}) is applied from the metal top contact and the Si-PD is grounded from the bottom.
The resonance frequency of the metal grating depends on several geometrical parameters of the structure (grating pitch, metal and dielectric material, metal thickness). In order to tune the grating geometry for our specific purpose (efficiency enhancement at 950 nm), finite element optical simulations have been run by means of the Lumerical FDTD.

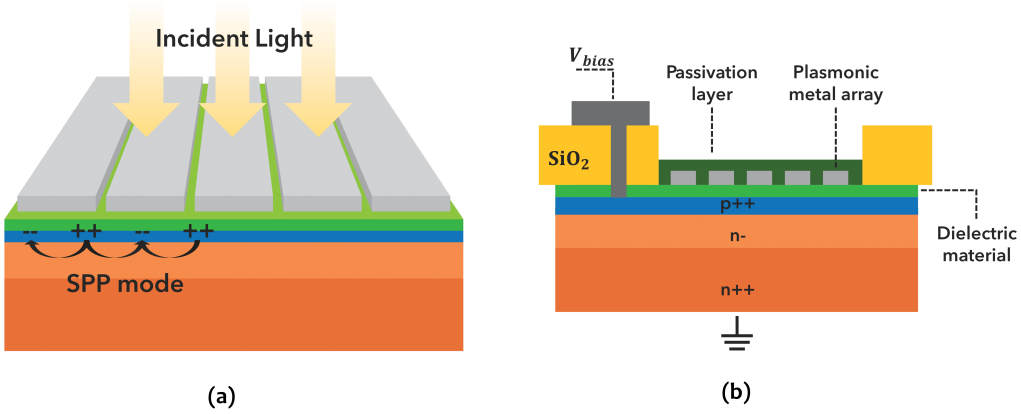

Figure 1. a) 3D sketch of the proposed structure of plasmonic metal array fabricated on the top of a silicon photodiode passivated with a thin dielectric film and supporting Surface Plasmon Polaritons (SPP) mode, b) cross-section of the plasmonic metal array over the active area of the Si-PD (p++/n-/n++), Si-PD is passivated by a thick SiO_2 layer and the bias voltage (V_{bias}) is applied from the metal top contact and the Si-PD is grounded from the bottom.

2.2. Simulation methods

In the simulation environment, the Si PD is represented by a semi-infinite silicon slab, over which a thin dielectric film is placed. The dielectric layer has a twofold goal: i) passivating the detector surface, reducing the surface recombination velocity, and ii)enabling SPP excitation at the interface between metal and a dielectric material. It is worth noting that to maximize the coupling between the surface SPP and the silicon, enhancing the carrier generation in the active substrate, the dielectric layer thickness has to be extremely thin (order of 10 nm) and precisely tuned, as demonstrated by numerical simulations in the next section. The simulated structures consist of 1-dimensional gratings, array of of infinite nanostrips. The light source is a planar wave TM polarized with respect to the strips. Only a unit cell has been studied by setting the proper boundary conditions to replicate an infinite array, see Figure 2. To maximize the fraction of the absorbed power in a 3 µm thick Si at 950 nm, the listed parameters have been finely tuned in the next section: i) grating pitch; ii) dielectric thickness; iii) metal thickness; iv) duty cycle (defined as the ratio between dot width and pitch). The maximized parameter is the total absorption power fraction at 950 nm, calculated as the ratio between the power absorbed in the first 3 µm of silicon (the active thickness of our devices) versus the total incident power.

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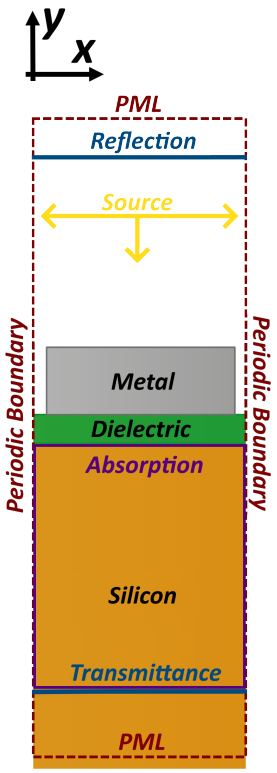

Figure 2. Cross section of the simulated structure cell with boundaries conditions (red dotted line) and recording monitors (blue for Reflection and Transmittance, purple for Absorption).

Figure 3 reports the simulated total absorbed power fraction versus the wavelength in the full visible-nir spectrum (orange curve). The same curve calculated for a device without any metal grating on the top is also reported for comparison (blue solid line). The simulated spectrum features three main peaks: i) an intense peak of around 58 % at 640 nm, ii) a less intense peak of 8 % at 700 nm and iii) the peak of our interest of 22 % at 950 nm.
It is worth noting that the simulated absorption curve shows a lower absorption than the reference across the whole simulated spectrum (450 - 1100) nm, with the exception of the peak at 950 nm where the absorption reaches the 22 %, about 4, 4 times higher with respect to the reference.
In Figure 3-b and -c are reported the H field 2D-maps, calculated on a plane perpendicular to the sensor surface, at 950 nm and at 900 nm, respectively. The magnetic field at 950 nm shows a pattern compatible with an SPP quadrupole resonance, with an evanescent component of the electromagnetic field, that becomes strongly confined in the first 500 nm from the surface. The EM field confinement can be considered the main responsible for the enhanced absorption at 950 nm. At a wavelength far from this resonance (i.e. at 900 nm) the electromagnetic field penetrates much deeper into the substrate, passing through the full active thickness of the device.
Generally speaking, the resonant modes of an open metal grating consist of hybrid optical-plasmonic resonance modes due to a combination of different phenomena. Among the others: i) cavity mode resonance in the inter-strip gaps [20,21]; ii) already mentioned SPP resonances at the interface metal/dielectric and iii) Wood-Rayleigh (WR) anomaly that consists in an abrupt change in transmittance at a wavelength where an order of diffraction is reflected outside the detector plane [22]. The latter effect is considered responsible for the asymmetric shape of the absorption peak at 950 nm. Approaching the WR anomaly at 950 nm, the first light diffraction order through the grating becomes more and more randent to the surface, producing a strong coupling with SPP, then, at the WR anomaly wavelength, the diffraction order is reflected out of the silicon surface, producing the abrupt drop of

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the absorption. For sake of completion, the physical explanation of the peak at 950 nm is well described and detailed in [23]. The geometrical parameters used in the simulated structure of Figure 3-a have been calculated and tuned by means of a simulative campaign, described in Section 2.3, in order to maximize the absorption at 950 nm in the first 3 µm of silicon. The silver grating has a thickness of 110 nm, a pitch of 535 nm and a DC of 0.80, while the dielectric interposer is an 11 nm thick silicon nitride layer. Finally, a 220 nm thick layer of PMMA coat the silver grating. The latter was designed to protect the metal and prevent silver tarnishing.

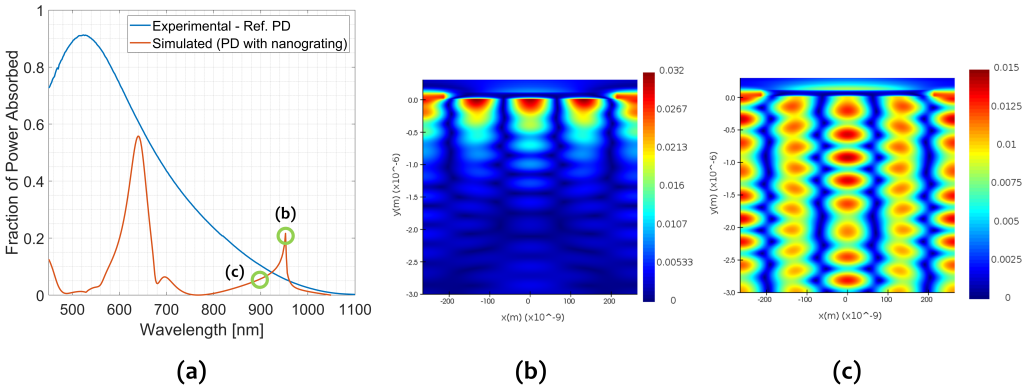

Figure 3. (a) Simulated absorbed light (orange solid line) and reference spectra (blue solid line) as a function of wavelength in the range (450 - 1100) nm; (b) Magnetic field intensity profile of the simulated section in Figure 2 at 950 nm; (c) Magnetic field intensity profile of the simulated section in Figure 2 at 880 nm demonstrating a diffraction pattern.

2.3. Simulative Campaign

The tuning process was a challenging task because of the multi-variable structures in which each factor is not independent of the other. The first step is to choose the best metallic and dielectric materials in terms of optical properties and their CMOS compatibility. The metal and dielectric materials available in Fondazione Bruno Kessler facilities and compatible with the PD fabrication process are silver, gold and aluminium and silicon nitride and silicon oxide, respectively. Among metals, silver is the most promising option because i) it has the strongest plasmonic resonance at 950 nm reaching an absorption 4.4 times more than the reference (compare to Au 2.1 and Al 1.9 only), ii) contrary to Au, Ag metal does not require any adhesion layer that could modify the plasmonic resonance behaviour. Although, the use of Ag required to take into consideration that it is easily tarnished. Regarding the dielectric material, both SiO_2 and Si_3N_4 have been tested as interposer material between silicon and metal grid, in the simulations. In both cases, thicknesses in the range of 5-50 nm have been tested. Using SiO_2 leads to an optimal thickness of 4 nm only, too thin to be precisely fabricated and to be used as a passivation layer for the PD. In the case of Si_3N_4, the maximum absorption at 950 nm is reached with a thickness of 11 nm. Therefore Si_3N_4 can be considered the better choice, mainly considering manufacturing feasibility.

Once the materials have been chosen, the geometric parameters (grating pitch, Si_3N_4 thickness, Ag thickness and duty cycle) need to be tuned. in spite of the multivariate problem, the tuning process has been faced by changing only one parameter at a time in an iterative process. The following steps could be summarize as:

1. find the pair of Ag thickness and grating periodicity (pitch) values that provides the highest absorption at 950 nm, see Figure 4;
2. select value pairs that are feasible by the nanofabrication point of view (low aspect to ratio factor) and at the same time guarantee a high absorption at 950 nm;

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3. study the influence of Si_3N_4 thickness and duty cycle (DC) on the fraction of light absorbed at 950 nm and select the best values, see Figure 5;

Ag thickness and grating pitch

The tuning process aimed at maximizing the absorbed power fraction of the structures in the first 3 µm of silicon at 950 nm. In the following plots this value has been normalized over the ideal absorption (with null reflection) of a 3 µm silicon without any metal grating on the top (absorption of about 5 % at 950 nm). In Figure 4 is reported the normalized absorbed power fraction as a function of the thickness (x-axis) and of the pitch (y-axis), from 100 nm to 300 nm the first and from 200 nm to 1000 nm the latter. At the pitch values of 260 nm, 535 nm and 790 nm, a higher absorption is visible. This effect is probably related to the WR anomaly at the n-th order of diffraction. In particular, at these pitch values, a strong maximum is present when the Ag thickness assumes values around 110 nm and 290 nm. Moreover, at these values of pitch (expected for the grater, 790 nm) ah higher absorption is shown at the Ag thickness values of 110 nm and 290 nm.

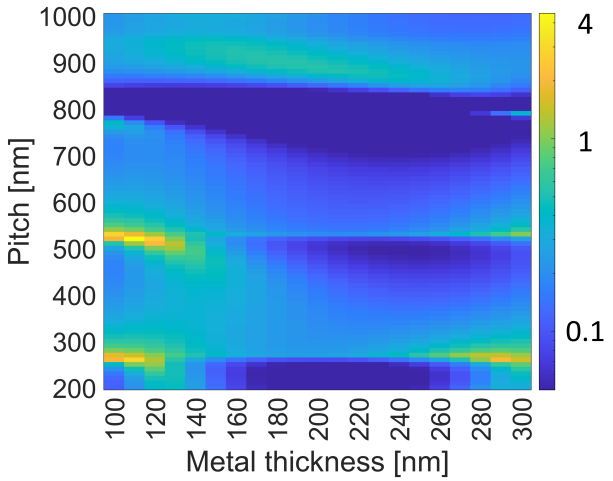

Figure 4. Normalized fraction of simulated absorbed power over the ideal absorption (with null reflection) of a 3 µm silicon slab integrated with a plasmonic metal array of a Dc of 0.80 over a thin Si_3N_4 layer of 11 nm at the wavelength of 950 nm as a function of the pitch and metal thickness.

Evaluation and selection of Ag thickness and itch

Considering the nature of the FIB technique (accelerated ion beam focused on sample to mill the material), a higher Ag thickness means higher dwell time (duration of stay unblanked over a point [µm], leading to a larger milling spot. As a result, the thicker the Ag layer is, the more difficult it is to obtain narrow slits. Thence, among the cited values couples the preferred Ag thickness is Ag thickness of 110 nm and a pitch of 535 nm.

3. Si_3N_4 thickness and duty cycle (DC)

The influence of the Si_3N_4 thickness and duty cycle (DC) is studied in Figure 5, where the absorbed power fraction as a function of the wavelength is reported.
Concerning the influence of DC (Figure 5-a): the peak position at 650 nm has a blueshift for increasing DC and a slightly increased intensity. By contrary, the behaviour of the peak at 950 nm is not influenced by the DC, but the higher the DC is, the more intense the peak is. Thence, theoretically, the best DC is 0.95, corresponding to a narrow slit of around 30 nm. To enable a feasible and reproducible nanofabrication process a DC of 0.80 (slit of about 100 nm) has been chosen as the best compromise between performance and feasibility.
Regarding the thickness of Si_3N_4 (Figure 5-b): the position of the peak at 650 nm has e redshift and a decrease in intensity by increasing thickness. The position of the peak at 950 nm is not affected by thickness, but its intensity does not have a monotonic dependence

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on the thickness of Si_3N_4, having indeed its maximum at 11 nm. The intensity of the peak at 950 nm is very sensitive to the thickness of Si_3N_4, in fact, the efficiency drops down to 4 % only for thickness greater than 18 nm and lower than 5 nm.

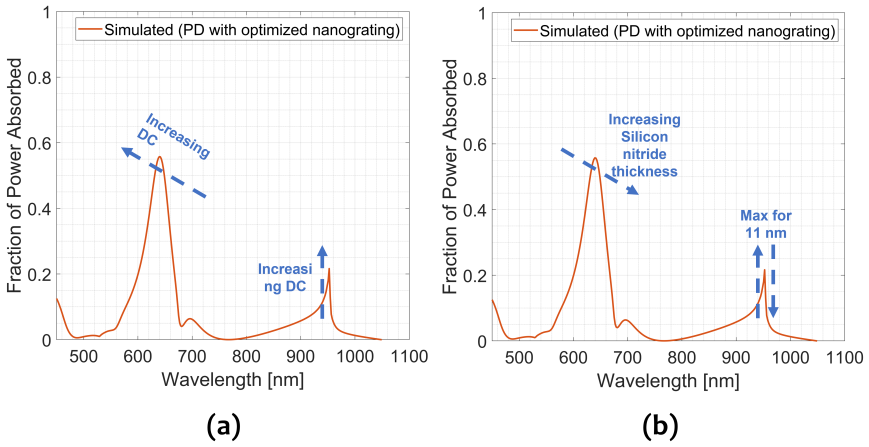

Figure 5. Fraction of simulated absorbed power as a function of wavelength and how the duty cycle and the silicon nitride thickness influence the main peaks.

To summarise, the optimised structure features a silver grating with a thickness of 110 nm, a periodicity of 535 nm and a DC of 0.80 lying over a thin 11 nm silicon nitride layer, and the array is passivated by 220 nm of PMMA.

3. Micro- and Nano-fabrication of integrated plasmonic detectors

Wafers with Si-PDs were fabricated using a standard CMOS-like processes at the internal facility of Fondazione Bruno Kessler. They were produced using a similar manufacturing process as the one developed for near-ultraviolet - high density (NUV-HD) Silicon photomultiplier (SiPM) technology, well described in [24,25]. Such a structure is provided with a shallow p on n junction, optimized to promote the photon detection efficiency in the near ultraviolet (NUV) spectral range. In fact, one of the challenges of this work is to demonstrate the potential efficiency enhancement of an optimized NUV device in the NIR by means of light confinement through plasmonic nanostructures. In this design, the Si-PD consists of a thin n-type epi-silicon layer (nominal thickness of 3 µm thick, featuring a planar shallow p-n junction (in order of (200 - 300) nm deep), formed by means of 11B ion-implantation. Subsequently, the top silicon surface is passivated by depositing the thin Si_3N_4 layer (by means of CVD deposition) and the periphery of the PD is protected by a thick (about 500 nm) layer of Silicon oxide. The ohmic contact is opened through this layer, and an Aluminium metallization is deposited to form front contacts to the p-type silicon to bias the junction.

To fabricate the silver nanostructures on top of the Si-PD, the Ag layer has been evaporated in an ultra-high vacuum physical vapour deposition (PVD) over the active area of the Si-PDs (100x100 μm^2). Areas defined by electron beam lithography (EBL), using a 10 keV electron beam on positive tone resist, Polymethyl methacrylate (PMMA). After the development, the Ag areas of Si-PDs were finally defined by removing the unexposed resist by lift-off in warm acetone (35 °C). Successively, the plasmonic nanostructures were patterned by FIB. After the patterning, to avoid silver oxidation and tarnishing, as well as the consequent degradation of the plasmonics performances, the device surface was capped with 220 nm of PMMA film by spin coating. The PMMA capping is then removed from the photodiode's pads with another EBL and development step, to make them electrically

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connectable to the printed circuit board (PCB) by gold-wire bonding.

3.1. Micro-nano fabrication methods

FIB patterning consists of an accelerated ion beam focused on the sample substrate, and because of the energy gain, the ions are able to sputter the sample's surface atoms thence milling the surface. The milling efficiency, called sputter yield (Y, i.e. number of sputtered atoms per incident ions), is affected by the sample's material as well as beam features (energy and ion species). Because of FIB process does not require any tool to transfer the pattern (unlike EBL and photolithography which need a resist and the latter also a hard mask), the geometries achievable by FIB have almost no constraints. However, the direct patterning by FIB could induce ion implantations in the substrate creating defects and damages in the sensor [26].

The Ag plasmonic nanostructures were patterned by using a Raith Velion FIB-SEM equipped with an Au-Si liquid metal alloy ion source (LMAIS) [27]. The structures were defined by an Au ion beam, accelerated at 35 keV with an ion current of 23 pA, and with the ion beam normal incidence to allow a better lateral resolution. Although Au is a well-known silicon contaminant, possibly reducing the minority carriers lifetime, the Au ion beam was found preferable to the Si beam because not only do they have larger Ag sputtering yield and thus shorter patterning times, but also shallower penetrations in the substrate that should limit the damages in the p-n junction region [28].

3.2. Experimental activities

Contrary to the fabrication on inert substrates, the integration of plasmonic nanostructures on an active device by FIB, needs to take into consideration the surface topography, the device's composition, the thermal budget limitations, as well as the ion implantation. Thence, the FIB milling parameters have been tuned by: i) optical investigation of the structures by secondary electron microscope (SEM) images, ii) selection of the optimal ion fluence (number of ions irradiated per unit of surface, also expressed as total charge irradiated per surface unit [$\mu C/cm^2$]) value to remove completely Ag by atomic force microscope (AFM) and iii) evaluation of the volume fraction of the implanted gold in the underlying device by dynamic secondary ion mass spectrometry (SIMS). The presentation of the FIB optimization process is not one of the aims of this work, for further details see [29].

The FIB process tuning leads to the following patterning parameters set: beam energy of 35 keV, beam current of 23 pA, ion fluence of 10 000 $\mu C/cm^2$.

In Figure 6 is reported the top view SEM image of the 1D Ag grating integrated on a Si-PD by FIB optimized process. The grating consists of an array of nanostrips with a measured pitch of 537 nm compatible with the nominal value, a dot width of 451 nm and therefore a DC of 0.84. In Figure 6, Ag grains are clearly visible and in some places have blown away probably due to too much stress. In addition to the top view image, the cross-section SEM image of a 1D grating is reported in Figure 7.

The 1D grating reported in Figure 7-a was produced with the same FIB process parameters but on a blank substrate (silicon chip) to enable faster analysis. the cross-section of the fabricated nanoarray was acquired using a Helios PFIB-SEM – equipment from Thermofisher, and to avoid any damage to the Ag structures, a Platinum layer was deposited using a gas injection system, 50 nm electron beam induced deposition (EBID), and 1 µm ion beam induced deposition (IBID), before proceeding with the cross section by a 30 keV Xe+ beam. The cross-section image confirms the thickness of the Ag layer of 110 nm, and suggests the funnel profile shape of the grating slit as a consequence of the nature of the FIB process. In addition, at the bottom of the slits, a brighter region is present as confirmation of the fraction of Au atoms implanted in the underlying device. For the sake of completeness, Figure 7-b shows all the labels to indicate precisely the different layers in the cross-section.

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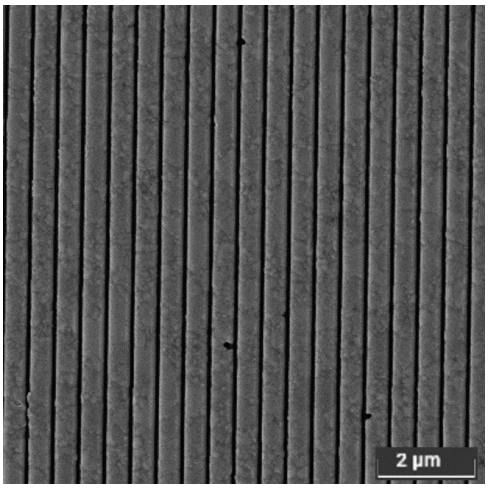

Figure 6. Top view SEM image of the FIB patterned 1D silver grating characterized by a pitch of 537 nm, a dot width of 451 nm and therefore a DC of 0.84.

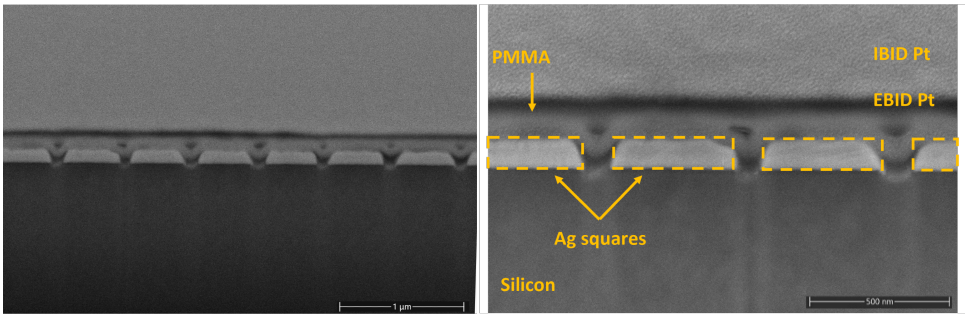

Figure 7. (a) Cross section SEM image of the FIB patterned 1D silver grating covered by 50 nm of electron beam induced Pt deposition (EBID), and 1 µm of ion beam induced Pt deposition (IBID); (b) Zoom in of the cross-section SEM image of the FIB patterned 1D silver grating with labels indicating precisely the different objects in the cross-section.

4. Results and Discussion

To characterize the integrated Si-PD and perform the electro-optical characterization, the Si-PD has been packaged on an appropriate printed circuit board (PCB), see Figure 8. The electrical link between the Si-PD's metal pads and the PCB pins is made via Au wire bonding technique. The back of the chip is coated with metal to act as bulk contact, yet, the chip is glued to the PCB by using conductive epoxy glow, with a final thermal curing process at 80°C.

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Figure 8. Top view picture of a produced sample after the integration on a printed circuit board (PCB).

Si-PD has been characterized using a custom-developed optical setup, which uses a halogen lamp as the (unpolarized) light source and a grating monochromator to choose the light wavelength impinging on the samples. The light exiting the monochromator passes through a variable aperture slit, which is set to select a bandwidth of 3 nm around the desired wavelength. This defines the wavelength resolution of the characterization setup. A polarizing filter is then mounted after the slit, to select a TM polarization with respect to the grating, for a direct comparison of the experimental spectrum with the simulations. The samples are mounted on a 3D moving holder that grants a precise positioning of the devices concerning the incident light beam. Once the PCB pins are connected to the holder, the responsivity (i.e. the ratio of generated photocurrent and incident optical power determined in the linear region of response), as well as the quantum efficiency (i.e. number of collected electrons over the number of incident photons of each Si-PD and one reference PD per chip) can be calculated. The Si-Pd is biased at 0 V working in photovoltaic mode. Responsivity spectra are acquired as a function of the incident wavelength, within the (450 - 1100) nm range. The QE of a reference diode, produced on the same chip, with the same thin layer of Si_3N_4 but without any metal grid has been also measured for direct comparison. These spectra can be compared to the expected simulated results calculated by FDTD Lumerical.
Figure 9 reports the measured QE curve of both reference PD and of the integrated PD described in this work. The simulated QE of the integrated PD is also reported for comparison (red solid line). In this case, the QE has been calculated from the simulated absorbed power fraction, by considering 100 % charge collection efficiency (CCE). In Figure 9, the QE curve of the reference PD is the blue solid line and it has an intense peak of almost of 90 % at 520 nm, which decreases as the wavelength increases and reaches a value of 5 % at 950 nm, the wavelength of our interested. The QE curve of the integrated PD (solid yellow line) reproduces all the three main peaks present in the simulations three peaks: i) an intense peak of around 50 % at 620 nm, ii) a less intense peak of 10 % at 750 nm and iii) a peak closer to the interesting wavelength of 24 % at 880 nm.

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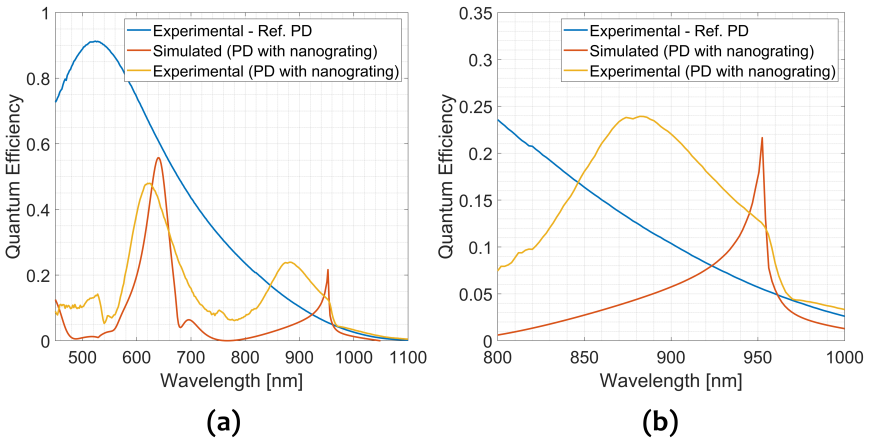

Figure 9. Measured QE of a reference PD (blue solid line), a fraction of absorbed light of the simulated structures (orange solid line) and measured QE of the integrated PD (yellow solid line) as a function of the incident wavelength in the range: (a) (450 - 1100) nm and (b) (800 - 1000) nm. Both simulated and QE of the integrated PD are lower than the QE curve of the reference at almost every wavelength except in the range around the wavelength of our interested 950 nm.

All the peaks in the measured spectra show slight differences in position or intensity with respect to the simulations. The peak around 620 nm is blueshifted of about 40 nm with respect to its counterpart in the simulated spectrum. In contrast, the less intense peak at 760 nm is redshifted from its counterpart of about 60 nm. Finally, the peak of our interest, which should be at 950 nm, is blueshifted of 70 nm and appear centred at 880 nm, but matching almost perfectly the QE drop at 960 nm. As expected, the QE of the integrated PD is lower than the QE of the reference PD for almost all the measured wavelengths, except for wavelengths around 950 nm, i.e. the target wavelength. At 950 nm the experimental QE demonstrates a value of 12 %, 2.2 times more than the reference but not as high as suggested from simulation (around 22 %, thence 4.4 times more).
Probably the difference between expected and measured QE is due to non-idealities found during the characterisation of the grating, such as funnel shape slits, Ag roughness, and conformal PMMA profile. The study of these non-idealities on the QE spectra required further investigation and simulations.

Despite the fabrication related not-idealities, the experiment QE enhancement can be considered an extremely promising result, demonstrating the strong potential of this structure for NIR absorption enhancement. To confirm this, in Figure 10 the measured QE is compared to the fraction of light absorbed by a slab of silicon covered by an ideal perfect antireflective coating (PARC, null reflection for every wavelength) with increasing thickness.
In particular, the QE curve and the simulated spectra are compared to ideal Si absorption with the same thickness (3 µm), two- (6 µm), three- (9 µm) and fourfold (12 µm) as the PD. It is interesting to note that to obtain the same fraction of absorbed light as one of the integrated diodes at 950 nm, it is necessary to triple the thickness of the Si with an ideal PARC. In addition, if we were able to achieve the same simulated QE, it would mean achieving the same absorption as a 16 µm silicon slab with a device only 3 µm thick.

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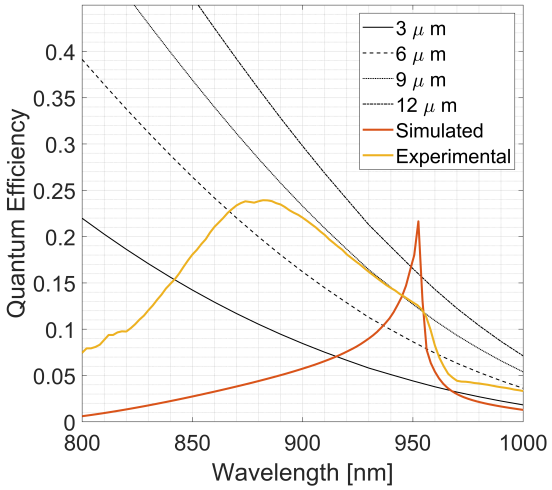

Figure 10. Comparison of the measured QE of the integrated diode and the simulated spectra with the fraction of light absorbed by a slab of silicon covered by an ideal perfect antireflective coating (PARC, null reflection for every wavelength) with increasing thickness.
In particular, the QE curve and the simulated spectra are compared to ideal Si slab absorption with the same thickness (3 µm), two- (6 µm), three- (9 µm) and fourfold (12 µm) as the PD.

5. Conclusion

Nowadays, light detection and ranging (LiDAR) applications, with the well know autonomous driving, are calling for silicon-based detectors capable of detecting single photons in the near-infrared (NIR). Silicon single photon avalanche diodes (SPADs) could meet the growing demand because of their properties and their lower fabrication cost because rely on well-developed and known silicon technologies. However, the main drawback of SPADs is the low performance in the NIR region due to the low absorption coefficient of Si in the NIR region.
In this work, we proposed to overcome the limited device's efficiency by the integration of CMOS-compatible nanostructures, specifically, metal array supporting Surface Plasmons Polaritons (SPPs), to confine superficially the incoming NIR photons and therefore increase photons probability to generate an electron-hole pair. The boost of the Si-PD efficiency in the NIR, specifically at 950 nm, is made possible by taking advantage of the plasmonic confinement of light at a deep-subwavelength scale.
The idea proposed is the integration on the active area of a Si-PD (layers: p++/n-/n++) of a 1-dimensional plasmonic silver array (thickness: 110 nm, pitch: 535 nm, duty cycle: 0.80) over a thin Si_3N_4 layer (thickness: 11 nm), passivated by a PMMA layer (thickness: 220 nm). The structure geometry was tuned by FDTD simulations to maximize the absorption of the underlying Si-PD at 950 nm.
From theoretical simulations, we expected an important enhancement (from 5 % to 22 %) at 950 nm. The Ag plasmonic nanostructures were obtained by patterning an Ag layer by using a Raith Velion FIB-SEM equipped with an Au ion beam.
Finally, the electro-optical properties of the integrated Si-PD with 1D plasmonic silver array are measured. The measured QE curve of the integrated Si-PD presents a peak of 24 % at 880 nm. At 950 nm the experimental QE demonstrates a value of 12 %, 2.2 times more than the reference diode without any metal grating (5 %) and well beyond the ideal absorption of Silicon with the same thickness, also considering no reflection losses.
Despite the considerable efficiency enhancement at 950 nm, the experimental value is still lowered than expected from the simulations. This difference can be due to some non-idealities, such as funnel shape slits, Ag roughness, and conformal PMMA profile. The study of these non-idealities on the QE spectra requires further investigation and simulations.

These results pave the way for further investigation and improvement of the structures, suggesting that better and better performance could be achieved in the next future.

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