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Article

Effective Number of Bits of the ADC with Input Driver Based on Operational Amplifier Working in Linear and Nonlinear Modes

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Abstract: The influence of linear and nonlinear modes of ADC driver on the operational amplifier (Op-Amp), which has different values of maximum output voltage slew rate, on the effective number of bits of ADC is considered. It is shown that the effective number of bits of ADC when op-amps on bipolar transistors with input signal amplitudes exceeding 50-100 mV is determined by the nonlinear modes of its input differential stage.

Keywords: effective number of bits ADC; ADC driver; operational amplifier; maximum output voltage slew rate; signal delay in ADC driver; linear and nonlinear operational amplifier modes

1. Introduction

The use of fast and ultra-fast ADCs such as EVIOAS150, EVIOAS350, AD9208, AD9691 in signal processing devices increases the requirements for operational amplifiers included in the ADC driver structure, which ensures the conversion of differential and non-differential input signals into differential signals at the ADC input.

The purpose and novelty of the present research is to estimate the effective number of bits ADC with regard to the signal delay time in the ADC driver, which depends significantly on the low-signal frequency characteristics of Op-Amp and the nonlinear operation modes of its input stage.

2. Amplitude-frequency and transient characteristics of Op-Amp in small and large signal mode

A typical circuit of Op-Amp in the structure of a high-speed ADC driver is shown in Fig. 1. In particular cases, the input analog signal can be fed to the first (In.1) or second (In.2) inputs, although the differential connection of the signal source is preferred.

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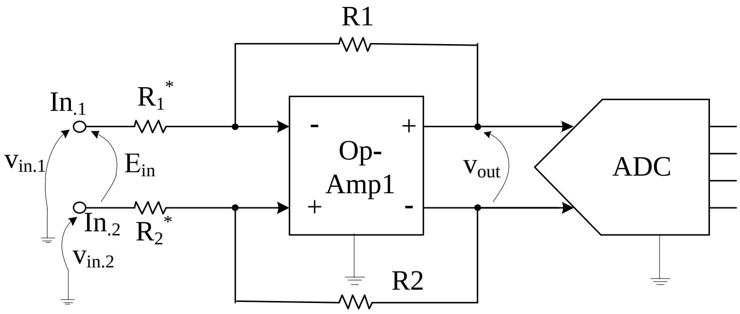

Fig.1 Circuit of ADC driver with non-differential and differential inputs based on Op-Amp with paraphase output

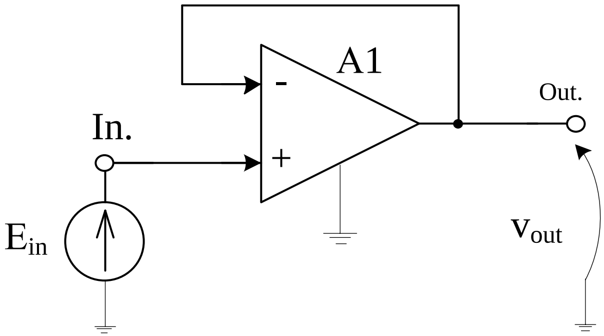

Fig.2 Non-inverting Op-Amp circuit (a special case of ADC driver)

The signal delay (t_{del}) in the driver in Fig. 2 can be determined from its transient in Fig. 3.

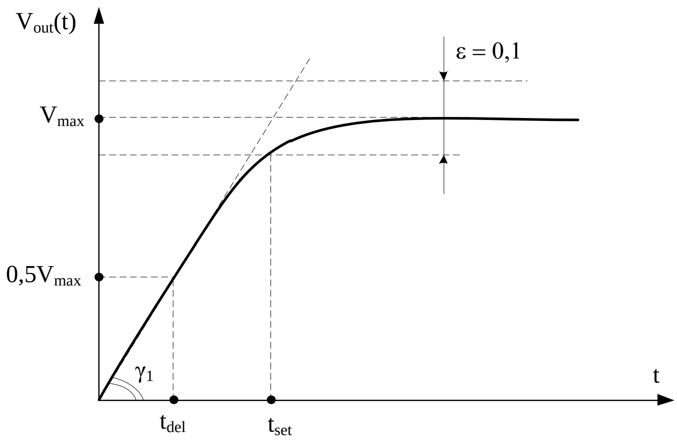

Fig.3 The transient process in the Op-Amp in Fig. 2 with 100% feedback ($V_{max} = E_{in}$)

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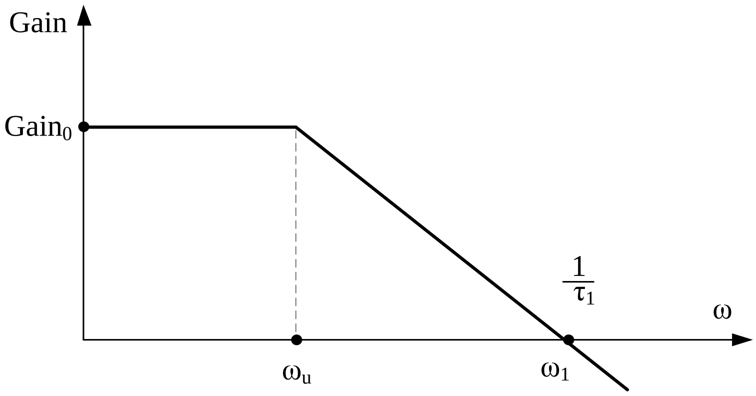

Fig.4 Logarithmic amplitude-frequency characteristic of an open corrected Op-Amp in Fig. 2

In the linear mode, the tuned Op-Amp with closed-loop feedback in Fig. 2 is a first-order LPF with Gain=1 (Fig. 5), the delay time in which $t_{del.S}$ reaches the smallest value.

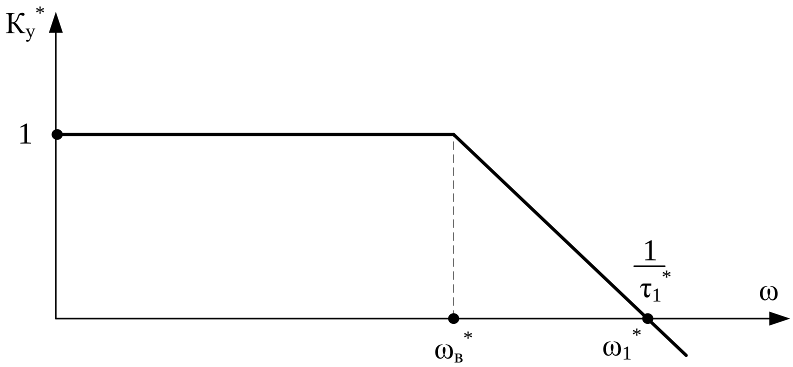

Fig.5 The LAFC of the closed-loop Op-Amp in Fig. 1 ($\tau_1^* \approx \tau_1/Gain_0$, $\omega_1^* \approx Gain_0\omega_1$, where ω_1^* is the single-gain frequency of the closed-loop Op-Amp; $\tau_1^* = \frac{1}{\omega_1^*}$)

In the high-signal mode (when $E_{in}=V_{max}$=1-5V), in which according to state standard the maximum slew rate of increase of output voltage of Op-Amp (SRB) is measured, the signal time delay $t_{del.B}$ can significantly (tens to hundreds of times) exceed the low-signal value $t_{del.S}$. The reason is a nonlinear mode of the input stage of Op-Amp (Fig. 6).

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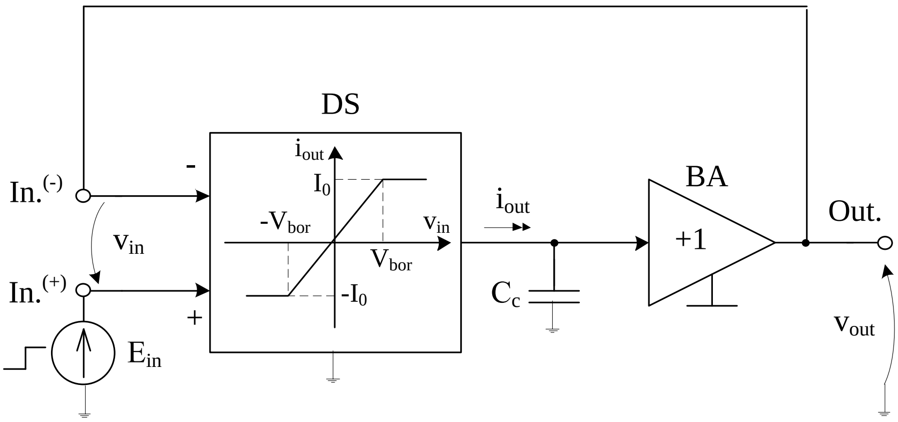

Fig.6 Operational amplifier with nonlinear input stage (DS)

For small and large signals, the 0.5V_{max} level delay time is determined by the formula:

$$t_{del.} = \frac{0,5V_{max}}{SR} \quad , \tag{1}$$

where $SR \sim tg\gamma_1$_1 is the maximum slew rate of the output voltage of the Op-Amp in linear or nonlinear modes;
V_{max} is the amplitude of the Op-Amp output voltage, which for the circuit in Fig. 6 is always less than the supply voltage.

Maximum slew rate SR_S for small signal in linear mode:

$$SR_S = \frac{E_{BX}}{\tau_1}, \tag{2}$$

where E_{in} is the amplitude of the input pulse; $\tau_1 = \frac{1}{\omega_1}$, $\omega_1 = 2\pi f_1$; f_1 is the low-signal frequency of the single-gain of the open corrected Op-Amp.

In the high-signal mode (with dynamic overload of the input stage in Fig. 6, Fig. 7)

$$SR_b = 2\pi f_1 V_{bor} = \frac{V_{bor}}{\tau_1} \quad , \tag{3}$$

where V_{bor} is the limiting voltage of the throughput characteristic of the input cascade of Op-Amp (Fig. 6).

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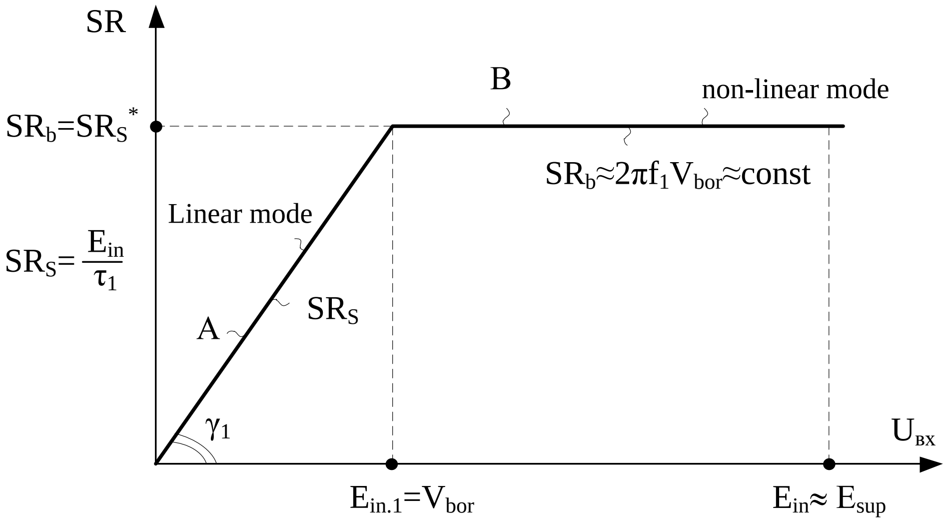

Fig.7 The dependence of the SR of the Op-Amp on the amplitude of the input pulse signal in Fig. 2 E_{in} ($SR_S^*=V_{bor}/\tau_1$)

Signal delay time in the ADC driver at small E_{in}

$$t_{del.S} = 0{,}5\tau_1. \quad (4)$$

The signal delay time in the ADC driver in the non-linear op-amp mode, when $E_{in}>>V_{bor}$:

$$t_{del.B} = 0{,}5\tau_1 \frac{V_{max}}{V_{bor}}. \quad (5)$$

If $V_{max}=V_{bor}$, i.e. Op-Amp is working at the border of linear and nonlinear modes, then

$$t_{del.B} = t_{del.S}.$$

When $E_{in}>>V_{bor}$, the proportion

$$\frac{t_{del.B}}{t_{del.S}} = \frac{V_{max}}{V_{bor}} = N_з \gg 1.$$

For Op-Amps on bipolar transistors at the supply voltage E_{sup}, for example, 5V, the numerical values of V_{bor} =50 mV, and the relative coefficient N_z reaches the value

$$N_з = \frac{5}{50 \cdot 10^{-3}} = 100.$$

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Thus, when performing ADC driver on bipolar Op-Amp and working with a large signal, the time delay increases by two orders of magnitude. This significantly reduces the effective number of bits of ADC with such a driver.

3. Estimation of ADC errors, taking into account the driver on Op-Amps, working in a wide range of changes in the input analog signal

Fig. 1 shows a circuit diagram of the monitoring and control system when performing ADC driver based on Op-Amps, working in linear and nonlinear modes.

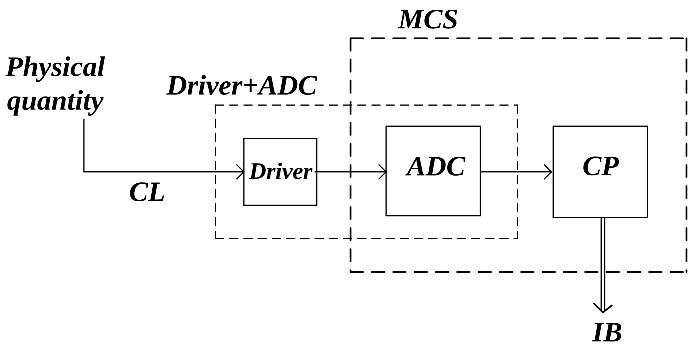

Fig. 8 Structure circuit of the monitoring and control system when executing the ADC driver based on the Op-Amp

In Fig. 8, the following designations are adopted:

- CP is a central processor of the automatic monitoring and control systems;

- IB is an interface bus of the MCS.

In this case, the effect of the driver on the processes in the system of Fig. 8 should be considered in conjunction with the ADC.

The static maximum reduced error of a q-bit ADC ($\gamma_{\mathrm{st}}^{\mathrm{ADC}}$) is determined by its least significant bit:

$$\gamma_{\mathrm{st}}^{ADC} = \left(\frac{1}{2^q}\right). \tag{6}$$

The dynamic error of the ADC ($\gamma_{\mathrm{dyn}}^{\mathrm{ADC}}$) occurs due to the delay of information at its output, which leads to an additional error [1], [2].

If we add to error (6) the dynamic error due to the time delay of the signal, then we can get the total ADC error ($\gamma_{\mathrm{com}}^{\mathrm{ADC}}$) in the form

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$$\gamma_{\text{com}}^{\text{ADC}} = \left(\frac{1}{2^{q}}\right) + \gamma_{\text{dyn}}^{\text{ADC}}. \tag{7}$$

This error corresponds to the ADC with the effective number of bits

$$q_{\text{eff}}^{\text{ADC}} = \left\lfloor \log_2\left(\frac{1}{\gamma_{\text{com}}^{\text{ADC}}}\right)\right\rfloor \ . \tag{8}$$

In (8), the sign $\lfloor\ \rfloor$ means that the nearest smaller integer number is taken.

Expression (3) can be written in the form that clearly shows the components of $q_{\text{eff}}^{\text{ADC}}$:

$$q_{\text{eff}}^{\text{ADC}} = \left\lfloor \log_2\left(\frac{2^{q}}{1+2^{q}.\gamma_{\text{dyn}}^{\text{ADC}}}\right)\right\rfloor = \left\lfloor q - \log_2(1 + 2^{q}.\gamma_{\text{dyn}}^{\text{ADC}})\right\rfloor. \tag{9}$$

The error of the driver located at the input of the ADC$(\gamma_{\text{com}}^{\text{Driver}})$ also has two components: static $(\gamma_{\text{st}}^{\text{Driver}})$and dynamic $\left(\gamma_{\text{dyn}}^{\text{Driver}}\right)$:

$$\gamma_{\text{com}}^{\text{Driver}} = \gamma_{\text{st}}^{\text{Driver}} + \gamma_{\text{dyn}}^{\text{Driver}}. \tag{10}$$

The driver error reduces the total effective number of bit of the analog-to-digital conversion process $(q_{\text{eff}}^{\text{com}})$:

$$q_{\text{eff}}^{\text{com}} = \left\lfloor \log_2\left(\frac{1}{\gamma_{\text{com}}^{\text{ADC}} + \gamma_{\text{com}}^{\text{Driver}}}\right)\right\rfloor. \tag{11}$$

Taking into account (9), expression (11) can be written in a form convenient for analysis:

$$q_{\text{eff}}^{\text{com}} = \left\lfloor \log_2\left(\frac{1}{\gamma_{\text{com}}^{\text{ADC}} + \gamma_{\text{com}}^{\text{Driver}}}\right)\right\rfloor = \left\lfloor \log_2\left(\frac{\left(\frac{1}{\gamma_{\text{com}}^{\text{ADC}}}\right)}{1+\left(\frac{\gamma_{\text{com}}^{\text{Driver}}}{\gamma_{\text{com}}^{\text{ADC}}}\right)}\right)\right\rfloor =$$
$$= \left\lfloor q - \log_2\left(1 + 2^{q}.\gamma_{\text{dyn}}^{\text{ADC}}\right) - \log_2\left[1 + \left(\frac{\gamma_{\text{com}}^{\text{Driver}}}{\gamma_{\text{com}}^{\text{ADC}}}\right)\right]\right\rfloor. \tag{12}$$

4. Direct and inverse tasks of estimating effective of number bits of ADC.

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Analytical dependence (12) allows two options for using the result obtained.

In the first option (direct problem), a specific analog-to-digital conversion system in the MCS is considered, in which the devices with known parameters (6), (7), (10) are used. As a result of the solution, the value of q_{eff}^{com} is obtained.

In the second option (inverse problem), admissible parameters (6), (7) and (10) are selected so that the value q_{eff}^{com} is not less than the specified one. Equations (6), (7), and (10) obtained allow us to formulate the requirements for both the ADC and its driver.

The static error of the ADC is determined by its number of bits q (6). The value of the maximum relative dynamic error of the ADC can be represented as [2], [3], [4], [5]:

$$\gamma_{dyn}^{ADC} = \frac{1}{A_0}|M_{max}|\,(t_{del}^{ADC}), \quad (13)$$

where: M_{max} is a maximum value of the first derivative of the converted signal; t_{del}^{ADC} is delay time of information in the ADC; A0 is an amplitude of the converted analog signal.

The delay time of information in the parallel ADC is determined by its timing diagram (Fig. 9):

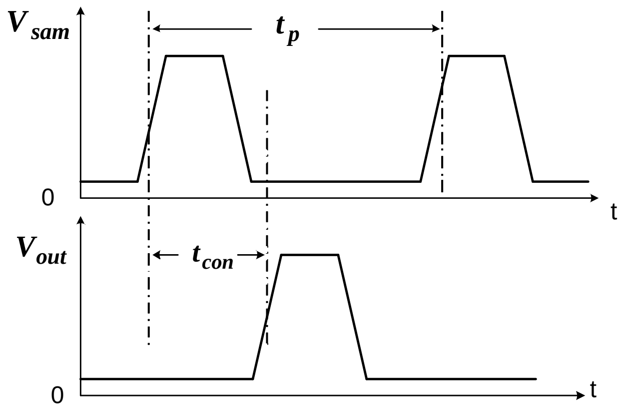

Fig. 9. Timing diagram of control pulses of the parallel ADC

In Fig.9, the following notation is adopted:

t_{con} is the time for conversion of the selected sampling into a digital code;

t_p is a sampling pulse period;

V_{sam} is ADC sampling pulses;

V_{out} – digital sample pulses.

The characteristic of the spectral density of the processed signal can be finite (the signal has a finite spectrum) or infinite (the signal has an extended spectrum). Subsequently, a signal

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with a finite spectrum is considered. Therefore, the maximum first derivative of the signal with a finite spectrum (M_{max}^{ϕ}) is determined by the Bernstein inequality [1], [3], [4]:

$$M_{max}^{\phi} \leq A_0 \cdot \omega_s, \tag{14}$$

where ω_s is a cutoff frequency characteristic of the signal spectral density at the level of $0{,}707 \cdot A_0$. Consequently,

$$\gamma_{dyn}^{ADC} = \frac{1}{A_0} |M_{max}| \left(t_{del}^{ADC}\right) = \omega_s \left(t_{del}^{ADC}\right). \tag{15}$$

5. Estimation of driver error on operational amplifier operating in linear and nonlinear modes.

The connection diagram of the driver to the ADC in the operational amplifier with the balanced input and output is given in Figure 1.

The static error of the driver (γ_{st}^{Driver}) is determined by the stability of the resistances of R1 ÷ R4, the offset voltage of Op-Amp1 and its drift, the input currents of Op-Amp1 and their instability, the attenuation factor of the input common-mode signal of Op-Amp1, the spread of resistances of the feedback circuits, the rejection factor on the power buses and it is determined by the well-known mathematical expressions [9].

The value of the maximum relative dynamic error of the driver (by analogy with the maximum relative dynamic error of the ADC) can be represented as:

$$\gamma_{dyn}^{Driver} = \frac{1}{A_0} |M_{max}| \left(t_{del}^{Driver}\right). \tag{16}$$

The value of M_{max}, as well as for the ADC, is equal to M_{max}^{ϕ} and it is determined by formula (14).

The value t_{del}^{Driver} determines the delay time of information in the ADC driver.

The information delay in the Driver can be obtained by representing it as the first-order Butterworth filter [7], [8]:

$$t_{del}^{Driver} = \frac{0{,}72772}{\omega_{Driver}}, \tag{17}$$

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ω_{Driver} is a cutoff frequency of the driver's spectral lasing at the level of 0.5, which actually determines the bandwidth of the Driver. Then

$$\gamma_{\text{dyn}}^{\text{Driver}} = 0{,}72772\left(\frac{\omega_s}{\omega_{\text{Driver}}}\right). \quad (18)$$

6. Evaluating the effect of ADC driver parameters on the effective of number bits of ADC

Table 1 shows the calculated values of the total effective number of bits ($q_{\text{eff}}^{\text{com}}$) of the ADC, taking into account the ADC driver, which show the change in $q_{\text{eff}}^{\text{com}}$ for the 10-bit parallel ADC with $q_{\text{eff}}^{\text{ADC}} = 9$from the ratio of the dynamic error of the driver $\gamma_{\text{com}}^{\text{Driver}}$ and the dynamic error of ADC $\gamma_{\text{com}}^{\text{ADC}}$, i.e. from the numerical values

$$N = \frac{\gamma_{\text{com}}^{\text{Driver}}}{\gamma_{\text{com}}^{\text{ADC}}}.$$

Table 1. Dependence of the total effective number of bits q_{eff}^{com} on the ADC parameters and ADC driver

$\frac{\gamma_{com}^{\text{Driver}}}{\gamma_{com}^{\text{ADC}}}$	0,0	0,1	0,5	1,0	2,0	3,0
$1 + (\frac{\gamma_{com}^{\text{Driver}}}{\gamma_{\text{com}}^{\text{ADC}}})$	1,0	1,1	1,5	2,0	3,0	4,0
q_{eff}^{com}	9	8	8	7	7	6

Thus, the error ratio $N = \frac{\gamma_{\text{com}}^{\text{Driver}}}{\gamma_{\text{com}}^{\text{ADC}}}$, which depends on the linear and nonlinear modes of Op-Amp operation, has a significant impact on the effective resolution of ADC.

Conclusion

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The inclusion of a driver based on high-speed operational amplifiers, operating in a wide range of changing amplitudes of the input signal at the ADC input allows the developer to purposefully address the issues of matching the modes of operation of the input functional units of the automatic control and monitoring system.

The dynamic characteristics of the op-amp driver, which depend on the amplitude of the input signal and the high-speed performance of the op-amp, significantly affect the overall effective resolution of the ADC.

The paper obtained mathematical expressions that allow to estimate the effective of number bits of ADC, taking into account the property of the Op-Amp-based driver - its linear and nonlinear modes.

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