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Article

Integrated 0.35 μm CMOS Control Circuits for High Performance Voltage-Mode DC-DC Boost Converter

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Abstract: The integrated DC-DC converter is appropriate for use in many domains, namely, display, cellular, and portable applications. This paper presents an integrated monolithic voltage-mode DC-DC boost converter with a low-power control circuit. The driver circuit requires an integrated converter to power up a digital logic circuit and converts the unregulated DC input to the controlled DC output at the desired voltage level. It is the integration of both power switches and control circuitry within the same CMOS technology to buck down and boost voltages using a switch mode regulator. In order to increase power efficiency in the DC-DC boost converter that provides low-power operation with a small chip size, a low-voltage operation is applied to the unique circuit characteristic. The operational transconductance amplifier(OTA), comparator, and oscillator in the control circuit are designed with the supply voltage of 3.3V and the operating frequency of 5.5 MHz. A compensator is used to create a pole that has sufficient phase margin for high stability. The DC-DC boost converter is measured in both experiment and simulation. Testing of the proposed circuit on the 0.35μm CMOS process shows that the output transient time of the amplifier can be controlled within of 7μsec and the output voltage is accurately controlled with a ripple ratio of 3%.

Keywords: CMOS; DC-DC converter; control circuit; integration; voltage –mode; boost converter

1. Introduction

In this paper we present a low-power system on DC-DC boost converter for display drivering applications. The high efficiency DC-DC converter with low-power integrated DC-DC boost converter is designed based on digital CMOS process[1,2]. An overall structure can be divided into two parts. The power stage includes two power MOS switches MN_1, MP_1 and the off-chip LC filter[3]. The control stage consists of the OTA, comparator, oscillator and gate driver. A power management circuit with buck and boost converters generates variable output voltages for high linearity and low power operations. The DC-DC converters require op-amplifier to reduce power transistors for power dissipation and generally achieve high accuracy [4-6]. The op-amplifier forces the drain-source voltage of the power transistor. This control circuit is a high gain in the differential pair[7,8]. The proposed integration boost converter is designed by few others works, but the buck converter is designed by many works. The Light Emitting Diode (LED) driver circuits for display applications require an integrated boost converter into the high voltage applications with low current load. A converter consists usually of a power switching stage and feedback control circuit. Among the variable circuit elements of the voltage-mode converters, OTA[9], comparator and oscillator in the control circuit are critical to the performance of the overall feedback control, which requires a fast-dynamic response and reduction of sub-harmonic oscillation. The feedback network is the system on integrated circuit for voltage-mode gate driver control. By using the properties of CMOS transistor, high performance control circuit can be manufactured. It enables an accurate sensing of inductor current at the high frequency. The proposed voltage-mode DC-DC converter is

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designed with a 0.35 μm CMOS technology. Though current mode control [10,11] is much better than voltage mode control, there are a lot of difficulties for the circuit implementation of current sensing skill. The CMOS process is suitable for use in voltage-mode controlled DC-DC buck and boost converter designs where rapid changes in input voltage are immediately reflected in feedback control circuitry. CMOS process is applied to the control circuit to obtain low noise and fast transient signal from the gate driver signal. It is suitable use of the high-performance regulators with simulation and experimental results of the proposed voltage-mode DC-DC boost converter.

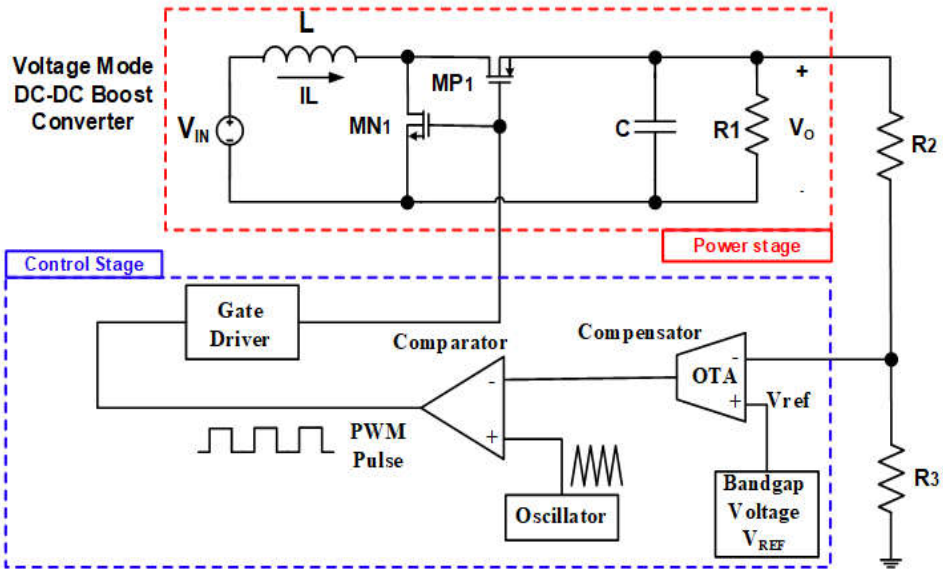

Figure 1. The block diagram of a voltage-mode boost dc-dc converter.

The structure of the voltage-mode boost converter consists for the power stage and control stage as shown in Fig. 1. The power stage includes two power MOS switches MN_1, MP_1 with off-chip LC filter. The voltage-mode DC-DC boost converter of the system on-chip is designed with 0.35μm CMOS process to provide a low-power and fully integrated power module. The input voltage of the op-amplifier is scaled down by R_2 and R_3. The off-chip LC filter are designed to have an inductance of 1 ~ 10 μH and a capacitance of 0.1 ~ 1 μF. The control circuit are designed with supply voltage of 3.3 V and operating frequency of 5.5 MHz.

2. Control Circuits

2.1. OTA(operational transconductance amplifier) Circuit

Two-stage operational amplifier configuration is a popular structure for CMOS op amps and it has reasonably good quality in addition to the simplicity of circuit. As seen in Fig. 2, two-stage operational amplifier configuration is composed of a differential amplifier input stage, current sources, and feedback compensator, which requires a fast transient response with low-power consumption.

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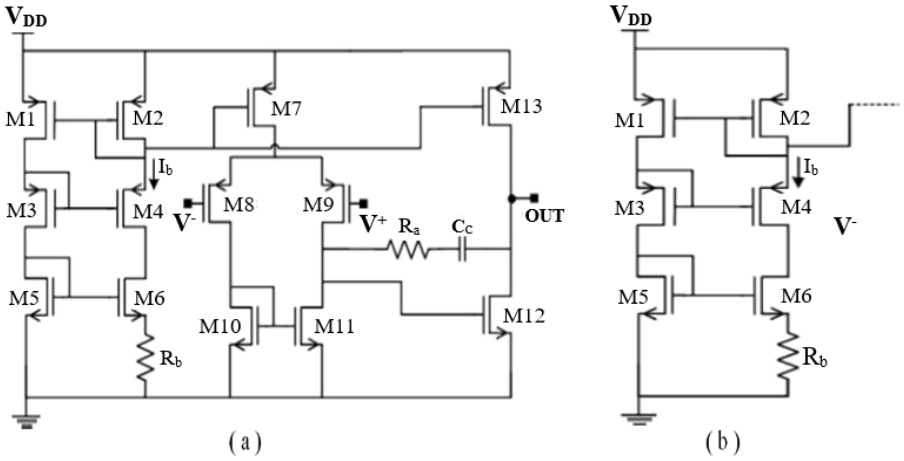

Figure 2. a)Two-stage CMOS op-amp configuration. (b)Configuration used to bias two-stage op-amp.

The OTA in Figure 2(a) consists of an input differential stage, source follower and current mirrors. A compensator is included in the op-amp to increase the stability of the frequency response and achieve a fast response time. Differential amplifier is used in the first stage since it is less sensitive to noise as a result of high CMRR(common mode rejection ratio). Although there is only a capacitor in the negative feedback path of the second stage (frequency-compensated) in OTA, a resistor R_a in series with C_C is used to improve the phase margin of the op-amp by placing zero at a negative axis location. It usually includes compensation circuit to achieve stability of frequency response and fast response time. The Compensators are used to poles or zeros to create sufficient phase margin for the high stability. A drawback of this configuration is that it does not have a low output resistance suitable for driving low loads or low input impedance next stages. In order to implement I_{REF} current in Fig. 2(a), the bias circuit in Fig. 2(b) needs to be that is capable of providing current independent of the supply voltage and MOSFET threshold voltage. A useful and interesting property of bias circuit is that the transconductances of the transistors biased by this circuit are only dependent on R_b value and device dimensions. As seen in Fig. 2(b), a resistor R_b is connected in series with the source of M_6. This resistor R_b is important in determining the bias current I_b and the transconductance of the transistor M_6.

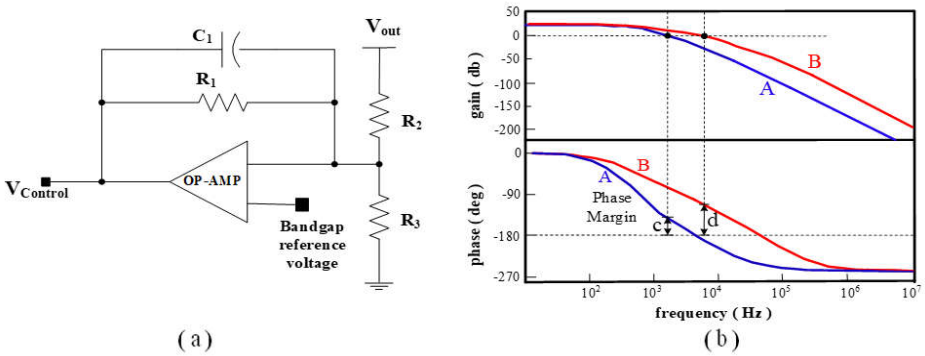

Figure 3. a) Schematic of compensator with operational amplifier. (b) Frequency response of the loop gain, with variation of the pole in the compensator.

Fig. 3(a) is an operational amplifier with a compensator. In terms of the frequency characteristics to the control-output transfer function, the function of the compensator with poles due to the RC filter can be written in the following form[12.13]. Miller's theorem can be applied to frequency characteristics. The resistors and capacitors are used to create poles or zeros in the compensator, where A_{op} and R_{out} are the gain and output

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resistance of the op-amp, and R_1 and C_1 are the resistance and capacitance of the compensator.

$$\frac{V_{control}}{V_{out}} = \frac{k}{(1 + sR_1C_1)} \quad (1)$$

$$f_C = \frac{1}{2\pi R_1 C_1} \quad (2)$$

$$A_S = \frac{A_{OP}}{(1 + S/\omega_P)}) \quad (3)$$

$$\omega_P = [R_P \cdot C_P]^{-1} \quad (4)$$

The stability and frequency response are determined directly by the pole. Whether the converter circuit is stable or not can be determined by examining the loop gain as a function of frequency characteristics. where k, R_1, and C_1 are the gain, resistance, and capacitance in the compensator. The f_C is the compensating frequency determined by the resistance R_1 and capacitance C_1 in order to increasing the phase margin in frequency response. Fig. 3(b) show in the frequency characteristics of output of op-amplifier which has phase margin of (B) is higher than that of (A). Here, the phase margin (c) is almost 0 ° and the phase margin (d) is 47 °. The frequency characteristic of the compensated op-amplifier is combined into the control feedback loop characteristics of the dc–dc boost converter. The results indicate that the compensator frequency should be higher than the natural frequency to provide a more stable condition in the frequency response and increased phase margin. The optimal phase margin is at least 60 °. Another factor affecting phase margin and stability is the gain of the op-amplifier given in equation (3). Op-amplifier are designed to maintain a small quiescent current during normal operation and withstand large input signal fluctuations. In this study, the transconductance of the operational amplifier was well controlled to maintain the stability of the converter.

2.1. Comparator Circuit.

The comparator in Fig. 4(a) is for the pulse-width modulation (PWM) control[14-15]. It is composed of bias circuit, input differential stage, and latch. The bias circuit is almost same as that of op-amplifier. The input stage is the circuit for start-up and bandgap reference. A start-up circuit is added to ensure that the bandgap reference circuit turns on when the supply voltage is applied. The load circuit consists of the current mirror configuration and thus presents the amplifier with a high resistance load. With current technologies, a gain large than 20 is achievable. The inverter and latch are used for a clear logic response and can act as a driver stage, so transistors in the current mirror can be made smaller to reduce parasitic capacitance.

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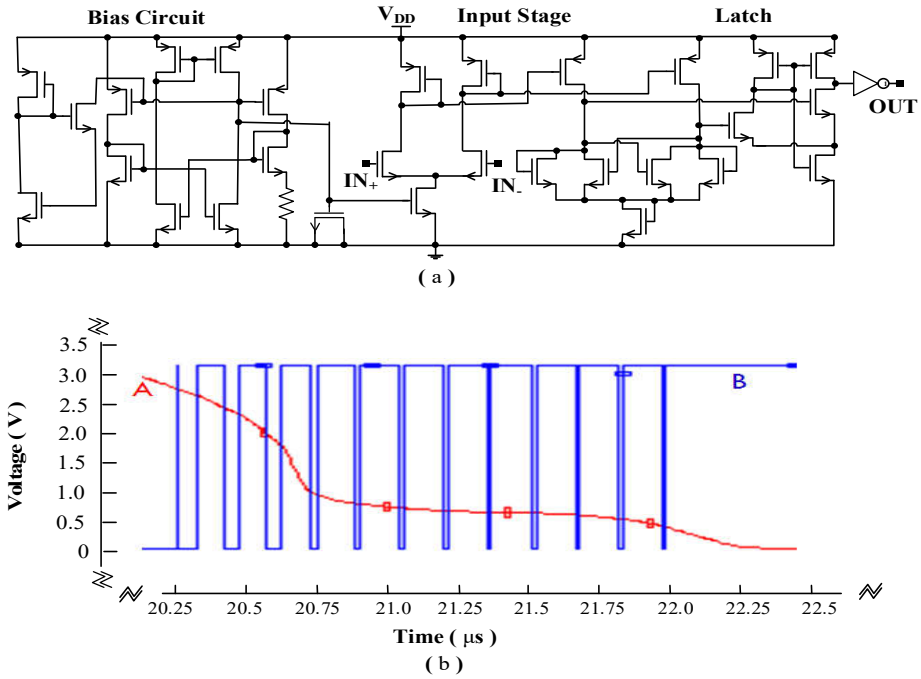

Figure 4. (a) Comparator circuit. (b) Outputs of op-amplifier (A), and comparator (B).

The operation of the comparator is a simple process. When the compensator output V is less than the triangular wave, the output voltage of the comparator has low values. When compensator output V is greater than the triangle wave, the output of the comparator is high voltage. Fig. 4(b) is the output wave forms of the op-amplifier(A) and the comparator(B). This is obtained from the Cadence simulation tool of the block diagram containing the power and control stage circuits. The output of the op-amplifier(A) quickly settles down due to the high conductance g_m of the differential pair. The comparator repeats the digital high and low logic until signal(A) passes the transient response.

2.3. Oscillator Circuit.

Oscillator is used for PWM control and in PWM switching [9]. The switch control signal is generated by comparing a signal level voltage control to a repetitive waveform. The signals of clock and ramp are shown in Fig. 5(a). Oscillator is sawtooth wave generator using the current sources and Schmitt trigger. The MOSFETs M_2 and M_3 is used as switches. Schmitt trigger circuit with NAND gate is implemented to obtain ramp signal and clock signal. The signal clock and ramp signal are generated from a trigger signal.

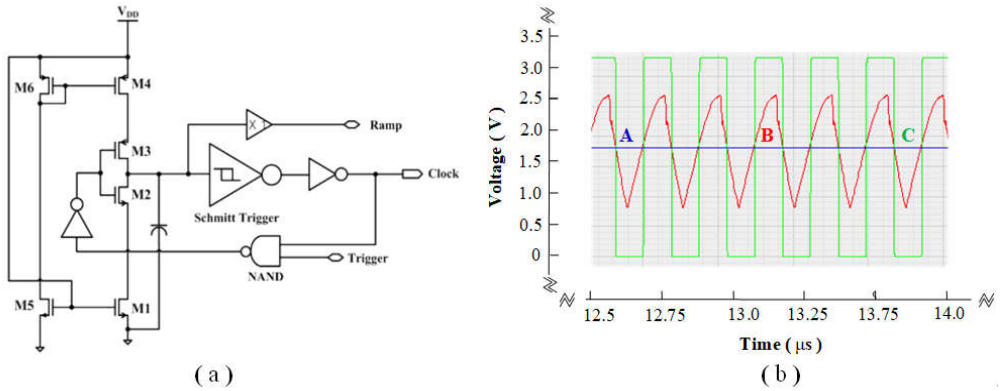

Figure 5. (a) Oscillator circuit. (b) Output of compensator(A), oscillator(B), and comparator(C).

Fig. 5(b) is the output wave forms of compensator(A), oscillator(B), and comparator(C). When the compensator output V is less than the triangle wave, the output of the

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comparator is a low voltage. When compensator output V is greater than the triangle wave, the output of the comparator is a high voltage.

2.4. Gate Driver Circuit.

Fig. 6(a) is the gate driver circuit. The circuit is connected to the power switches of the MN_1 and MP_1 power MOSFETs and it is must be carefully designed as it can be draw large currents and provide overshoot currents during switching transitions. Gate driver circuit consists of NAND, NOR gates and SR latches. The signals of ramp (A) and clock (B) are as shown in Fig. 6(b). The duty ratio, frequency, and amplitude can be changed by variation of the parameters V_H, V_L, and V_{REF} inside the oscillator.

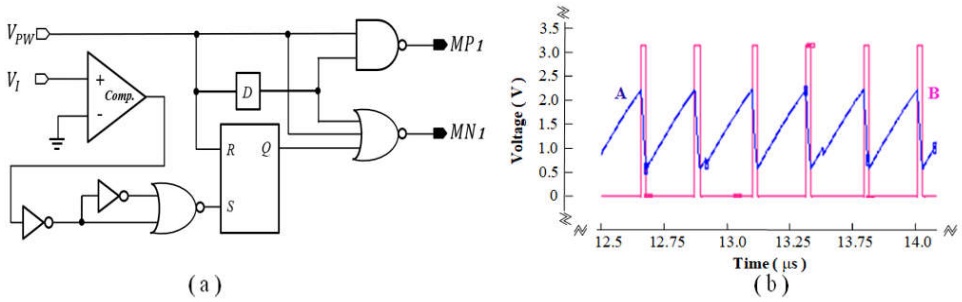

Figure 6. (a) Gate driver circuit. (b) signals of ramp(A) and clock(B).

3. Results

3.1. Output results of simulation and experimental.

The voltage-mode DC-DC converter with on-chip integrated PWM circuit operates at 5.5 MHz frequency with input voltage of 3.3 V. The power MOSFET of the power block is isolated from the control block to avoid noise. LC filter is designed with inductance of 1~10 μH and capacitance of 0.1 ~1 μF. The simulation result of inductor current I_L and inductor voltage V_X is shown in Fig. 7(a). It obtained with the input voltage of 3.3 V, inductor 10 μH, capacitor 1 μF, and the duty ratio of 0.7. Charge and discharge time of the inductor current I_L is accurately sensed. The ripple current depends on the output voltage, inductance, and duty ratio. The discharge time is approximately 0.07μs.

The inductor current indicates 190 mA within 5% ripple. Fig. 7(b) as show in the output and ripple voltages of DC-DC boost converter are 6.3V and 75mV, respectively. The output voltage can be obtained as expected with a negligible ripple ratio, and in LC filter converters, glitches typically occur in the on-off switching transistors in the power block. Fig. 1 is obtained from the cadence simulation tool which includes the power and control circuits. The duty signal for the power switches of the MN_1 and MP_1 power MOSFETs is approximately 70%.

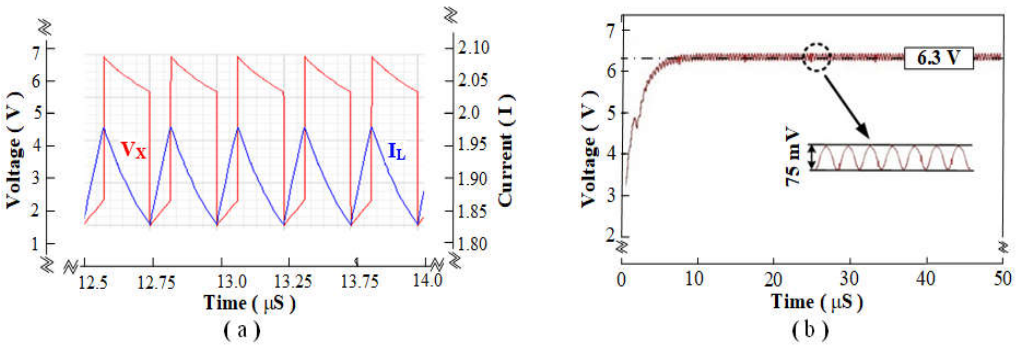

Figure 7. (a) Gate driver circuit. (b) signals of ramp(A) and clock(B).

Experimental signals from the oscilloscope are shown in Fig. 8(a) the input trigger signal and Fig. 8(b), where A, B, and C are the inductor voltage V_L, feedback voltage, and

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output voltage respectively. The output voltage is obtained as 5.6 V at a switching frequency of 5.5MHz. The signal is acquired as expected. The voltage V_L after the inductor shows the high ripple signal during the on-off switching state. The output power is approximately 300mW. The glitches in the A and C signals are caused by mismatch to the power switch of the MN_1 and MP_1 power MOSFETs. It was obtained with inductor of 10 μH, input voltage of 3.3 V, capacitor of 1 μF, and duty ratio of 0.5.

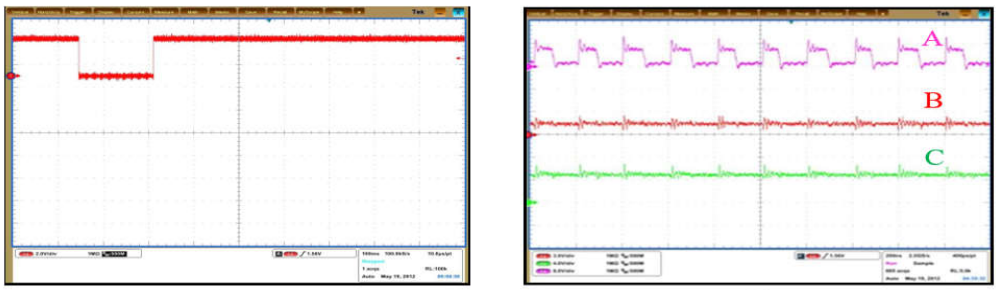

Figure 8. (a) Input trigger signal. (b) Experimental output result. Inductor voltage(A), feedback voltage(B), and output voltage(C).

3.2. Designed condition and photo die of the proposed DC-DC boost converter.

The performance of proposed voltage-mode DC-DC converter is compared as shown in Table 1. It achieves the high figure of merit with a small chip area

Table 1. Design condition.

Technology	**0.35 *μm* CMOS process**
Input voltage (V_{IN})	3.3 *V*
Output voltage (V_O)	5 ~ 7 *V*
Load current (I_L)	15 *m* ~ 100 *mA*
Switching frequency (fs)	5.5 *MHz*
Ripple voltage	10 *m* ~ 100 *mV*
Efficiency	77% (I_L; 100 *mA*)
Die area size	0.5 mm^2

The proposed DC-DC boost converter is designed in 0.35 μm CMOS technology with 2-poly and 4-metal process.

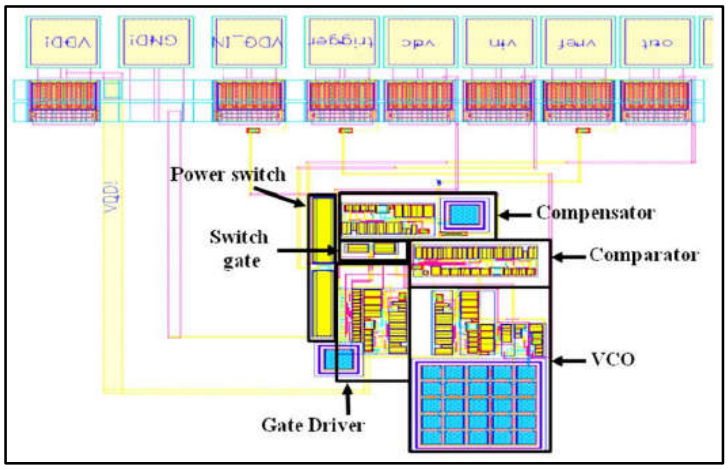

Figure 9. Die photo of the DC-DC boost converter.

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4. Conclusion

Voltage-mode DC-DC boost converter with a fully integrated power system is presented in this article. The proposed voltage-mode DC-DC boost converter is designed 0.35 μm CMOS technology with 2-poly and 4-metal process. The experimental result of the output voltage was 5~7V at an input voltage of 3.3V and a switching frequency of 5.5MHz. The proposed converter can be used chip miniaturization and a low power LED driver IC. The power consumption is approximately 300mW and the maximum efficiency 77%. As a result, the voltage-mode DC-DC boost converter has a simpler circuit structure than the current-mode converter. It was superior performance in terms of output voltage and power consumption.

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Conflicts of Interest: The authors declare no conflict of interest.

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