 doi:10.20944/preprints202210.0255.v1

Article

Implementation of a Modular Distributed Fault-tolerant Controller for MMC Applications

Semih Isik [1]*, Vasishta Burugula [1], Mohammed Alharbi [2], Ali Azidehak [1] and Subhashish Bhattacharya [1]

[1] Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC, 27606 USA
[2] Department of Electrical Engineering, College of Engineering, King Saud University, Riyadh 11421, Saudi Arabia
* Correspondence: sisik@ncsu.edu

Abstract: Centralized control algorithm limits the hardware flexibility of a Modular Multilevel Converter (MMC). Therefore, industrial MMC applications have started adopting distributed control structures. Even though distributed controller reduces a single point of failure risk compared to the centralized controller, the failure risk of the entire control systems increases due to the number of local controllers. However, the distributed controller can be programmed in such a way as to bypass the faulty local controller and take care of the power modules with the adjacent local controllers. This paper implements a modular distributed fault-tolerant controller for a scaled laboratory MMC prototype. Experimental results show that an MMC can operate without interruption, even under two local controller failures. Besides, the experimental results are verified with the Opal-RT, a real-time simulator with the same controller in a Control Hardware in Loop (CHIL) environment.

Keywords: controller; centralized; distributed; CHIL; fault-tolerant; MMC; prototype; Opal-RT

1. Introduction

Global energy demand rises every day, but the rise in the generation is not as fast as the demand. Most electric energy demand is supplied by burning fossil fuels. However, energy generation from fossil fuels is not sustainable and threats the planet. So, energy demand should be supplied through sustainable energy sources to reduce the carbon footprint and the harmful effects of fossil fuels. Sustainable energy sources, such as solar, wind etc., grow daily. Still, existing utility grid infrastructures are not yet ready to integrate all the distributed sources due to their complex and traditional structure [1]. Besides, sustainable sources vary naturally, so energy storage systems are needed for smooth integration. Undoubtedly, the need for clean, affordable and sustainable energy is more significant than ever to protect the environment and meet the demand. To integrate bulk power from renewable energy sources, conventional AC power grid infrastructures should be strengthened, and energy storage systems should be developed to reduce the variability effect of the renewables [2]. However, modernizing the existing power grids might be challenging, time-consuming and extremely costly.

On the other hand, High Voltage Direct Current (HVDC) transmission is a versatile alternative to AC transmission for carrying more power from remote locations with fewer conductors and lower losses. HVDC transmission is more cost-effective for longer distances because it has minor capacitive losses than the HVAC, especially when the conductors are placed closer to the ground. Hence, reactive power compensation is not required along with the transmission as opposed to AC transmission. Unlike DC cables, HVAC lines are subject to corona discharge, so the conductors are bundled to increase the effective radius. However, bundling the conductors increases the overall line capacitance and reactive power consumption [3]-[7].

DC current transmission is an excellent candidate to integrate renewable energy, yet high voltage transmission is necessary to lower transmission losses. However, raising the

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voltage to hundreds of kV is challenging with two- or three-level converter topologies due to the limited number of series-connected power modules. Therefore, Modular Multilevel Converter (MMC) has recently been the primary selection for high voltage transmission applications due to its scalable and modular structure. MMC can easily increase or decrease the voltage level with the series connected power modules, called Sub-Module (SM). However, the performance of an MMC highly depends on the control structure as each SM capacitor voltage needs to be monitored and controlled at all times [8],[9].

The MMC controller should manage AC and DC side voltage and internal MMC current. These tasks can be categorized under the higher-level and lower-level control, respectively. In general, higher-level control aims to control DC link voltage or the output power of the converter. The lower-level control is much faster than the higher-level control and manages the inner current, capacitor voltage balancing, averaging, and modulation. Circulating Current (CC) control can also be categorized under lower-level control. A Central Control Unit (CCU) or distributed controllers can perform higher and lower-level control tasks. In the case of a centralized controller, all computation is performed based on the measured signals and control commands in a central control unit such as Digital Signal Processor (DSP), Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC) chip. The centralized control algorithm is relatively fast, but hardware flexibility is limited. Besides, the computational burden, modification of the controller and the communication links can be pretty challenging for high voltage MMC applications due to a vast number of power modules. A centralized controller is currently adopted for MMC-based medium voltage motor drive applications [10] or laboratory scale prototype applications [11]. The CCU limits the scalability and modularity features of an MMC because the entire control system needs modification in case of any hardware changes. In case of a high number of SM, a significant computational burden on CCU might be experienced, and this might cause an undesirable overrun for each control cycle.

On the other hand, the distributed control algorithm assigns some tasks to the Local Controller (LC) while keeping a central unit as a master controller. MMC-based industry applications have recently started moving towards a distributed-based control structure [12[,[13]. In distributed control structure, local controllers of each SM or group of SMs can make necessary computations with less communication with the master controller. This scheme's significant advantage is reducing the communication bandwidth and computational load on the CCU. However, precise synchronization between the local and master controllers is necessary for proper operation. Otherwise, improper controlled power modules may cause unstable operation for an MMC application.

A distributed controller can significantly reduce the probability of a single point of failure. Nonetheless, the failure risk of the entire control system increases due to the number of local controllers. Nevertheless, the distributed controller can be programmed in such a way that any faulty controller can be bypassed, and the adjacent local controller can take care of the power module. Therefore, a well-structured distributed controller can easily handle the failure of a local controller(s) or power modules.

This paper presents a distributed fault-tolerant controller [14] implementation with a downscaled MMC prototype to prove the concept of MMC operation under local controller failures. The experimental results show that MMC can be operated without interruption, even under two failed local controllers. Besides, the experimental results are validated with the Opal-RT real-time simulator with the same modular fault-tolerant controller.

2. Mathematical Model of an MMC

The circuit configuration of an MMC can be seen in Fig. 1 with Half-Bridge SM (HBSM). Cascaded connection of HBSMs in series with the arm inductor (L_{arm}) establishes an MMC arm. A three-phase MMC consists of six identical arms. Each HBSM has one capacitor (C_{SM}) and two IGBT switches. Controlling the switches in the HBSM, each capacitor can be connected in series with the arm inductor or bypassed from the circuit.

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Arm voltage is determined based on the number of inserted SMs. Thus, increasing or decreasing the voltage level of an MMC application depends on the number of inserted modular SMs. The references voltage for the upper ($v_{u,x}$) and the lower ($v_{l,x}$) arm can be determined based on AC and DC side dynamics as (1) and (2), respectively. V_{DC} represents the DC link voltage, V_{mx} represents the AC side voltage and V_{cx} represents the circulating voltage (3) induced on the arm inductors due to circulating current [15]-[17]. Circulating current occurs due to voltage differences between the arms.

$$v_{u,x} = \frac{V_{DC}}{2} - V_{mx} - V_{cx} \tag{1}$$

$$v_{l,x} = \frac{V_{DC}}{2} + V_{mx} - V_{cx} \tag{2}$$

$$v_{z,x} = L_o \frac{di_{Z,x}}{dt} \tag{3}$$

$$n_{u,x} = \frac{1}{V_{cu}^{x}} V_{u,x} \tag{4}$$

$$n_{l,x} = \frac{1}{V_{cl}^{x}} V_{l,x} \tag{5}$$

$$i_{u,x} = i_{z,x} + \frac{i_x}{2} \tag{6}$$

$$i_{l,x} = i_{z,x} - \frac{i_x}{2} \tag{7}$$

$$i_{z,x} = \frac{i_{u,x} + i_{l,x}}{2} = i_{dc,x} + i_{circ,x} \tag{8}$$

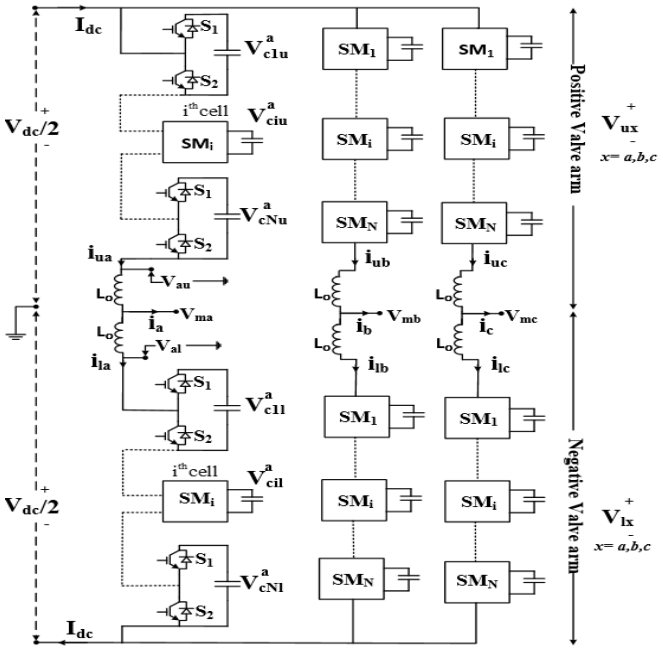

Figure 1. Three-phaseMC Circuit Configuration with Half-Bridge Sub-Module.

The modulation index determines the number of inserted or bypassed capacitors based on the arm's reference voltages. During a steady-state, the insertion index for the upper and lower arm is determined in (4) and (5), respectively where $\boldsymbol{V_{cu,l}^{x}}$ represents individual capacitor voltage in the arms. Similarly, upper ($\boldsymbol{i_{u,x}}$) and lower ($\boldsymbol{i_{l,x}}$) arm current

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can be expressed in terms of differential current and AC side current (6) and (7), respectively. Differential current ($\boldsymbol{i_{z,x}}$) (8) has AC and DC parts. The AC part is the circulating current, the same for all the phases, whereas the DC part is one-third of the DC current per phase under a steady state.

3. Modular Distributed Fault-tolerant Controller

As seen in Fig. 1, series-connected SMs are the backbone of the MMC structure. Increasing or decreasing the number of the series-connected SMs allows adjusting the generating voltage level. In case of a high number of MMC applications with a centralized controller scheme, any changes in the hardware require extensive control algorithm modification. Therefore, a centralized controller indirectly limits hardware flexibility. Unlike the centralized control scheme, distributed control scheme helps reduce the burden on the master controller and assigns some of the tasks to local controllers. An illustration of the modular distributed fault-tolerant controller can be seen in Fig. 2. In distributed control scheme, the master controller mainly controls the total energy in the MMC arms by measuring the AC and the DC side and communicates with the local controllers for the capacitor voltage balancing. Averaging (phase balancing) controller, seen in Fig. 3, ensures that phase voltages are distributed equally (9). Differential current compensates for the error whenever there is a mismatch between the average arm voltage and the individual SM voltage. The master controller synchronizes the local controller based on its reference frequency. The synchronization process compares the reference frequency of the master controller and the local controller, and the error is compensated (10) where f_m is the reference frequency, f_e is the error and f_l is the frequency of a local controller. Similarly, the time error can be determined in (11) as a function of frequency and compensated when needed.

$$V_{dc} = \sum_{n=1}^{4} V_{SMn,x\,ul} + L_{arm}\frac{d(i_{u,x} + i_{l,x})}{dt} \tag{9}$$

$$f_e = f_m - f_l = w_e = 2\pi f_e \tag{10}$$

$$t_e = \frac{f_e}{f_m}t \tag{11}$$

$$CAM_{i,1} = \begin{cases} 0\ if\ [F_{LC,i} \wedge F_{LC,i+1} \wedge F_{LC,i-1}] = 1 \\ 1\ Otherwise \end{cases} \tag{12}$$

Distributed controllers for multilevel converters have become an appealing research topic due to easy modification, less data transfer, and faster computation. Besides, the distributed controller reduces the risks of the single point of failure. In literature, most of the fault-tolerance and resiliency research are devoted to SM-level failure and redundancy [18]-[20] due to a higher failure rate of the SM components. However, it is critical to consider the failure of SM controllers. Especially in critical systems, failure of a local controller(s) is unacceptable as the system stability will be lost due to miscalculation. Therefore, adding a fault-tolerant feature to the distributed control algorithm is highly desirable. A resilient controller aims to reduce the effect of a failure utilizing firmware or redundant components. This paper adopts a resilient two-dimensional redundant controller [21], seen in Fig. 4. to integrate into a scaled-down, three-level MMC prototype. In this controller, local (slave) controllers have a one-dimensional array that synchronizes the local controllers with the master. The controller has one master and twelve Texas Instrument (F28379D) Digital Signal Processor (DSP) cards. The local controllers are connected to the master controller through a shared serial-communication bus. The output of these controllers is fed into dedicated Altera (ACM-204-40C8) Field Gate Programmable Arrays (FPGAs). The role of the FPGAs is to detect fail-over the local controllers. A controller block diagram can be seen in Fig. 5. Each local controller checks the neighbor controllers'

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status for every control cycle. In case of a local control failure, the faulty controller is by-passed, and the neighbor controller takes care of the faulty controller's SM. In this design, each controller is directly connected with all the controllers and data is transferred using a series port. Therefore, each controller controls the dedicated power module and communicates with the neighbor controllers. Each controller compares the computation results and measured signals to check the health status of the neighbor controller. In case of a local controller failure, both the neighbor controllers compare the errors to detect the failure as in Fig. 5. Then, one takes the faulty controller's role. The Controller Availability Matrix (CAM) expresses (12) if there is any controller available to take the vacant SM where $F_{LC,i}$ is the failed controller, $F_{LC,i+1}$ is the upper controller, and $F_{LC,i-1}$ is the lower controller. The dedicated FPGA runs the matrix and chooses the necessary controller for the vacant module. Each FPGA has six PWM signals as inputs from three controllers, the main and two neighbor controllers. Besides, two error signals are fed into the FPGAs to determine the health status.

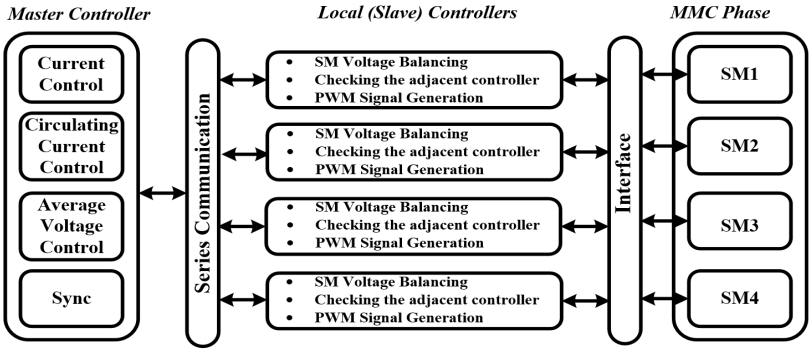

Figure 2. An Illustration of the Modular Distributed Fault-tolerant Controller.

Two PWM signals from two controllers are compared to check a mismatch. If the PWM signals of the neighbor controllers are not the same at an instant, the counter, seen in Fig. 6, exceeds a predefined threshold, and the error signal goes high. This event is named a fail-over condition, and it has two steps. The first is to check the fault signal to decide if any of the main controllers are faulty. The main controller's output is compared with the adjacent controllers. If the outputs of these comparisons are different, the main controller does not create the appropriate output signal. This situation may occur if the main processor gets faulty or the controller has no supply voltage.

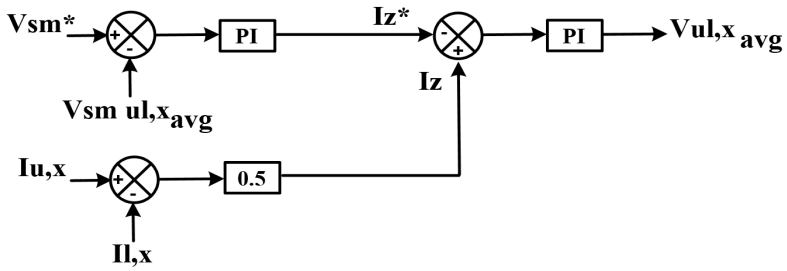

Figure 3. A Block Diagram of the Averaging Controller.

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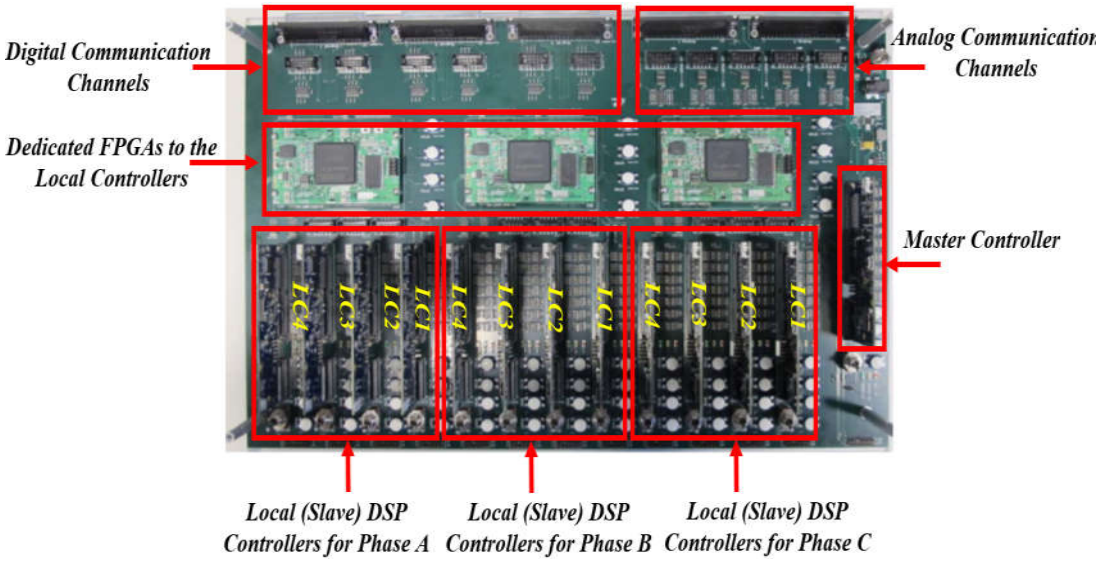

Figure 4. Modular Distributed Fault-tolerant Controller.

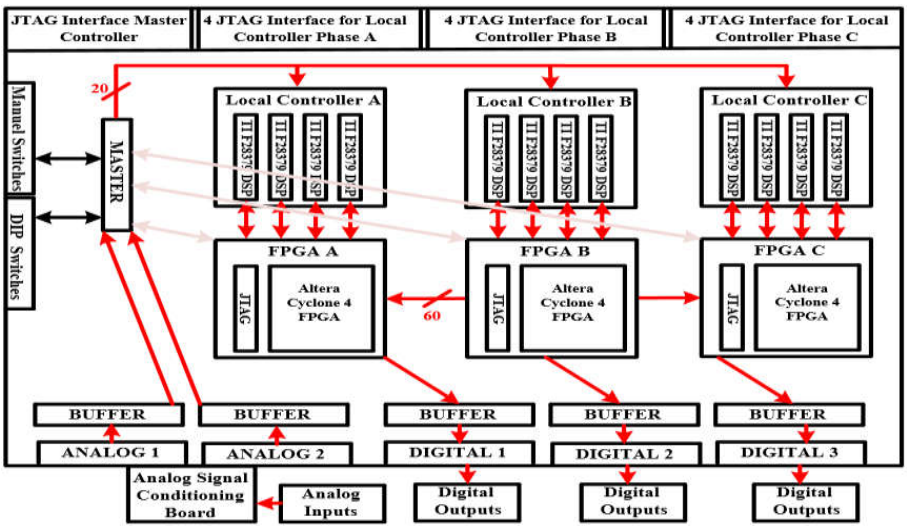

Figure 5. A Block Diagram of the Controller.

Suppose such a case occurs and the output signal comparison of the adjacent controllers are not the same. In that case, the fail-over signal gets high, and one of the adjacent controllers replaces the faulty main controller. If both the adjacent controllers are faulty based on the health status check seen in Fig. 7, then there is no available controller to take care of the SM. In such cases, the SM will be bypassed. The scope of this paper investigates the conditions under local controllers' failure. Hence, bypassing the SM through the controller will be considered in another research paper.

The master controller is a critical element in this control structure because it controls AC voltage, phase circulating current, and capacitor voltage averaging for each phase of the MMC. The master controller is responsible for regulating output voltage through the active and reactive current based on the modulation signal, as seen in Fig. 8. SM capacitor voltages are averaged based on the sensor reading of each phase to regulate the average voltage of each converter leg. On the other hand, each local controller is responsible for balancing the capacitor voltages and generating the PWM signals for the switches [22]-[24]. Besides, each local controller manages the capacitor voltage balancing as in Fig. 9. Then, the output of the balancing controller is fed into the PWM generation block.

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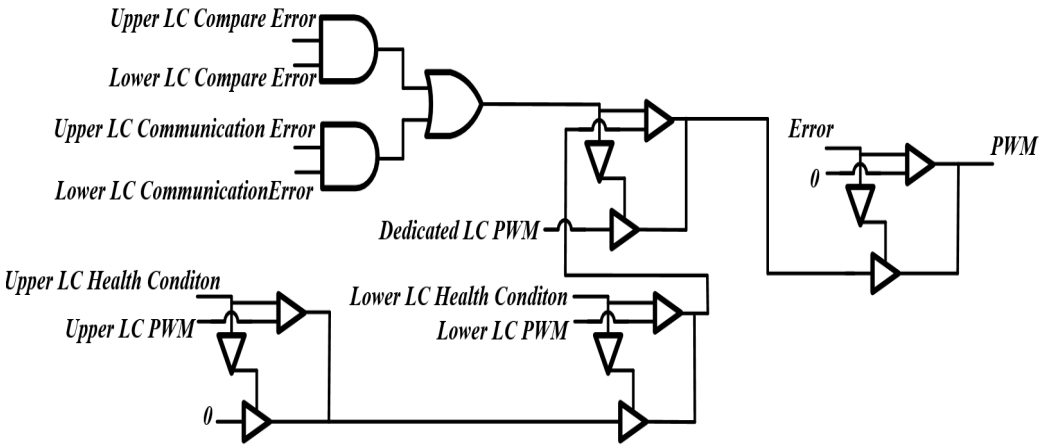

Figure 6. SM Controller Failure Detection based on Result Comparison.

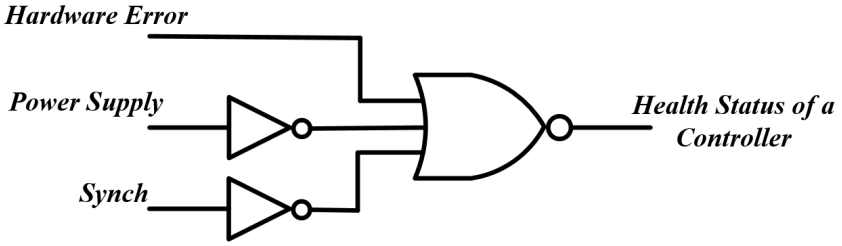

Figure 7. Controller Health Status Check Logic Diagram.

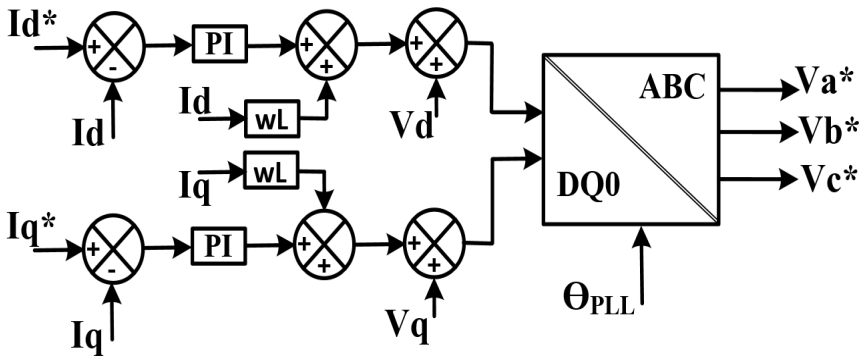

Figure 8. A Block Diagram of the Voltage Controller.

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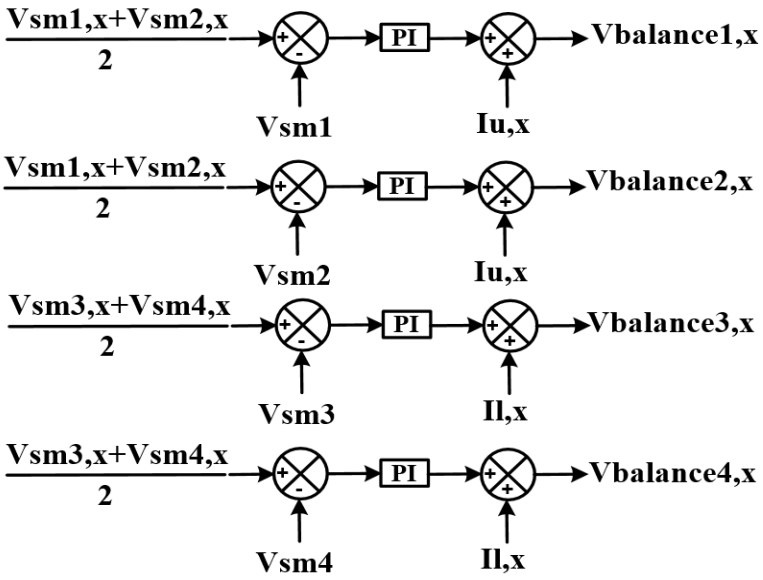

Figure 9. A Block Diagram of SM Capacitor Voltage Balancing Controller.

4. Experimental Verification

A three-phase MMC prototype with two SM per arm is designed to test the controller, which has four local controllers per phase. The test setup is developed to validate the modular fault-tolerant distributed controller under steady state and local-controller failure conditions. Each phase leg of the MMC prototype is connected to a constant DC power supply, an N5700 series 150V, 10A, 1500W from Keysight Technologies. The DC source provides stable output power, and the MMC is operated in an inverter mode. The AC side of the porotype is connected to an inductive load, represented by a 2.5 mH inductor and 20Ω resistor. An illustration of the experimental setup can be seen in Fig. 10, and a photo of the test setup is shown in Fig. 11.

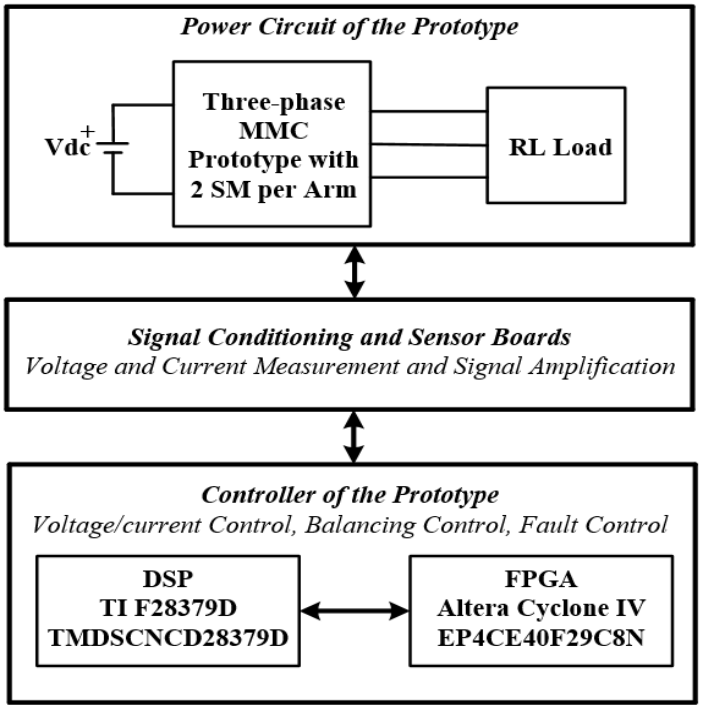

Figure 10. An Illustration of the Test-setup.

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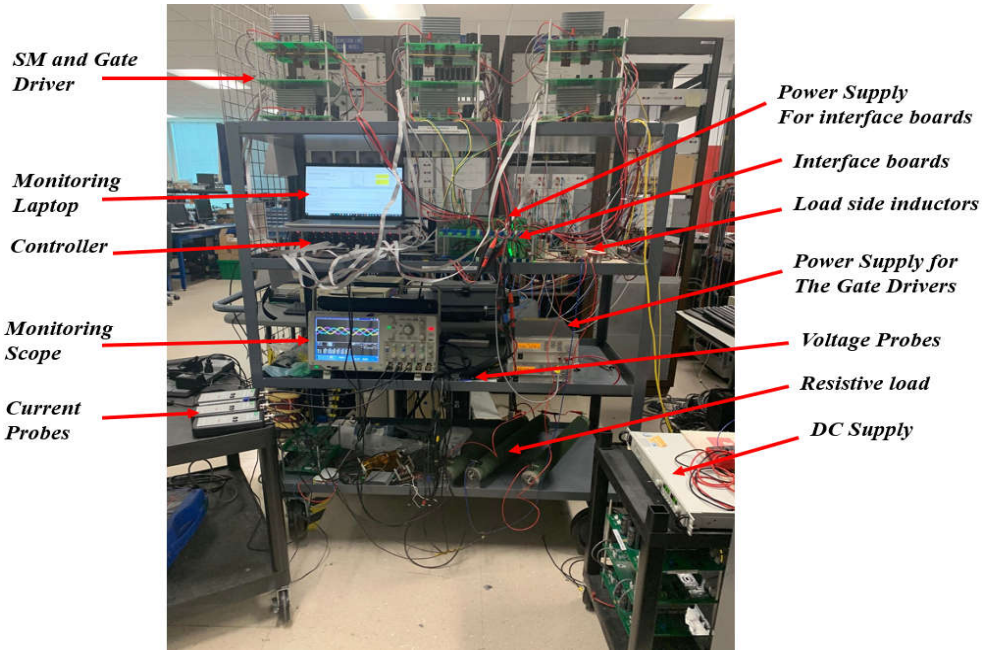

Figure 11. A Photo of the Test-setup.

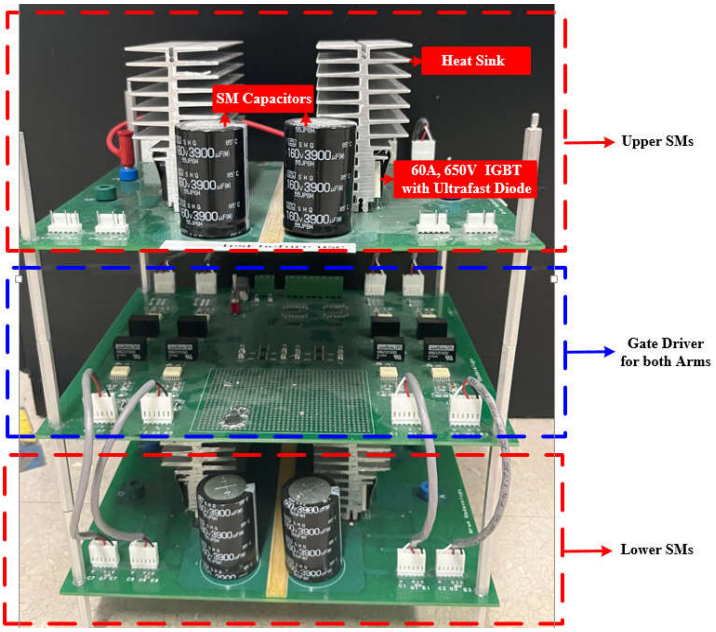

Figure 12. A Phase Leg of the MMC Prototype.

A list of parameters of the prototype can be found in Tab. 1. A photo of the MMC phase module can be seen in Fig. 12; each phase leg has four SMs and an isolated gate driver. Each HBSM has a 60 A, 650 V field stop trench gate IGBT (STGW60H65DRF) with an ultrafast diode attached to a heat sink and a 3.9mF snap-in capacitor. LEM ® sensors, placed on a single board, are used to measure the signals from the SMs. The measured signals are fed into a signal conditioning board, seen in Fig. 13, to filter the analog signal and amplify the useful signals for the controller cards. Fig. 14 shows the experimental results for the SM capacitor when the DC voltage is changed from 0 p.u to 0.8 p.u. It can be seen that all four capacitors share the DC bus voltage almost equally. The capacitor voltages' summation is not quite equal to the DC link voltage due to the voltage drop on the relatively large arm inductor (1mH), resulting in $\mathbf{2}\boldsymbol{V_{cx}}$ based on (1) and (2). The DC link voltage is increased to 100V in Fig. 15. The load current and the capacitor voltages of

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the upper SMs can be seen accordingly. Capacitor voltages of the SMs show that the balancing controller is effective.

Table 1. System Parameters.

DC Voltage	80 V -100V	Number of SM per arm	2
AC Frequency	60 Hz	Capacitor Ref. Voltage	50 V
Switching Frequency	10 kHz	SM Capacitance	3.9 mF
Load Inductance	2.5 mH	Load Resistance	22 Ω
Arm Inductance	1 mH	IGBT at $T_c = 25^oC$	60 A, 650V

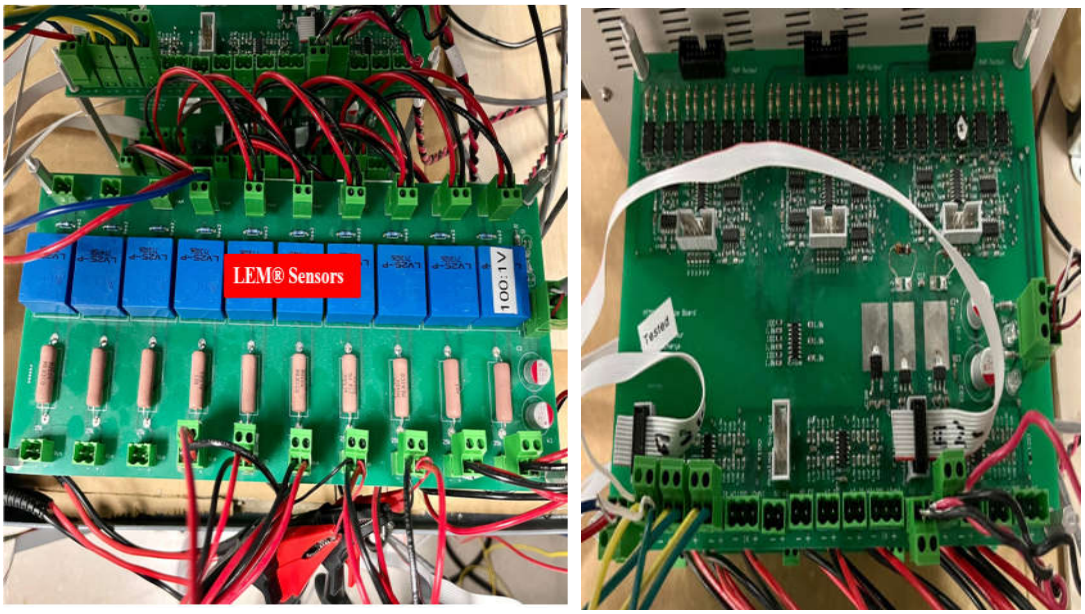

Figure 13. Sensor (left) and Signal Conditinioning (right) Board of the MMC Prototype.

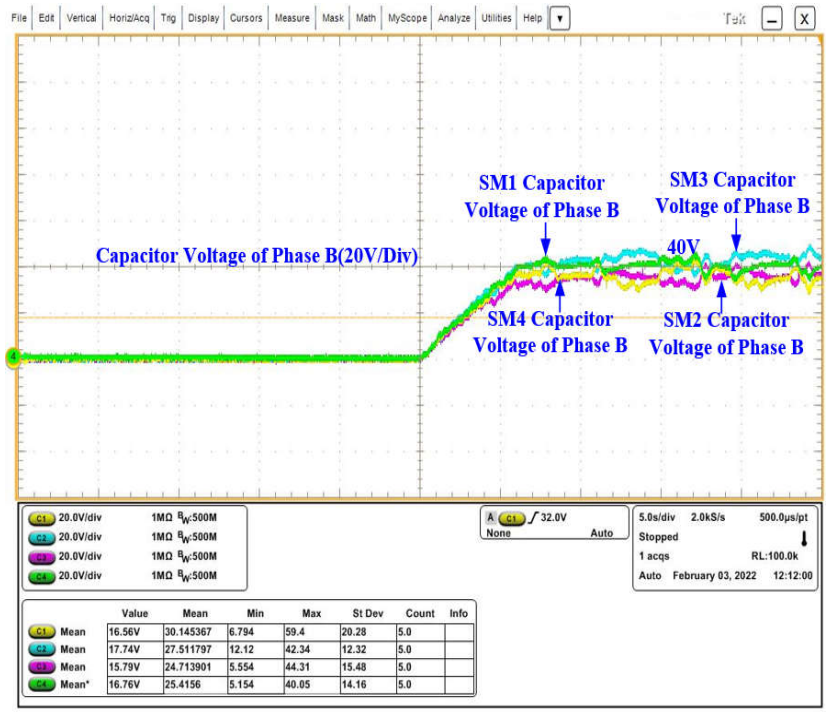

Figure 14. Dynamic Performance of Phase B when the Reference Value of the DC Voltage from 0 PU to 0.8 PU.

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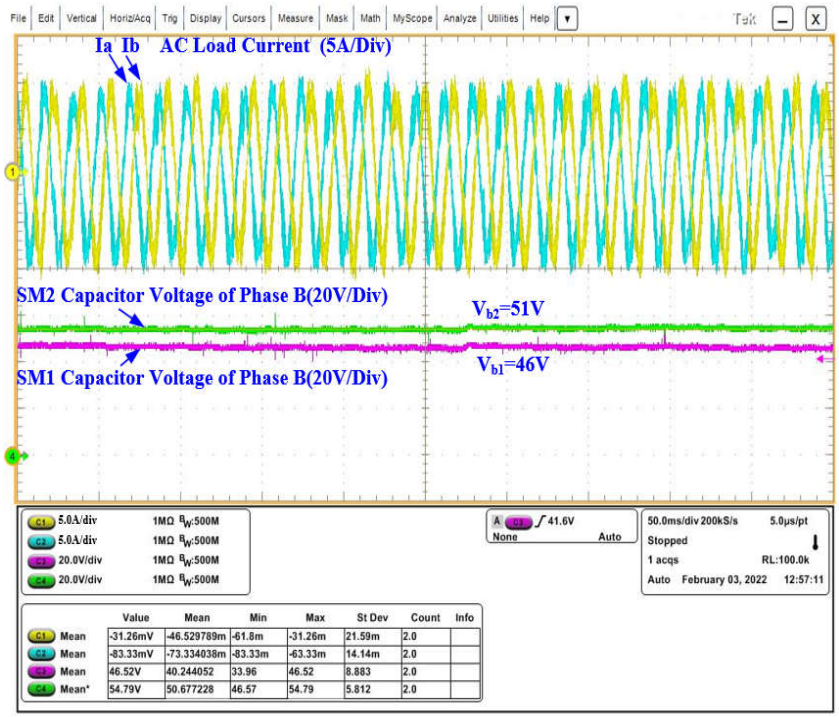

Figure 15. AC Curent and SM Capacitor Voltage at 100V DC link.

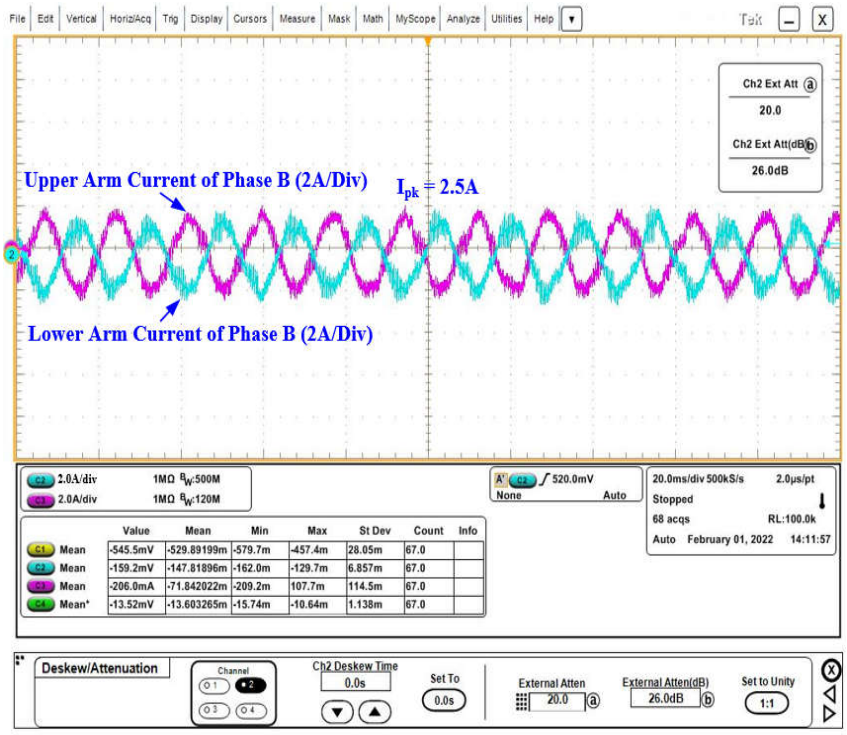

Figure 16. Parameters of Phase B under Steady State.

TThe main scope of this paper is to test the controller capability under LC failure. Hence, the prototype is operated at 80V DC link voltage to test the scenarios. The arm, load, circulating current and the SM capacitor voltage can be seen in Fig. 16 and 17 during the steady state. The circulating current controller is disabled, and the dominant second-order harmonic can be seen in the circulating current. Besides, switching frequency circulating current is observed in the circulating current. As seen from the SM voltages, the balancing controller effectively balances the capacitor voltages.

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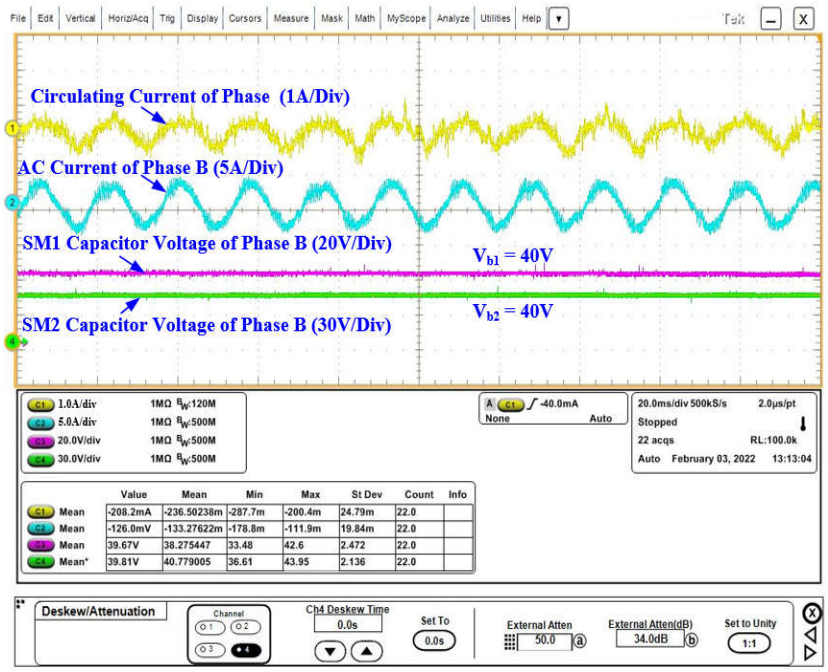

Figure 17. Parameters of Phase B under Steady State.

Table 2. The Take-over Chart during Fail-over Condition

LC1	*LC2*	*LC3*	*LC4*	*System Status*
Failed	Takeover	No Change	No Change	Up
Takeover*	Failed	Takeover*	No Change	Up
No Change	Takeover*	Failed	Takeover*	Up
No Change	No Change	Takeover	Failed	Up
Takeover	Failed	Failed	Takeover	Up
Failed	Takeover	Takeover	Failed	Up
Failed	Takeover*	Failed	Takeover*	Up
Failed	Failed	No Change	No Change	Down
No Change	No Change	Failed	Failed	Down

**the dedicated phase FPGA decides which LC takes over based on the health status*

The LC of the second SM (LC2) failed by cutting the supply voltage. The controller's health is immediately reported based on Fig. 7 to manage the SM through the adjacent controllers. The circulating current and the capacitor voltage momentarily respond while the adjacent controller takes over the SM2. Due to the dynamic response of the controller, there is a rise in capacitor voltage during the take-over, which is less than 5% of the rate value seen in Fig. 18. The circulating current shows a high magnitude due to the time delays involved with regards to the detection and switching of control inputs from failed DSP to healthy DSP. This process takes around 500 μsec. The FPGA allocated for the DSP failure detects the failure based on the loss of communication signal from the DSP. Since the synchronization check occurs once every control cycle, there is a detection delay of one control cycle. Besides, there is a delay associated with deciding the available healthy LC for the particular SM. Therefore, a loss of control occurs due to the delays and a high magnitude of circulating current is observed as a result.

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Although there is a transition delay, the take-over process is still fast enough to observe no effect on the load current and the SM capacitor voltage balancing. Similarly, two LC-failure are tested simultaneously by cutting the supply voltage. The health status of the controllers is reported, and the failure detection occurs within 500 µsec. The process of two LC failures is the same as in the previous case, but the number of control delays is increased. As a result, higher oscillation is observed in the circulating current in Fig. 19. Still, the controller can sustain the SM capacitors with two healthy LCs. There is a rise in capacitor voltage during the take-over, which is around 5% of the rate value due to the dynamic response of the controller. The take-over process repeats itself until a healthy LC is available to take over an SM. Tab. **2** shows the algorithm of the take-over process during a fail-over condition.

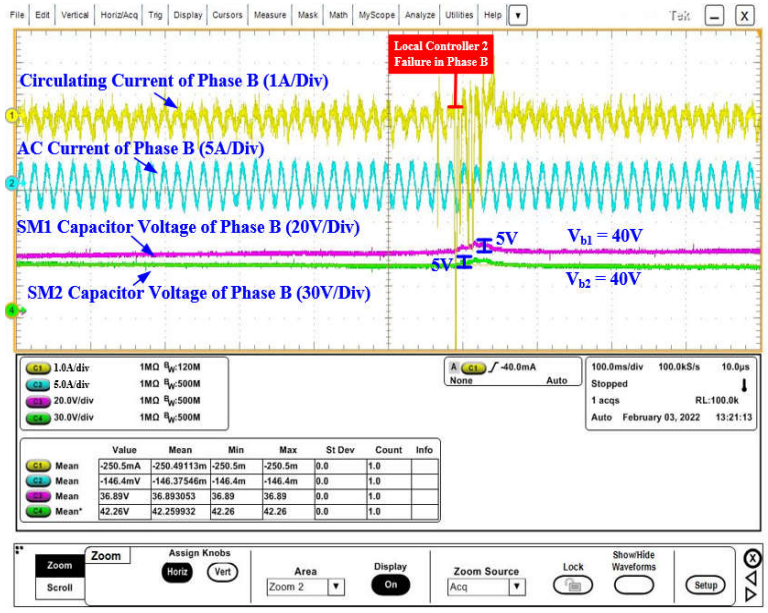

Figure 18. System Parameters under Failure of One Local Controller.

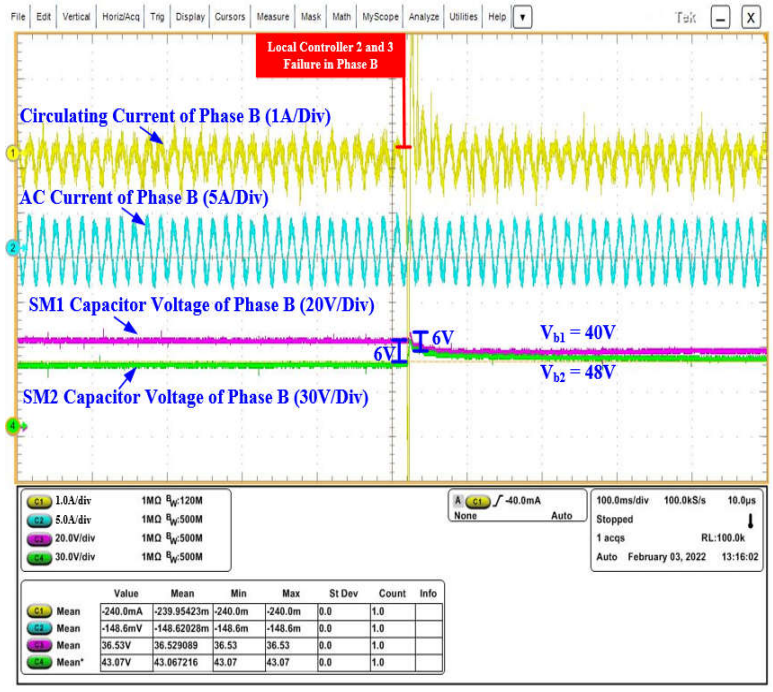

Figure 19. System Parameters under Failure of Two Local Controllers.

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As can be seen, the controller can sustain the operation under any one LC failure. Further, the controller can sustain the operation under two LCs failures as long as the failures are not located in the middle and the corner LCs. For instance, the controller is still operational if LC2 and LC3 fail because LC1 and LC4 can take over the faulty LCs. However, if LC1 and LC2 fail simultaneously, the system must shut down. The reason is that there is no available neighbor controller to take over the LC1 in this case. The experimental results are verified with the Opal-RT real-time simulator, as seen in Fig. 20. A Control-Hardware-in-Loop (C-HIL) environment is developed with a modulation index of 0.92 using the same modular distributed fault-tolerant controller. The same power circuit is modeled in the Virtex 7 FPGA using MATLAB Simulink ®. Due to the high switching frequency operation of the controller, the required simulation time-step is less than 1 µs. Although the time-step around 1µs satisfies the communication, this will significantly increase the simulation time. Therefore, power electronics components are chosen from the RT-event® library to reduce the simulation time step and overall time. The C-HIL setup aims to test the controller capability before testing the hardware setup. The behavior of the current and voltages are compared and validated with the hardware result. The circulating current observed in the OPAL-RT result is more significant than in the hardware result. This is because the circulating current is fed to the controller during the OPAL-RT simulation and calculated as quantity using signals sampled in the OPAL-RT system's CPU. In the prototype, the circulating current is measured through the arm currents using LEM sensors for each phase, but it is not possible to place a current measurement sensor in OPAL-RT that directly measures the circulating current. Due to this limitation, the arm currents are measured from the simulation in the CPU and processed to calculate the circulating current based on the discrete-time simulation. This process has communication delays between the simulation FPGA and the CPU. Therefore, the circulating current in the OPAL-RT results can not be correlated directly to the measurement result because it is not a direct measurement. Yet, the aim is to compare the behavior of the current under LC failure. Fig. 21 shows phase B's load, circulating current, and upper SM capacitor voltages. This figure validates the experimental results shown in Fig. 17 at

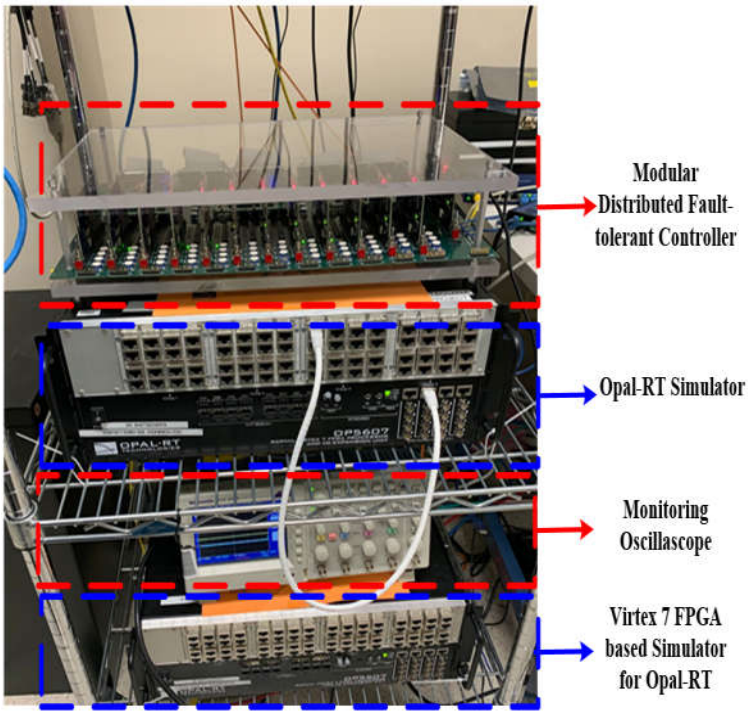

Figure 20. Opal RT and the Controller HIL Setup

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80V DC link voltage.. Similarly, Fig. 22 shows the same result pattern as Fig. 18 when LC2 is hard-failed. Lastly, Fig. 23 validates the experimental results under the failure LC2 and LC3, as seen in Fig. 19.

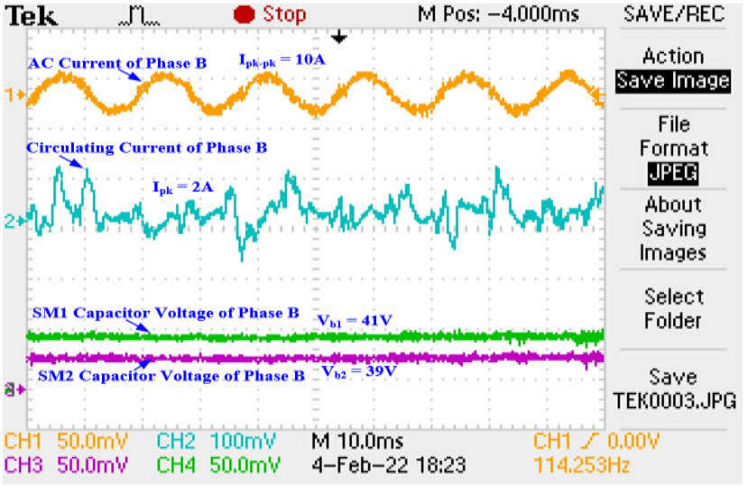

Figure 21. Result Validation of Fig. 17 with Opal-RT.

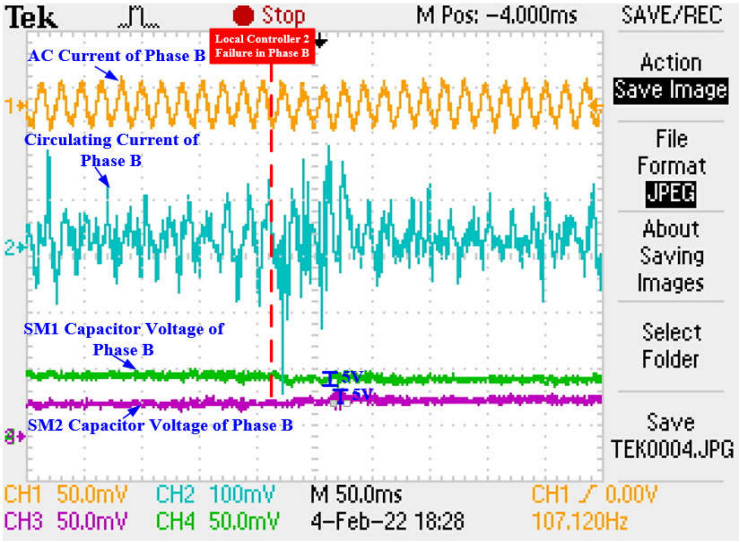

Figure 22. Result Validation of Fig. 18 with Opal-RT.

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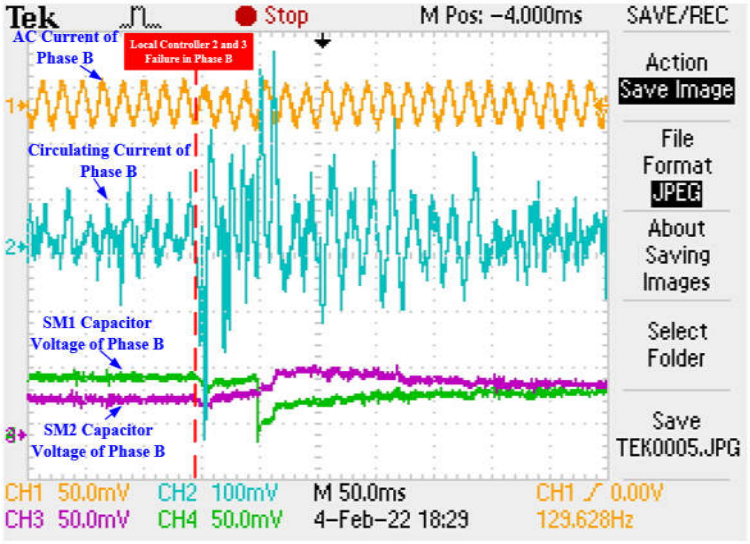

Figure 23. Result Validation of Fig. 19 with Opal-RT.

5. Conclusion

The MMC topology is one of the promising candidates for medium and high voltage applications. One of the reasons is that an MMC can generate almost a sinusoidal voltage with several hundred series connected SMs per arm. Besides, the number SMs can be easily modified, and the rated power can be redefined. However, the controller of an MMC should be modified accordingly, but it might be challenging if the MMC is controlled with a centralized control structure. Modifying a centralized controller for hundreds of SMs is difficult as all the data is sensed and computed in a large processor.

On the other hand, a distributed control structure is more flexible to modify than a centralized controller. The reason is that a distributed controller has multi-control points such as master and local (slave) controllers. Hence, modifying a master or the local controllers is relatively easier than modifying a master controller with hundreds of control lines. Besides, distributed controller significantly eliminates the single point of failure compared to a distributed controller. On the other hand, the failure risk of the controller increase due to the increased number of controller. However, a distributed controller can be resilient if programmed accordingly. On the other hand, the local controller imposes more sampling delays and the oscillatory system response as opposed to a centralized controller. Especially, a fault-tolerant distributed controller can experience more oscillatory response during fail-over and take-over processes.

This paper implements a distributed modular fault-tolerant controller for a scaled laboratory MMC prototype. A CHIL environment with the Opal-RT is also utilized to validate the hardware results. The results show that a distributed controller can sustain the MMC operation even under local controller failure. Due to the control and communication delays, high oscillation is observed in the circulating current. It is worth mentioning that the oscillation magnitude can be decreased with circulating current suppression control. Despite the delays, the distributed control scheme can be feasibly employed in MMC systems with additional harmonic compensators.

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