 doi:10.20944/preprints202209.0312.v1

Article

ULP Super Regenerative Transmitter with Digital Quenching Signal Controller

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Abstract: This paper demonstrates an on-off keying (OOK) super-regenerative quenching transmitter operating in 402- 405MHz MICs band applications. To reduce power consumption, the transmitter is controlled by a novel digital quenching signal controller that generates a digital control signal to start transmitter operation when a baseband signal is input to the transmitter. The digital signal controller consists of an envelope detector, a comparator, and a quench timer designed using a state machine to synchronize the operation between the digital controller and the input baseband signal. The transmitter consists of a Colpitts oscillator operating in double operating frequency followed by a frequency divider by 2, this configuration reduces system area and improves phase noise and signal spectrum. The proposed transmitter is implemented using UMC 130nm CMOS technology, and a 1.2V supply. Simulation shows that the proposed transmitter can meet MICS band mask specifications with data rates up to 1Mbps and total power dissipation of 537uW.

Keywords: quenching transmitter; super-regenerative transceiver; MICS band; quenching signal controller; Colpitts oscillator; TSPC divider

1. Introduction

Recently, the demand for Ultra-low power (ULP) transceivers for implantable devices grows dramatically with different solutions for energy consumption reduction and optimization [1-4]. In 1999, the FCC published the medical implant communication service (MICS) around 400 MHz, to provide a good compromise between device size and penetration depth into living tissue, while concerns about interferences are relaxed [5]. To further reduce the risk of interference maximum effective isotropic radiated power (EIRP) and bandwidth are limited to −16dBm and 3MHz, respectively. Thereby, out-of-channel emission has to be −20 dB [6-7].ULP, typically means an average power consumption in the range of sub-mW, considering MICS applications to allow for energy harvesting operation using on chip antennas (operates in MMwave frequency ranges such occupied area is very small compared with complete system) [7,8]. ULP transceivers are required for implantable sensors and surgical procedures in the sub-mW supply operation for usage of energy harvesters and wireless power transfer modules [9,10]. To achieve ULP operation, on-off keying (OOK) combined with super-regenerative reception (SRR) is often used in ULP MICS transceivers [11-16] with very low energy per bit ratios from 4.2nJ/b down to 0.18nJ/b [15,16]. The main operating principle is to switch off the transceiver when no data transfer occurs. In this paper, a quenched transmitter as a part of a fully regenerative OOK transceiver is designed in standard UMC 130nm CMOS technology and can be used with an already designed low power OOK regenerative receiver. Various works of SR technique are presented, as the use of digital-to-analog quench controller, phase locked loop frequency synthesis and low efficiency envelope detectors [17] which increases power consumption and circuits' complexity. A novel digital quenching signal controller is proposed to control the operation periods of the transmitter, which enables the oscillator - the main block in the proposed transmitter- to switch on only during data

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transfer and switch off during idle operation. The proposed controller consists of a state machine determines the oscillation period start up and controls a quenching timer. The state machine is controlled using a comparator digital signal derived from an envelope detector for the transmitted signal. The paper is organized as follows. Section 2 describes block diagram of the complete system. Section 3 demonstrates the quenched transmitter building blocks and their simulation results. The design concept of the proposed quenching signal controller and the state machine is in section 4. Complete system simulation results are reported in section 5. Finally, conclusion is drawn in section 6.

2. Proposed Regenerative Transmitter Block Diagram

The block diagram of the quenched transmitter is shown in Fig.1. It contains an oscillator turned on and off by enabling and disabling its bias current Ibias. This is controlled by multiplying the output signal enBias from a quench generator with that of the OOK input sBB in digital domain. Then, the result is converted into the bias current. Hence, if enabled by the quench control, the bias current is only available during a high state of the baseband signal. As the bias current is activated, an oscillating output voltage is rising up. The oscillator outputs a signal at around 800 MHz, which is fed through a buffer followed by a dynamic frequency divider that creates the desired frequency of about 400MHz. To control the quenching signal the oscillator's output runs through an envelope detector first. By comparing its output to a reference signal Iref, a started oscillation is indicated. Based on this 'detection signal' output from the comparator, combined with a signal from a quench timer, a state machine decides whether the bias current is enabled. This ensures synchronization between quenching and the input bit pattern. Furthermore, the state machine enables the divider operation, once the oscillator has settled. Working at twice the frequency offers usage of integrated inductors having nearly twice the quality factor and smaller area within this frequency range, which results in reduced power dissipation. Furthermore, it isolates the oscillator from a power amplifier (PA), thus suppressing the effect of injection pulling [18]. A power amplifier is not included in this work, but considered as a load. In the following sections, the implementation of the signal path architecture is presented first. Afterwards, the building of the feedback path generating the quenching signal are worked through.

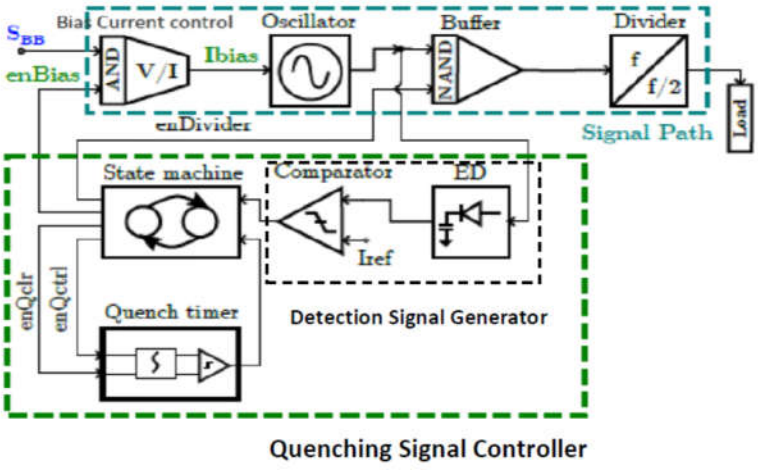

Figure 1. Block diagram of Quenched transmitter with digital Quenching signal controller.

3. Signal Path Circuit design

Signal path block consists of three parts, bias current control circuit, Colpitts oscillator followed by a NAND buffer and a Master- Slave true single-phase clock (TSPC) frequency divider. In this section circuit diagram for each block is explained.

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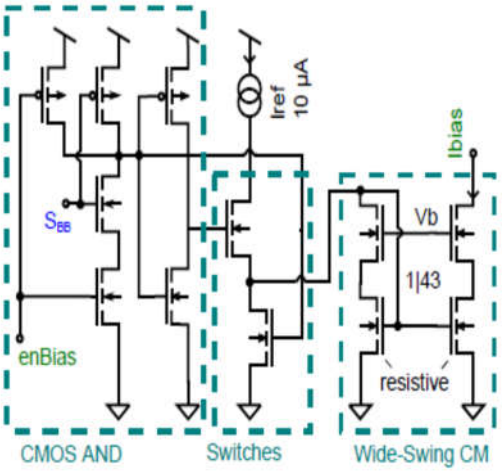
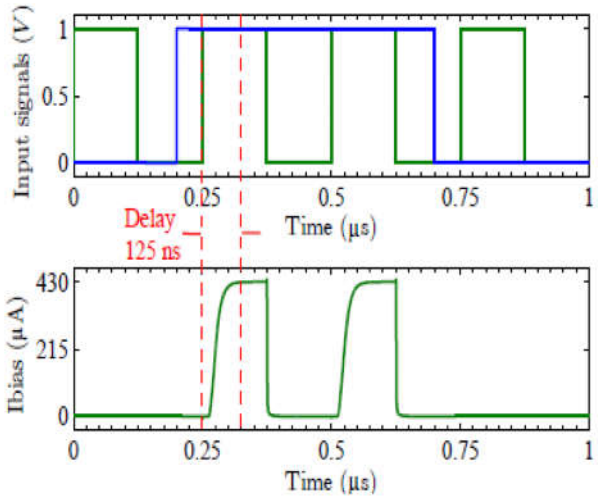
3.1. Bias Current Control

The bias current control shown in Fig.2(a) provides the bias current Ibias for the quenched oscillator. The bias current is fed to the oscillator only if enabled by two control signals applied to an AND gate. One signal is provided from a state machine enBias, another from the digital baseband signal sBB. The working principle is shown with simulated waveforms in Fig.2(b). If both inputs are driven to high state a reference current is allowed to be mirrored up as the oscillator's bias. Otherwise, no current is applied to the oscillator.



(a)



(b)

Figure 2. a) Circuit diagram of the bias current control logic, (b) Transient simulation of the switched bias control with input signals enBias (green), sBB (blue) on top and the output bias current Ibias at bottom.

3.2. Oscillator

To generate the local oscillator signal, Colpitts oscillator in common gate configuration shown in Fig.3 is used. It provides large output voltage swings with good phase noise performance. Quenching is made possible by a controlled bias current. By setting Ibias below the required for starting an oscillation the oscillator is quenched. The design considerations for starting the Colpitts oscillator is given by [18]

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$$g_m R_p \geq \frac{(C_{top}+C_{bot})^2}{C_{top}.C_{bot}} \qquad (1)$$

As quality factor QL of integrated inductors is small, Rp is dominated by the inductor, as Rp≈Lω0QL [18]. For ω0 = 2τ •400Mrads−1 an inductance of 22 nH with QL ≈ 5 is provided -by the UMC130nm CMOS technology- yielding Rp≈276Ω. By doubling ω0 to 2τ 800 Mrad.s−1, an inductance of 2 × 11 nH is used with QL is increased. As a result, Rp reaches 1k roughly. Thus, the required gm and Ibias for a set swing are reduced. Simulated waveform is shown in Fig.4.

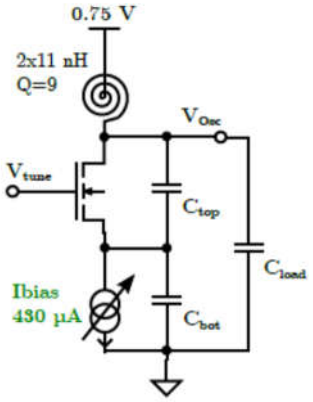

Figure 3. Circuit architecture of the Colpitts Oscillator.

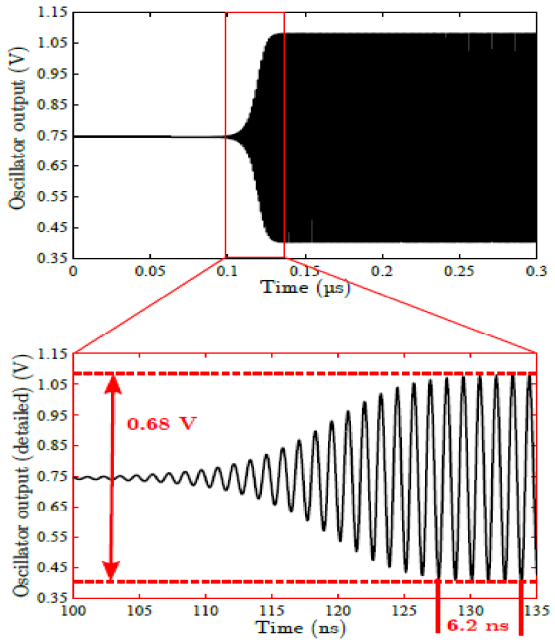

Figure 4, Simulated transient characteristic of the Colpitts oscillator.

3.3. Frequency Divider

The frequency divider is necessary to get the desired carrier frequency of about 400MHz from the local oscillator, which operates at 800MHz. A TSCP divider architecture shown in Fig.5 exploits the master-slave configuration presented in [19]. The master-slave architecture prevents glitches, which would occur at the output for the traditional flip-flop. To prevent driving the switches of the divider by the oscillator, a CMOS NAND gate serves as a driver. One input comes from the oscillator, the other from a digital logic. A NAND logic is necessary to fully shut off the driver. Otherwise, in absentia of an AC signal, the DC voltage from the oscillator (of 0.75V) would cause the driver to consume static

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power. The simulated waveform of the divider for an ideal input oscillation is presented in Fig. 6(a). Once the divider is activated, the task dividing the input frequency by two is completed even for an input amplitude of 12% below the nominal value achieved by the Colpitts oscillator. The simulated spectral characteristics if combined with the designed oscillator are given in Fig. 6(b) with the input frequency at 800MHz is sufficiently suppressed by −30dB and frequency spurs are well below −80 dB relative to the carrier of 400MHz. To give a measure for the power consumption the individual stages of the divider are regarded as inverters driven at 400MHz. Additionally, the switches driven by the NAND gate at 800MHz are considered. The average dynamic power consumption of a digital inverter is calculated by

$$P_{avg} = V_{DD}^2 C_{load} f \qquad (2)$$

Assuming a capacitive load of 100fF, power consumption of 85µW for driving the switches and respectively 123µW for the divider stages is estimated, which in total is about 0.2mW.

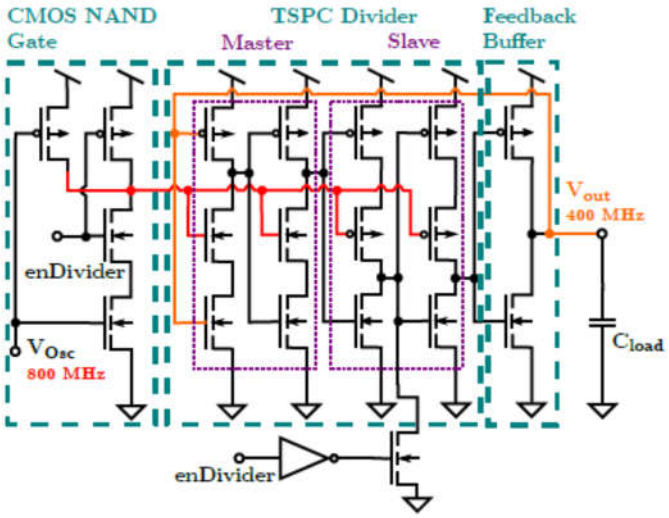
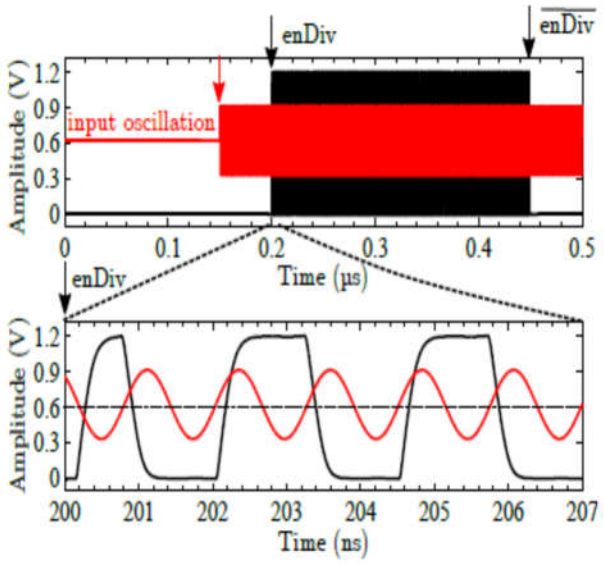


Figure 5. Dynamic divide by two frequency divider with controlled input buffer.



(a)

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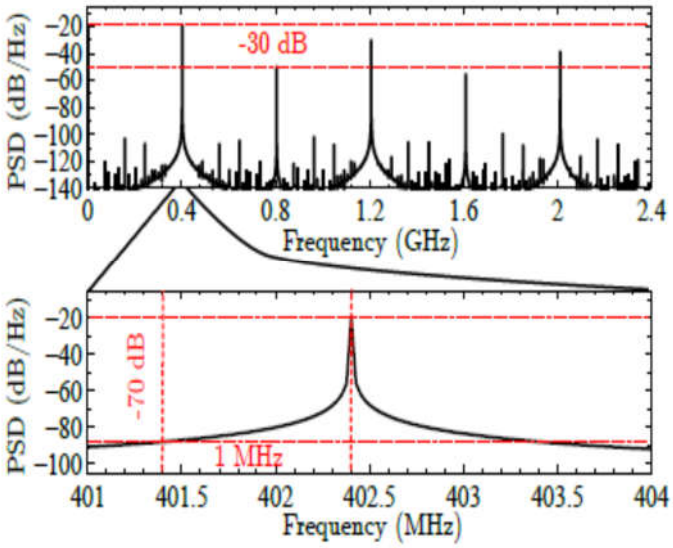

(b)

Figure 6. (a) Simulated time response of the frequency divider, (b) Power spectral density (PSD). plot of the combination of divider and Colpitts oscillator (N = 2^{20} resolution bandwidth 25.1 kHz).

4. Quenching Signal Controller

The quenching signal controller deals with generating the quenching signal input to the oscillator as shown in Fig.1. Since the quenching is controlled with digital signals, the analog output of the oscillator is transformed into digital domain. In order to obtain this, an envelope detector followed by a comparator is used. These two circuits indicate a started or quenched oscillation, by generating a detection signal. Depending on their output a state machine starts the quenching period or not. For a defined quench cycle, a quench timer is used which is part of the feedback for the state machine.

4.1. Envelope Detector

The envelope detector (ED) establishes the first part by means of generating an oscillation 'detection signal'. As indicated by its name this device outputs a signal depending on the envelope curve of the input signal, while the high frequency oscillation is removed. Hence, the following stages have to process low frequency signals only, thereby reducing their power consumption. The schematic of the implemented ED is presented in Fig.7. It contains an input transistor biased as a diode and a filter capacitor. The diode only lets through positive voltages relative to the input common-mode voltage (0.75V) and suppresses the negative ones. So, it works as a half-wave rectifier. The rectified input voltage causes a current successively charging the filter capacitor Cf. Since the charging process is faster than the discharging by the bias circuit the output voltage Venv rises. So, it performs like a first-order sample-and-hold which is similar to a first order low-pass filter. Considering the suggested design, the filter pole frequency P is at [20]:

$$P \approx \frac{gm_{diode}}{C_f} \quad (3)$$

With gmdiode = 130 µS. Cf of 0.5pF the pole frequency is 260MHz. With an input frequency –from oscillator- of 800MHz below the filter frequency, a first-order low-pass the input signal is suppressed. Since the fundamental of a halfwave rectified sinusoidally is only half of its amplitude, another −6 dB is obtained in a steady-state. Fig.8 shows simulation of the ED, with a charging time of 2.9ns, discharging time 23ns, and voltage ripples of 10mV. The delay caused by the discharge time of 23 ns is not very critical, because the oscillator requires about 100 ns for the start-up.

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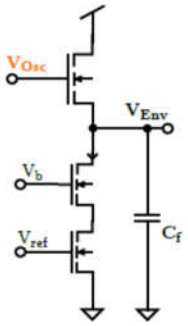
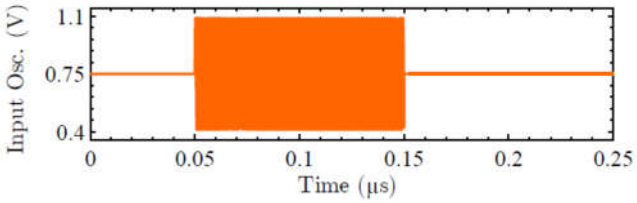
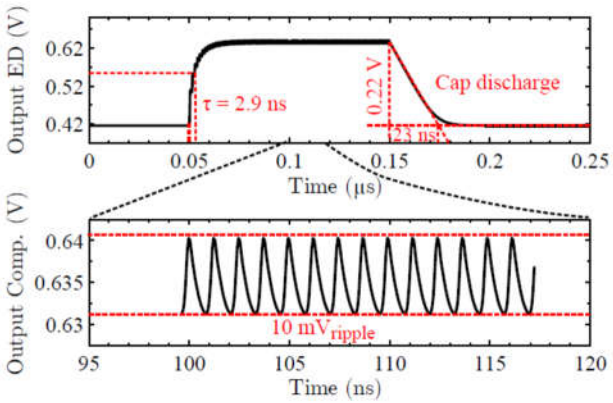


Figure 7. Implementation of the envelope detector.



(a)



(b)

Figure 8. (a) Oscillator Input signal, (b) ED output waveform and voltage ripple.

4.2. Comparator

The comparator is used to transform the output voltage of the envelope detector to a usable voltage for the digital control logic. Because the signal levels of the envelope detector are too low to sufficiently driving conventional comparators, the architecture shown in Fig. 9(a) is used. Here the output voltage of the envelope detector Venv is converted to a current, which is mirrored and compared to a reference current. If the resulting current is higher than the reference the output is driven low, otherwise the output remains at high state. Since currents are compared it is called a current comparator. However, to somehow get a logical meaning an inverter follows the output. Hence, an increased voltage of the envelope detector results in a high state at the output. Moreover, the output is more 'hard switched' giving a more defined logic state. For ensuring the detection of a started oscillation, the switching point is chosen at the minimum value provided by the envelope detector, a detection point is compromised to 0.45V. The dc characteristic of the comparator is presented in Fig.9(b).

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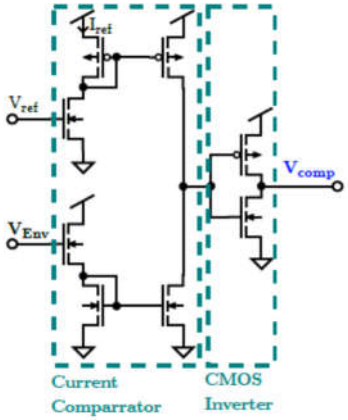
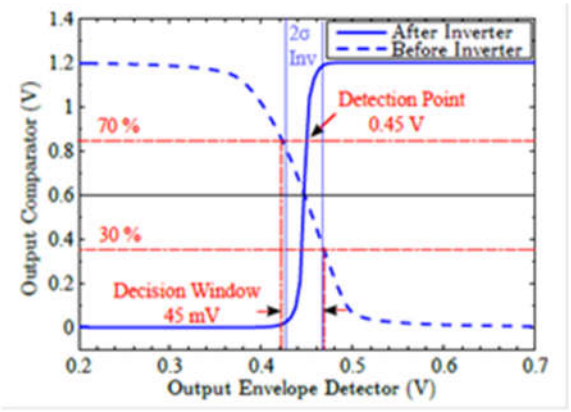


(a)



(b)

Figure 9. (a) Schematic of the current comparator, (b) Current comparator dc characteristic.

The transient behavior of the current comparator, while connected to the envelope detector, is shown in Fig.10. It can be seen, that the decision point is shifted in the time domain due to some delay introduced by parasitic capacitances. Further, the dead-time is extended from 23 ns (Fig. 8) to 35ns, but is still not critical. Performing a Monte-Carlo simulation for 200 runs with envelope detector and comparator connected, results in 100% detected oscillations but seven out of 200 are false detections, which gives 96.5% yield. Hence the minimum dc level seems to be more critical. To solve this problem, the nominal detection point is adjusted to a higher value of 0.55V. The simulated static power consumption is 11µW if no oscillation is detected (output low) and respectively 26µW in case-of a detected oscillation (output high).

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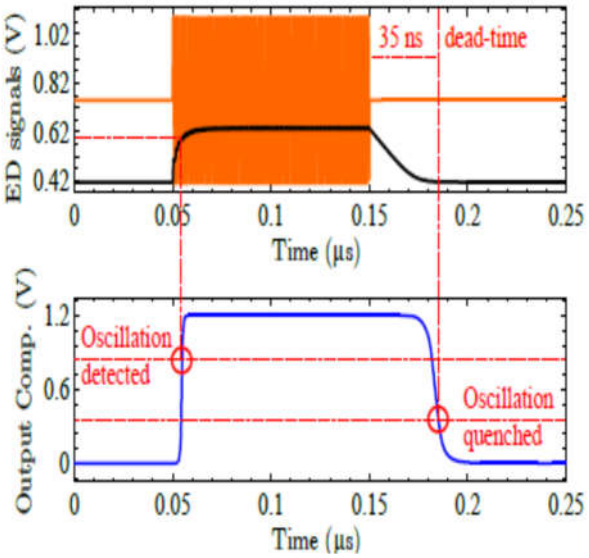

Figure 10. Transient behavior of the Envelope Detector and the comparator for ideal oscillator input.

4.3. Quench Timer

The quench timer determines the duration of the quench period as well as the on-time of the oscillator but becomes only active if an oscillation was detected and is controlled by the state machine. Thus, the quench timer outputs two states. First, the timer is in the quench period and secondly, the timer is in sample or 'allow oscillation' mode. In turn, the current state is fed back to the state machine, which decides whether the timer is reset or its state is changed. To generate these two periods the circuit shown in Fig.11(a) is used. A current source charges or discharges a capacitor depending on the state of the input signal enQctrl. If enQctrl is low the capacitor is charged and discharged otherwise. The charging is sensed by a subsequent Schmitt-Trigger, as long as the capacitor voltage is above a lower threshold, the output of the Schmitt-Trigger enTimer is low. Once the lower threshold is hit the output switches to high and vice versa for an upper threshold voltage. Whether the capacitor is charged or discharged depends on the output signal which is processed by the state machine giving the input signal enQctrl, hence the quench timer operates in feedback. But basically, discharging occurs during sampling mode and charging during the quench period. To provide the same initial conditions for each cycle of sampling and quenching a timer reset is available, which is controlled by the state machine, too. Moreover, the timer reset is enabled if nothing is to do. Thus, the quench timer is waiting in sampling mode with the output enTimer at low. To determine the duration of the sample and quench period, the system's delay times have to be considered. These are about 125ns from the switched bias control (Fig.2(b)), 100ns until the oscillator builds-up a detectable oscillation (Fig.4), and 35ns from the dead-time of the envelope detector combined with the comparator (Fig.10(a)). Adding up these values results in 260ns, which represents the nominal time of the system during the oscillator is indicated as quenched. Since sample and quench time needs to be equal to obtain a clean spectrum, the minimum time for oscillation would be 260ns as well. But this would mean the quench timer does not need a quench or charge period. Hence, the timer cycle is doubled to about 1 µs or in means of frequency 1 MHz, which also is the maximum pulse rate needed to be detected on the receiver side. Thus, the quench period is a third of the entire timer cycle. To realize this, the capacitor is preloaded to 1.2 V at the beginning of a cycle. Further, the threshold voltages are set to 0.9 V and 0.3 V. Well, to change the output from low to high the capacitor needs to be discharged from 1.2 V to 0.3 V. To switch back the output, charging from 0.3 V to 0.9V has to be done. By defining the charging current, a quarter less the discharging current, the quench period (charging) needs one third of a cycle, now. The mismatch in currents is achieved by using properly designed current mirrors within the switched current source. The idea is verified by simulation as shown in Fig.11(b).

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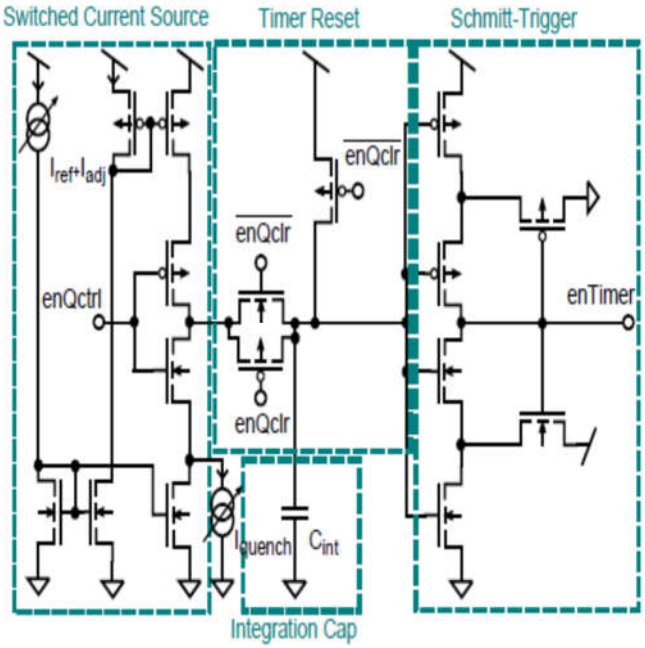
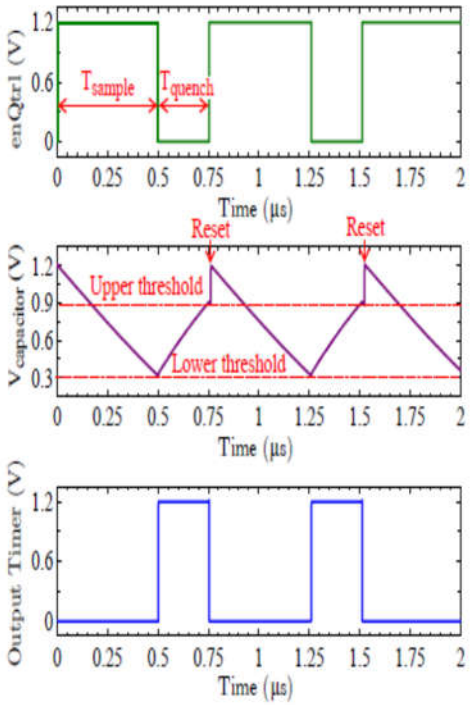


(a)



(b)

Figure 11. (a)Circuit implementation of the quench timer, (b) Simulated output waveforms of the quench timer. The quench timer is free-running by using an ideal delay element for feedback as a substitute for the state machine.

4.4. State Machine

To achieve synchronization between the start of quenching and an incoming high bit a state machine is used. This is realized by delay elements [21] that activates the quench timer as soon as a high state is detected. Besides, the state machine ensures divider start-up only once the oscillator has settled. This prevents self-oscillation of the dynamic divider due to the common-mode voltage of the oscillator. The idea of the synchronized

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quenching is shown in Fig.12. The quenching is divided into three stages. In the first phase, the state machine lies in wait for an incoming input denoted by 'Listen'. Once an input is detected, it passes over to the 'Sample' phase. This state is held until the quench timer reaches its upper limit. Hereafter, the 'Quench' phase begins and kept until the quench timer hits its lower limit. Then it goes back to 'Listen' state to check if an input is still available and if true the cycle starts again. Circuit implementation of the system state machine is not considered in this work. During Listen and Sample state the output signal for bias control enBias is set to high, which multiplied by the input signal sBB gives the signal to activate the oscillator's bias current Ibias. The state diagram is illustrated in Fig.13. The inputs T and O consider the quench timer output and 'oscillation detected' signal, respectively. The outputs B, D, Q, and C denotes the states for enBias, enDivider, enQctrl, and enQclr as presented in Fig.1. Thereby, enQctrl and enQclr stand for 'activate quench timer' and 'clear quench timer'.

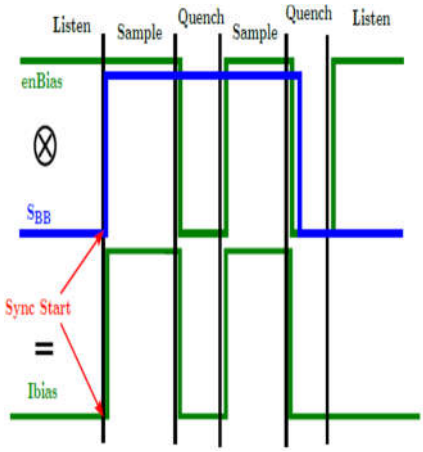

Figure 12. Sketched timing diagram to the idea of a synchronized quench control.

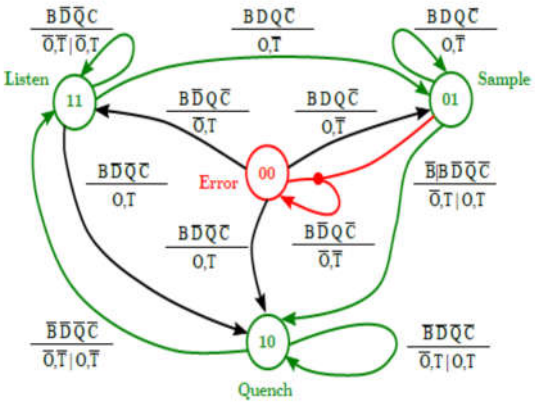

Figure 13. State diagram for quench control with inputs *T*, *O* and outputs *B*, *D*, *Q*, *C*. Normal operation is marked green. The error state indicates cut off during sampling phase at the end of an input bit (red).

The results for the outputs are calculated as follow:

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$$\begin{aligned} B &= enBias = \overline{\overline{Z_0 \wedge T \wedge \overline{Z_1} \wedge \overline{O}} \wedge \overline{\overline{Z_0} \wedge \overline{Z_1}}} \\ D &= enDiv = \overline{\overline{\overline{T} \wedge O} \wedge \overline{Z_1 \wedge \overline{Z_0}}} \\ Q &= enQctrl = T \wedge \overline{\overline{O} \wedge \overline{Z_0}} \wedge \overline{Z_1 \wedge \overline{Z_0 \wedge O}} \\ C &= enQclr = Z_1 \wedge \overline{T \wedge \overline{Z_0}} \wedge \overline{Z_0 \wedge O}. \end{aligned} \tag{4}$$

with the combinatorics of the states Z (the three phases Listen, Sample, Quench) yield to:

$$\begin{aligned} Z_{0,+1} &= \overline{T \wedge \overline{O} \wedge Z_1 \wedge \overline{Z_0}} \wedge \overline{\overline{O} \wedge Z_0 \wedge \overline{Z_1} \wedge \overline{Z_1 \wedge T}} \\ Z_{1,+1} &= \overline{\overline{T} \wedge Z_1 \wedge \overline{O \wedge Z_0}}. \end{aligned} \tag{5}$$

The block diagram of the state machine is shown in Fig.14. For simplicity of implementation its combinatorics and delay elements are implemented by minimum sized static CMOS NAND and NOT gates only. Besides, CMOS gates provide the advantage of ideally dissipating no static power. However, the number of gates is set in Table 1. The number of delay elements is chosen so that a change in state takes twice the time of the critical path within the output logic, while symmetry is respected for state paths. The remaining fourth state Error indicates a timing mismatch as described in Fig.15, which can happen if the quench cycle does not fit in multiples of the bit time. A simulated timing diagram for a random input pattern at 1Mbps is shown in Fig.15. Once the input is switching to high, the state machine starts the quench cycle, which means enQctrl is set high and goes to the sample state afterward by setting Z1 to low. As long as the input is kept at high, the alternates between sample quench and listen-state, while the quench timer is reset by enable enQclr after each cycle. The listen-state is not visible because of its short duration. Further, the bias of the oscillator enBias as well as the divider enDividier are disabled in quench state (Z1 = high, Z0 = low). The quench timer is driven into charge period with enQctrl = low during quench state, too. When the input osc detected changes back to low the state machine returns to listen-mode and waits for the next input, which will cause the cycling to start again. Note that the divider is only enabled in sample-mode (Z1 = low, Z0 = high) here. Hence, an output signal is available only during the sample-mode as well. An average and root mean square (rms) power of the state machine of 60µW and 210µW respectively, are simulated for the given input signal.

Table 1. Number of gates for state machine.

Gate	State Logic	Output Logic	Inputs	Delay
NAND	11	15	0	0
NOT	1	4	4	12

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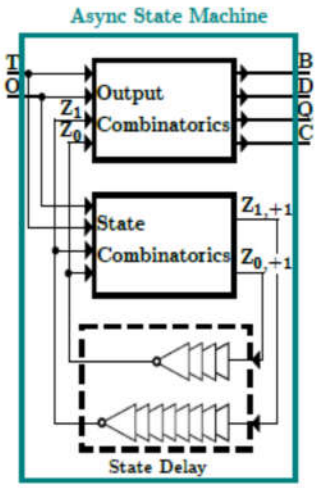

Figure 14. Block diagram of the asynchronous state machine.

5. System Performance

Fig.16 shows system performance for random input data at 1Mbps to the proposed transmitter with quench frequency 1MHz and Oscillator output signal and envelop detector/comparator signals are shown. The frequency spectrum is shown in Fig.17 with desired carrier at 0.4GHz -30dB, but Oscillator signal (800MHz) leaks to the output at 27dB below the carrier power. Hence, the bandwidth limit considering MICS spectral is dominated by the quench frequency. To meet MICS band Pulse shaping is required to meet the MICS band requirements, and can be obtained by RF matching circuits or pulse shaping filters. Complete transmitter specifications are set in Table.2. Table.3 shows a comparison between this work and previously published OOK & super-regenerative transmitters. The proposed transmitter has low energy/bit compared with other architectures except for [22] as quench generator is considered in this work. This shows the simplicity of complete transmitter design with ULP dissipation.

Table 2. Simulation results of the entire quench transmitter.

Parameter	Carrier Freq. (MHz)	Tuning range (MHz)	Max. input data rate (Mbps)	Max./Min Quench freq.(MHz)	Carrier PSD (dB/Hz)	Carrier 3rd harm. (dB)	Oscill. isolation (dB)	1MHz Prms (μW)
Sim. result	402-405	±1	2	1/0.19	-30	-10	-27	537

Table 3. Transmitter Performance Summary and Comparison with other OOK super regenerative transmitters.

Parameter	[22]	[23]	[24]	[25]	[26]	This work
Frequency (MHz)	402-405	13.56	2400	401-406	433	402-405
Technology	90nm	65nm	90nm	180nm	180nm	130nm
Data Rate	1Mbps	100Kbps	100Kbps	1Mbps	NA	2Mbps
Supply voltage (V)	0.6-1	0.8	1	1.8	1.8	1.2
Energy/bit	0.16nJ	0.425nJ	25.3nJ	23nJ	NA	0.27nJ
Power Dissipation	160μW@0.6V	42.5 μW	2.53mW	23mW	580 μW	537 μW

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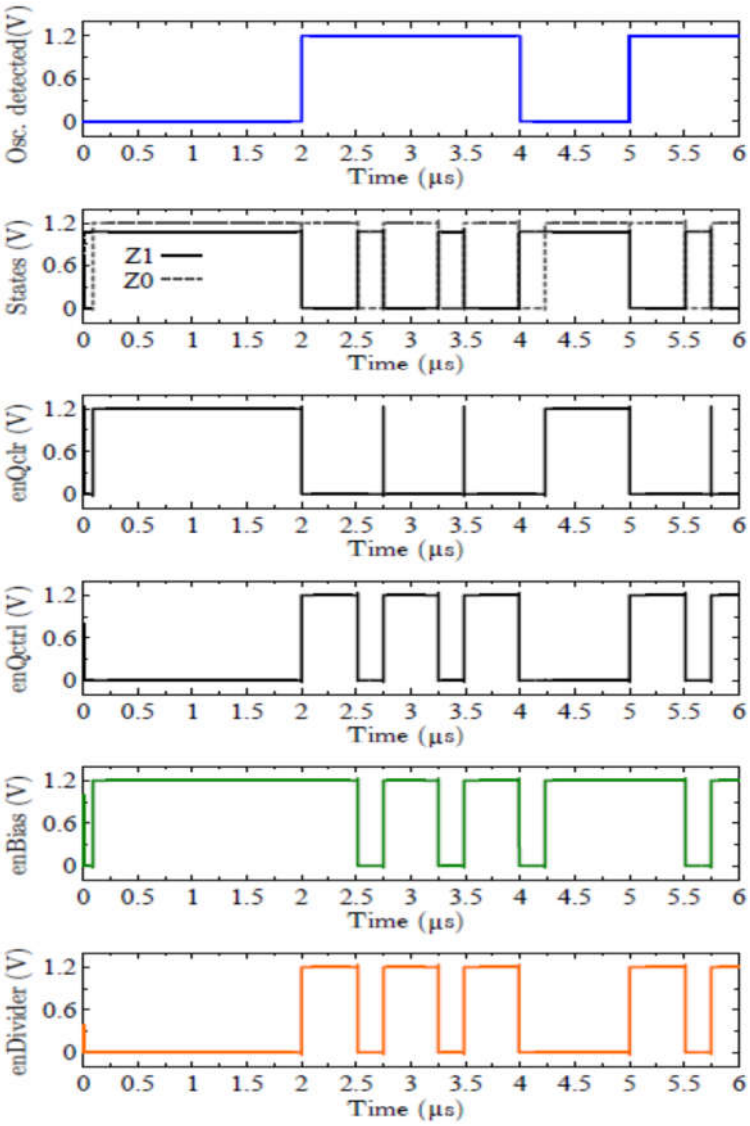

Figure 15. Simulated waveforms of the state machine with quench timer connected for a random input bit pattern (top, blue) at 1 Mbps.

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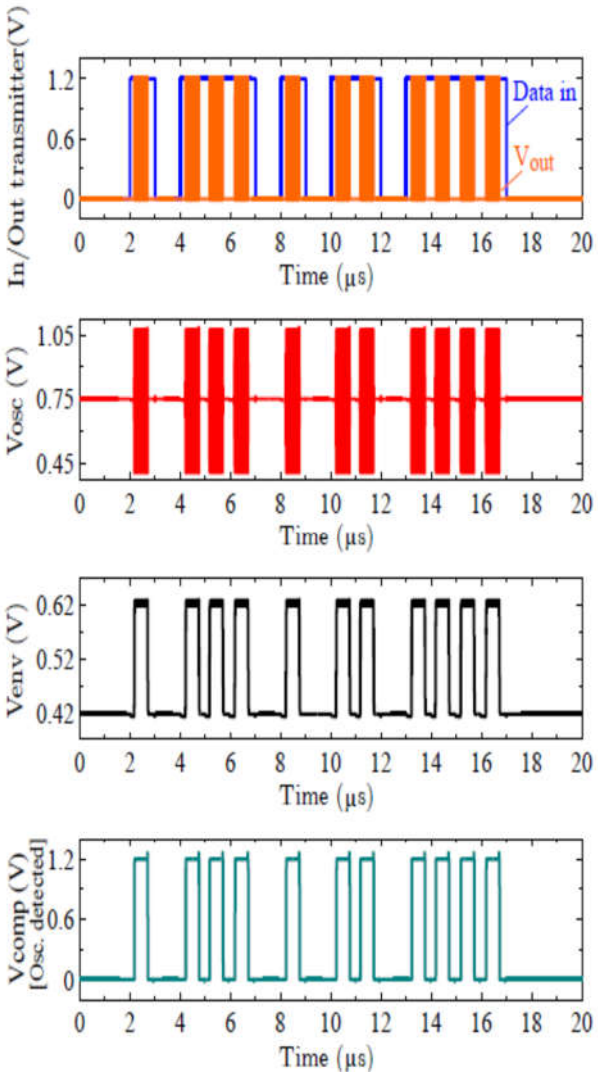

Figure 16. System Performance for random input data at 1Mbps to the proposed transmitter with quench frequency 1MHz.

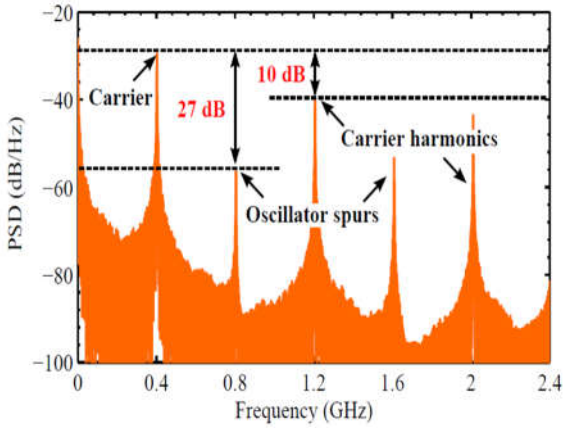

Figure 17. Complete transmitter performance for input data rate 1Mbps with quench frequency signal 1MHz.

6. Conclusions

In this paper, an ultra-low power high/data rate quenched transmitter for OOK super-regenerative biomedical applications is designed. A transmitter consists of a bias current control block, a colpitts oscillator, a frequency divider all used to generate the oscillation signal. A novel digital quenching signal generator is proposed to control the

quenched oscillator operation. The digital control is obtained using an envelope detector that converts the oscillator high frequency to a low frequency signal, input to a comparator to be converted into a digital detection signal indicates the switching of the oscillator. The detection signal is input to the state machine to control the transmitter operation. The complete proposed transmitter is implemented using UMC 130nm CMOS technology 1.2V. The frequency spectrum of the proposed system is simulated to check its ability to meet FCC regulations, the harmonics PSD can be improved using a pulse shaping filter. The proposed transmitter operates at high data rates compared with other architectures (up to 2Mbps) and consumes 537μW.

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