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Article

Design and Simulation Full-Subtractor Based of Reversible logic in Quantum Cell Automata Technology

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Abstract

Quantum cell automata (QCA) is a nanotechnology that uses a transistor-free structure to design digital circuits and overcome the limitations listed for CMOS circuits. The computing circuits that make up the bulk of computers can be designed and using this technology. Subtractors are a big part of computational circuits. This research deals with the design of a subtractor that due to the innovation in the design of this circuit and the novel arrangement of quantum cells of its kind has caused the number of cells used in the design of the circuit to reach its lowest value compared to previously designed circuits. The size of the circuit as well as the loss power are minimized compared to the circuits designed by the subtractors. Another trait clears of this circuit compared to many previous designs is its single-layer design, which reduces latency and noise in the output waveform. The circuit designed by the QCADesigner simulator is tested and simulated inadition the results are displayed in the simulated waveform. Also, the results of calculations for power dissipation in each QCA cell were evaluated by QCAPro software, which is a powerful tool for estimating power loss simulation. It has less implementation and level (single layer) than Previous designs.

Keywords: Nanotechnology; Quantum cell automata; Full-subtractor; Waste of power and Reversibility logic

1.Introduction

One of the main goals of building fast and small quantum computers is to save energy. One of the main and important problems in designing VLSI circuits is the dissipation of thermal energy produced by circuit transistors and therefore the design of low power circuits has become a very valuable field for hardware designers. Quantum cellular automata is a computational technology used to build nanoscale circuits. The technology is based on the QCA cell, a cell consisting of four holes arranged squarely next to each other [1].This new generation of computers which are based on quantum cellular automata technology has a high processing power of up to terabytes. Among the advantages and key roles of QCA are the intersection of same-plane wires processing along the wire and moving memory [2].

A QCA cell consists of four quantum dots located inside a square. Two extra electrons are inside the cell and can move freely between four quantum dots. Frequent movement between quantum dots through tunneling into or out of the cell is not adjacent and does not occur [3]. This makes the power dissipation in this technology very low. Electron repulsion between electrons causes the charges to be placed opposite each other as far apart as possible idealogy. Depending on which square diameter

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the bars are on the polarity of cells is 1 and -1. Polarity 1 is equivalent to one binary and polarity -1 is equivalent to zero binary [4].

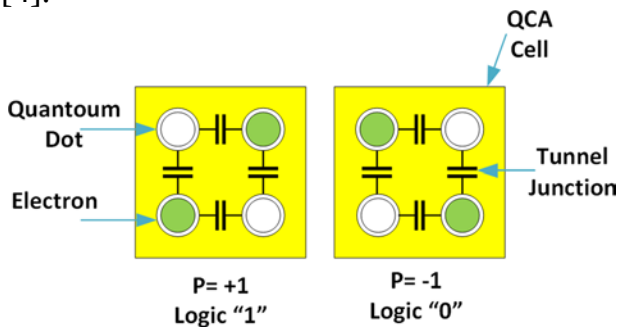

Figure 1. QCA cells with two different polarities and display their binary equivalents.

In 1961, Land Rover first introduced communicate physical reversibility and logical reversibility known as the Land Rover principle states that if the relationship between each input and output is not unique in any logic circuit then it is logically irreversible and will waste energy.

According to the second law of thermodynamics the processing of a logic operation returns irreversible energy whose exact value per bit is equal to KTLn2. K is the Boltzmann constant T = 300K, K = $1.3806505 \times 10^{-23}$ JK^{-1}; Therefore, if a logic operation is irreversible, regardless of the technology used in its design and implementation it will undoubtedly have a power dissipation. [5] The amount of heat generated for a bit is 2.9×10^{-21} J, which has been experimentally proven by Brutt et al. [6] So it can be said that at the time this issue was raised by Land Rover this amount of loss per bit was not significant but since today millions of processes are done in a few seconds and the frequency of system processors is increasing day by day, we will face a loss of power due to these lost bits, with a significant amount.

In the early 1960, Land Rover [7] based on thermodynamics showed that the design of logic and digital circuits based on irreversible logic leads to an unwanted waste of energy. This is because there are more inputs to these circuits than there are outputs. In 1965 Mr. Moore stated that the number of digital circuit transistors would almost double every two years. [8]. Therefore, with this increase according to Landover we will directly see more energy loss. After Landover, Bennett proved in 1973 that only circuits made of reversible gates could have zero loss power, and that there was a direct relationship between the bits lost in the system and the loss power [9]. The proposed design of QCA-based half and full- subtract has an area of 0.06 µm and 0.10 µm, respectively, which occupy an area of 0.13 µm and 0.17 µm, respectively, compared to conventional subtractor. Also, this modified half and full- subtractor has 83 cells, respectively, while the normal half and total subtractor have 93 and 122 cells, respectively [10]. The concept (QCA) was introduced by Togo and Lent in 1993. They proposed this new method as an alternative to making electronic devices. In this paper, full-subtractor reversible gate is designed. This gate has 63 quantum cells and an occupied area of 0.05 square micrometers. The proposed gate is implemented in QCA technology [11].

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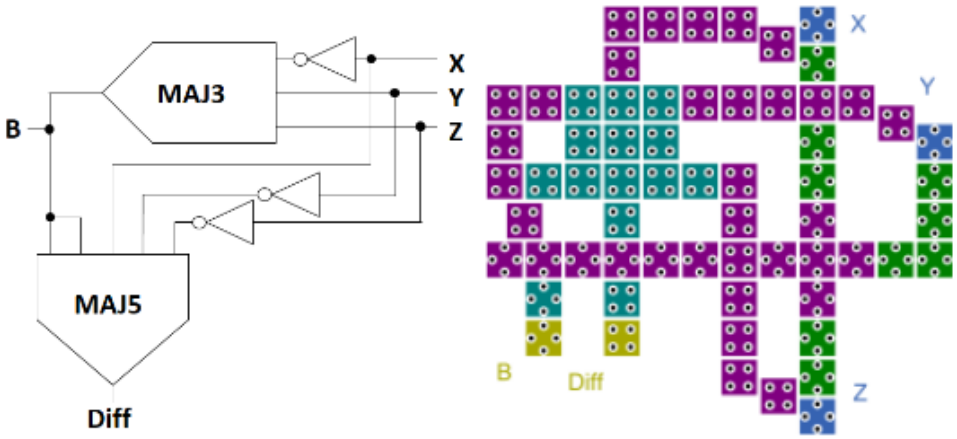

Figure 2. All collector blocks [11].

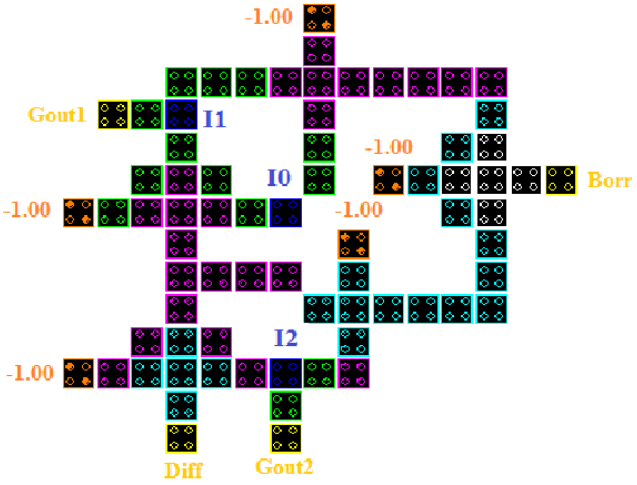

Figure 3. Full- reversible subtractor block diagram [12].

One of the proposed designs for full- subtractors is related to figure (4). It was designed by 178 cells with dimensions of 0.205 μm in three layers. [13]

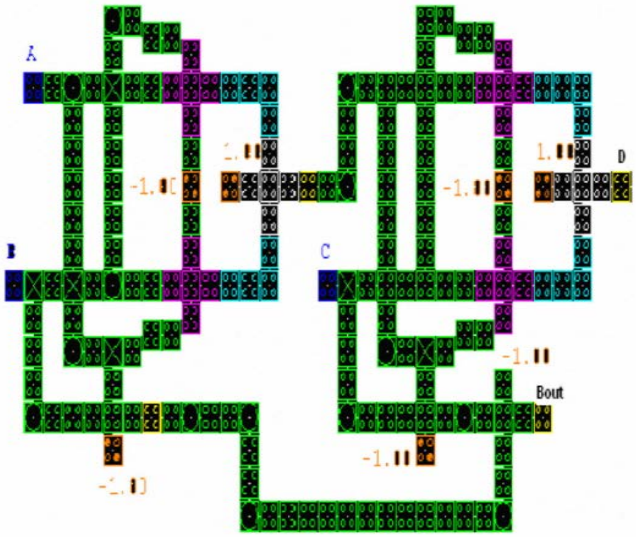

Figure 4. Full- subtractor circuit related to the design [13].

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The subtractor block diagram is shown in figure (5). As can be seen this design consists of nine gates a majority of three inputs and six inverting gates.

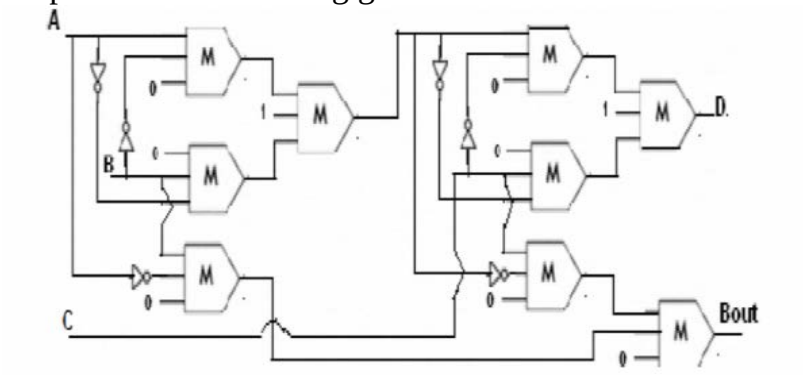

Figure 5. full- subtractors diagram block with majority gate [14].

The next design to be considered for full- subtractors is the circuit design that the circuit designed with QCA is shown in figure (6). [14] It was designed by 136 quantum cells and occupies a size of about 0.168 square micrometers. The block diagram of the design is shown in figure (7).

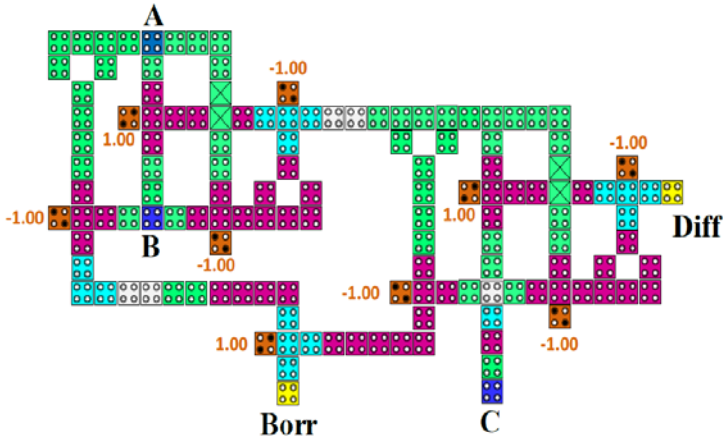

Figure 6. Full- subtractor circuit. [14].

It was designed by nine gates a majority of three inputs and four inverter gates.

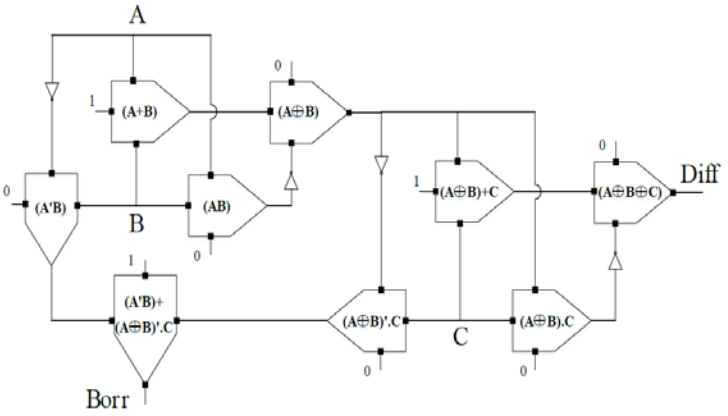

Figure 7. Full-subtractor diagram block with the majority.

QCA circuit we have considered is the full-subtractor circuit, which contains 104 quantum cells measuring approximately 0.1043 square micrometers. This circuit is shown in figure (8). [15]

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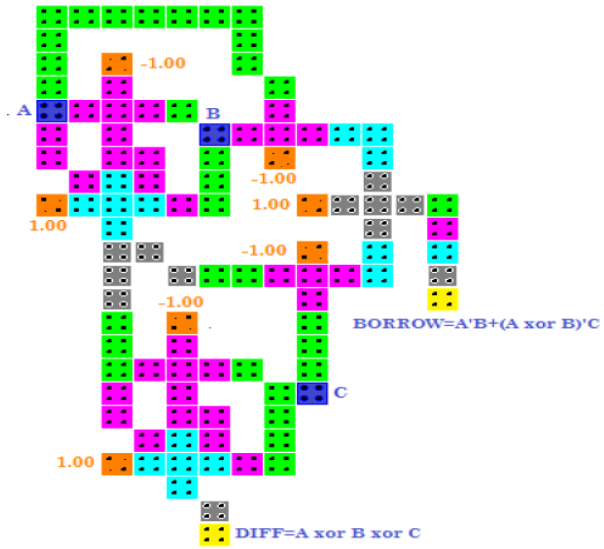

Figure 8. Full- subtractor circuit [15].

2. Cell Quantum Automata Technology

Cell quantum automata is a computational technology used to build electronic circuits at the nanoscale. The cells of this technology are square in shape and have four quantum dots which are placed next to each other as shown in figure 9 (a). The size of the side of each cell is 18 nanometers and the distance between the cells is 2 nanometers. There are two extra electrons in each cell that can move freely between quantum dots. Unlike today's transistor-based technology it is the interaction of QCA cells that creates the desired logic. In general, it is possible to imagine a state for electrons to be placed inside quantum dots (figure 10) [16] but despite columbus repulsion (electrostatic attraction and repulsion), not all of these states are stable. The electrons are always at the farthest distance from each other [17], meaning that only the first and second states in figure 10 are stable.

In calculations logical values of 0 and 1 are attributed to these two states respectively. Each cell can also be rotated 45 degrees counterclockwise; This is used to cross two wires and make an inverter. The rotating cells (Figure 9 (b)) are rhombic in shape.

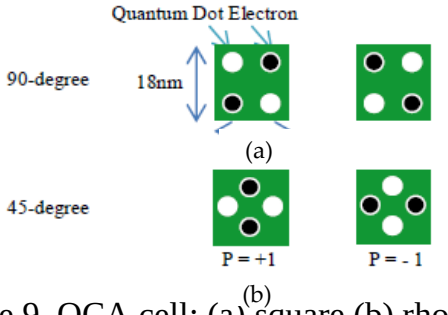

Figure 9. QCA cell: (a) square (b) rhombic

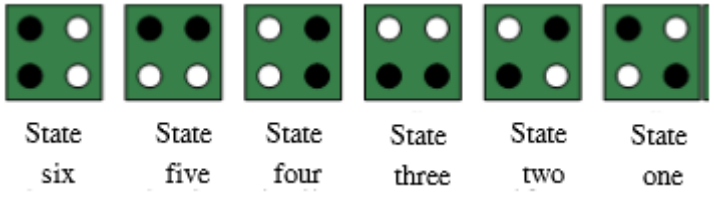

Figure 10. The positions of electrons inside quantum dots.

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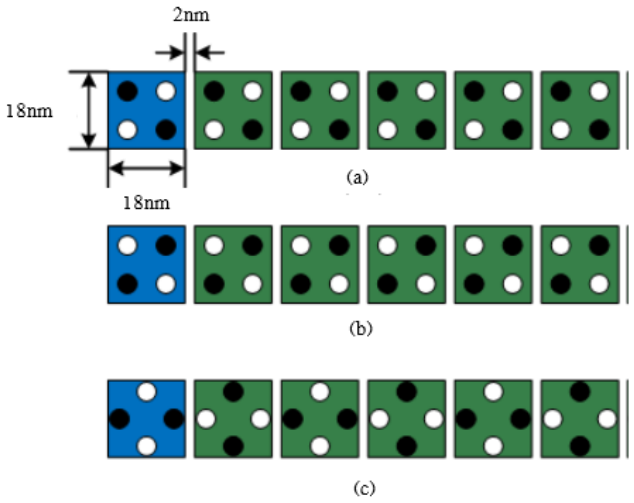

Figure 11. (a) Propagation of logic 0 (b) propagation of logic 1(c) propagation by rhombic cells.

Columbus repulsive force affects not only the cell but also adjacent cells. When two cells are placed next to each other electrons move at quantum points in a way that minimizes the Columbine repulsion force throughout the set. As a result, as shown in figures 11 (a) and (b) in a consecutive array of cells, any change in the first cell also affects subsequent cells. This is how the QCA wire is made. The placement of rhombic cells next to each other in figure 11 (c) forms a chain of inverters. Wire is the most basic tool for building electronic circuits. The size of the cells is also shown in figure 11. Cell clock is used to control data flow. In this method the cells are connected to one of the four areas of the clock (with different coloring) (Fig. 12). Each clock has a phase difference compared to the adjacent clock size of 27% percent. The arrangement of the effect is that the cells affect the clock range (0 <i <3) on cells with a clock range of 4 mod (1 +1). There for as shown in figure 13, the data flow is determined in QCA circuits. Using the clock, the electrons of the cells can be freely abandoned, reducing their movement speed, or even kept electrons in its place. Each clock also has four phases. [18]

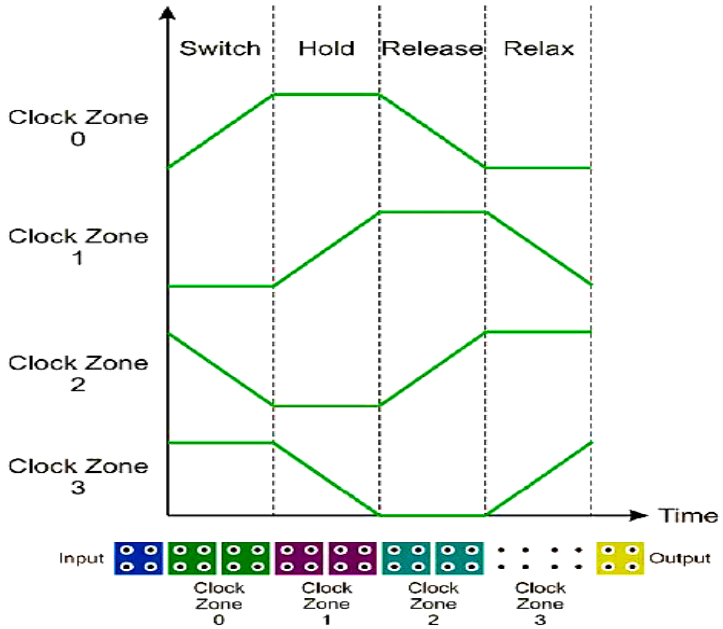

Figure 12. Clock signals in cell quantum automata technology.

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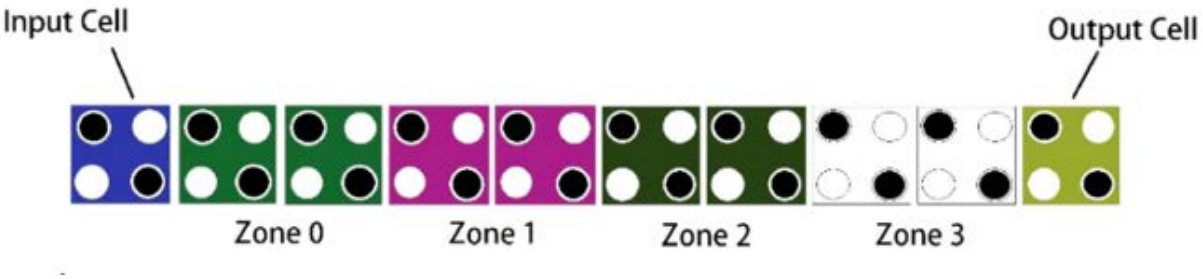

Figure 13. Data flow according to how clapland.

1. Switch phase: The forces prevented the movement of electrons inside the cell and the motion of the electrons gradually slow.
2. Hold phase: The forces have reached its highest and the location of the electrons remains almost constant.
3. Release phase: The amount of blocking forces decreases and the electrons are slowly released.
4. Relaxed phase: The barrier forces reach the lowest level and electrons move freely inside the cell.

With regard to the complexity of the large circuits, the passage of two wires is inevitable. In the cell quantum automata technology, the passage of two wires from each other has challenges. There are three different methods for this. The first method (Fig. 14 (a)) is the combination of square and rhombic wires. The second method (Fig. 14 (B)) is performed using multi-layer quantum automata technology. The third method (Fig. 14 (c)) is also done according to the areas when they are not affected. The cells that differ in two clocks are not affected by each other. The third method is the most reliable and low-cost way of passing the wires [19]. The simplest logical function is the inverter, which is shown in figure 15 of the common methods of implementing it [20]. The gates AND and OR are implemented using the majority voting function (Fig. 16 (a)). The votes function of the majority (relationship 1) with binary inputs b, a and c is a base gate in this technology. [21]

$$\text{Majority}(a,b,c)=a.b+a.c+b.c \quad (1)$$

To create functions AND and OR, one of the inputs of the majority voting function is placed equal to the constant value of 0 (polarization -1) and 1 (polarization 1) (Fig. 16 (b) and (c)).

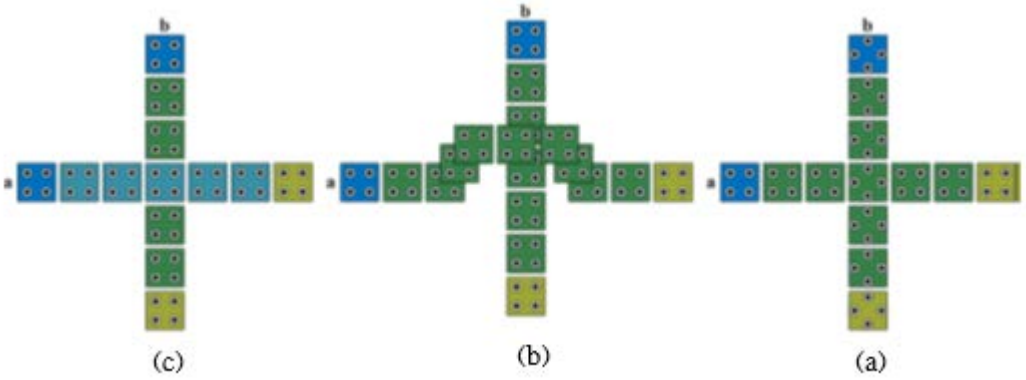

Figure 14. Methods passing two QCA wires from each other: (a) using the composition of square and rhombic cells (b) using multi-layer implementation capability (c) using phase difference of time zones

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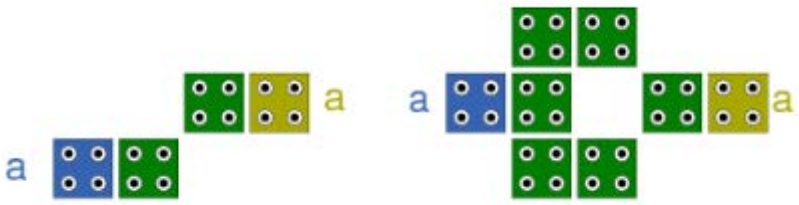
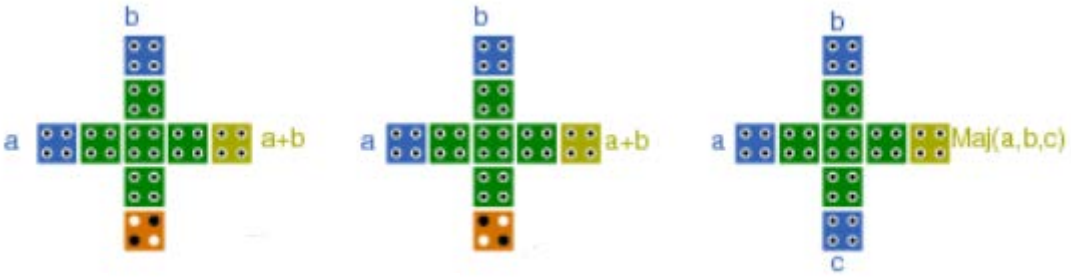


Figure 15: A variety of commonly reversed implementation methods



(c) (b) (a)

Figure 16. Implementation of logical gates: (a) Majority vote function(b) function AND(c) OR function.

3. Proposed plan for XOR three inputs

in this section examines the proposed design for full- subtractor, as well as examining the improvement and enhancement of the number of quantum cells, design dimensions and clock number of phases used and also examines the map of thermal power of designs and their comparison with the wasted thermal power it is addressed. The proposed scheme for xor is three inputs in figure 17. This design is designed with at least possible cells and in small dimensions than other xor examined in the previous section. This optimization saves the size and number of cells and thus in the waste of energy.

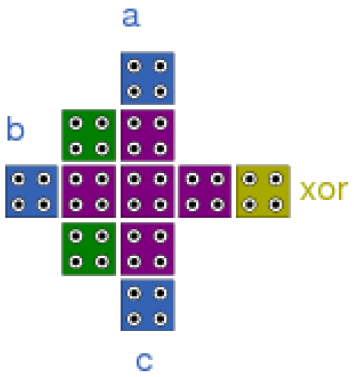


Figure 17. Proposed plan for xor three inputs.

As shown in the figure this three-input xor is designed with 11 quantum cells and operates in two phases of the clock. To ensure proper operation we simulated this circuit in QCADesigner software and showed the results of the diagrams in Figure (18).

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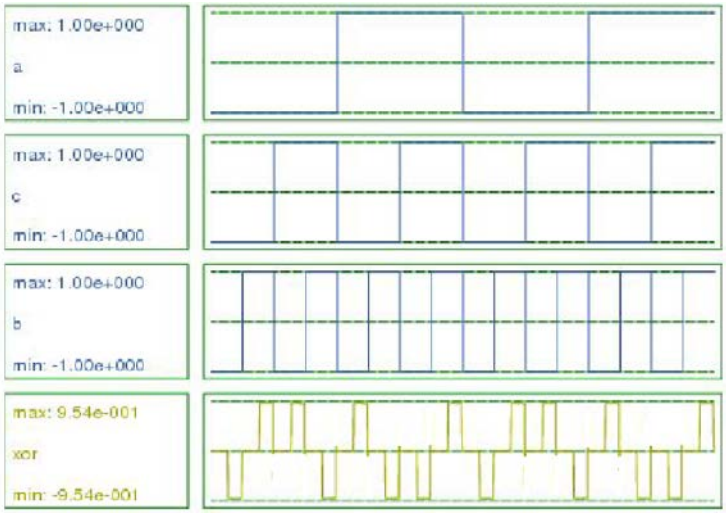

Figure 18. Proposed xor simulation results.

1-3. The proposed design for full- subtractor

using the proposed xor layout in the previous section designed to design all the subtractor with QCA which is shown in figure 19. This full- subtractor is designed with minimum quantum cell. The phases used in three clocks are zero, one and two as the design of the circuit is composed of two parts of the xor three proposed entries and a majority gate of three inputs and input A reversed into one of the majority gate inputs. Inputs of B and C are directly connected to the majority gate.

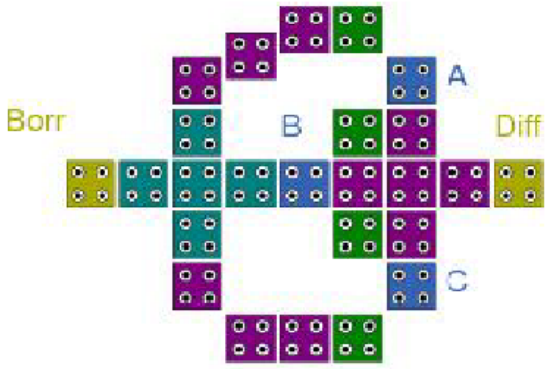

Figure 19. Proposed scheme for full- subtractor.

The circuit consists of a new three-input xor a three-input majority gate, and an inverting gate which are closed as a block diagram (figure 20). The total number of cells used in this QCA circuit is 25 cells. For the first time we designed a full- subtractor circuit with this number of cells.

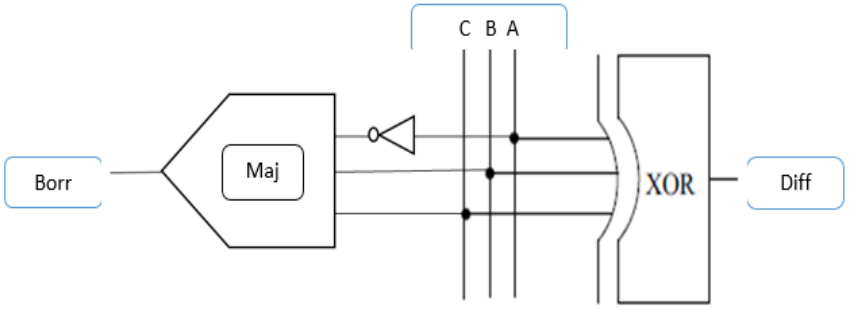

Figure 20. Block diagram of proposed full -subtractors.

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A bit input has the highest value and C bit has the lowest value. This bit is the same as Borr input or input assumption. To check the Diff and Borr outputs in the diagram block of the full-subtractor circuit and to confirm the correctness of the circuit a logical equation must be confirmed for this circuit. Equation (1) shows the output relationships of the full-subtractor block diagram. To prove this, we must first examine the orbital shape of the subtractor and then arrive at the final equation from the inputs and outputs of the circuit. Figure (21) shows the logic circuit of the whole subtractor.
Equation (1) The subtractor equation with the majority gate

$$\text{Diff}=A\oplus B\oplus C$$

$$\text{Borr}=\text{MAJ}(\overline{A},B,C)$$

Equation (1) shows the relationships of blocks of the block diagram of Full- subtractors. For this proof we must first examine the shape of the subtractor and then reached the final equation from the input and outputs of the circuit.

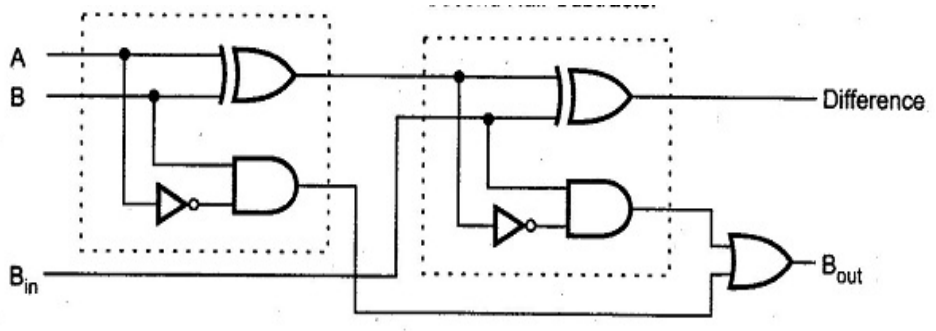

Figure 21. Shows the logical circuit of full- subtractor.

As shown in the form of the circuit the Diff output is exactly matched with the equation (1). Borr output in equation relationships (2) has been proven.
Equation (2) proof of subtractor equation with majority Gate

$$\begin{aligned}
\text{Borr} &= \overline{A}B + (\overline{AB} + AB)C \\
&= \overline{A}B + \overline{A}\,\overline{B}C + ABC \\
&= \overline{A}B(1 + C) + \overline{AB}C + ABC \\
&= \overline{A}B + \overline{A}\text{BC} + \overline{AB}C + \text{ABC} \\
&= \overline{A}B + BC(A + \overline{A}) + \overline{AB}C \\
&= \overline{A}B + BC + \overline{A}\,\overline{B}C \\
&= \overline{A}B(1 + C) + BC + \\
\overline{A}\,\overline{B}C &= \overline{A}\text{B} + \overline{A}C(\text{B} + \overline{B}) + \text{BC} = \overline{A}B + \overline{A}C + BC \\
&= Maj(\overline{A}, B, C)
\end{aligned}$$

2-3 The simulation results of the full- subtractors

In this section, the results of the output diagrams will be examined and some parameters of the previous circuits will be compared with the proposed designs. In the following, using the simulator tool QCAPro 1.0, [22] the heat loss power loss will be estimated. Using QCADesigner 2.03 software, we tested the proposed QCA circuit, and the results of the output diagrams are shown in figure (22).

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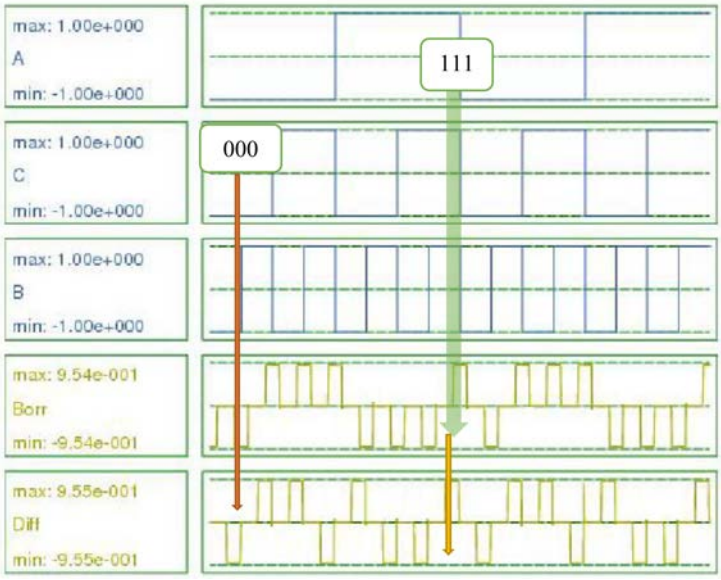

Figure 22. Simulation results of proposed subtractor.

We examined two situations on the diagram one of the 000 inputs and the other inputs 111. In the complete subtractor table showed that in the state of 000 for inputs the Diff output is zero logic and the Borr output is zero logic. If the Diff output diagram checks the zero status. Also for the status of inputs 111 according to the accuracy table, both Diff and Borr outputs are 1 logic that are confirmed by referring to the output diagram. It should be considered that because the Diff output in the phase clock of the one and the Borr output is in the phase clock two these two outputs will have a phase difference with the size of a clock.

3-3. Comparison of the parameters of the previous three xor designs with the proposed design

To examine the advantages of the proposed design with the previous three designs, two tables have been prepared in which both three xor circuits and three subtractor circuits have been compared with the proposed designs. Table (1) is a comparison of the proposed xor with the previous three designs.

Table 1. Comparison table of previously introduced xor with the proposed design

Gate	Number of cells	Approxmiated area ($\mu m)^2$	Type of wire crossing	Latency clock cycle	Gate count (MG+Inverter)
xor Gate [10] (2 input)	30	0.0233	coplanar	0.75	4
xor Gate [11] (3 input)	97	0.2	coplanar	1.25	3
xor Gate [12] (2 input)	32	0.0235	Coplanar	1	3
Proposed xor (3 input)	11	0.0098	coplanar	0.5	New combination

As can be seen from Table (1), the proposed scheme for xor is superior to the previous three designs in terms of number of cells and area occupied, as well as the number of phase clocks. Examining the xor three inputs in the table, it can be seen that the number of cells has been reduced by about 9 times in the proposed design. We also reduced the occupied area more than twice in the plan. The superiority

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of the phase clock is also quite clear. The proposed design is also superior to the two-input xor according to the table.

4-3-Comparison of three subtractor schemes with the proposed subtractor scheme

Like the xor design for full -subtractors a table has been created to compare with the three designs introduced in the previous section. In table (2) items such as the number of quantum cells, the occupied area the number of phase clocks as well as the number of gates used in the previously mentioned designs are compared with the proposed design of full -subtractors.

Table 2. Comparison table for full -subtractors introduced with the proposed scheme

Gate	Number of cells	Approxmiated area ($\mu m)^2$	Type of wire crossing	Latency clock cycle	Gate count (MG+Inverter)
Full- Subtractor [12]	73	0.0831	coplanar	4	13
Full -Subtractor [13]	178	0.205	3 Layer	8	15
Full -Subtractor [14]	136	0.136	3 Layer	7	13
Full- Subtractor [15]	104	0.1043	coplanar	7	14
Full- Subtractor [16]	108	0.12	coplanar	3.5	13
Full -Subtractor [17]	45	0.05	3 Layer	3	12
Proposed Full- Subtractor	25	0.0245	coplanar	3	3

By examining and comparing the parameters examined in table (2), the complete superiority of the proposed subtractor design can be seen. The proposed design is reduced to a quarter in terms of cell number and halved in terms of number of phase clocks, which in turn reduces output delays. In terms of occupied area, it is reduced by about one-fifth, which in turn reduces power loss.

4.Investigation and estimation of heat loss

4-1-QCAPro software

This software is a probabilistic model for evaluating the polarization error and power loss due to non-adiabatic switching in QCA circuits. This technique is used by the rapid Harter approximation [22] to estimate unsuitable cells in QCA circuits. This tool is also used to estimate power losses in sharp clocks in transition phases from one phase to another. This tool is also used to estimate the maximum and minimum loss power for the corresponding inputs. Power loss in QCA circuits is a very important parameter for researchers in this field, because the power loss and losses for these circuits must be very small. QCAPro creates a polar map of the QCA circuit for each specific input vector. This step is repeated many times to create a polar map for all input vector states. To create a power loss map for the QCA circuit, a set of input vectors to be switched and the ratio of kinetic energy to tunneling energy to the software is applied. The software then calculates the power loss map for all input vector modes.

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4-2-Investigate the lost power of the proposed subtractor circuit with QCAPro

We have applied the proposed scheme for full -subtractors to QCAPro software to investigate the loss power. And we have a map of the power lost in each cell. The more colorful the points, the greater the power drop. We repeat these steps for the three kinetic energy inputs. Figure (23) shows the results of the power loss map for the energy 0.5 E_k, 1E_k and 1.5 E_k.

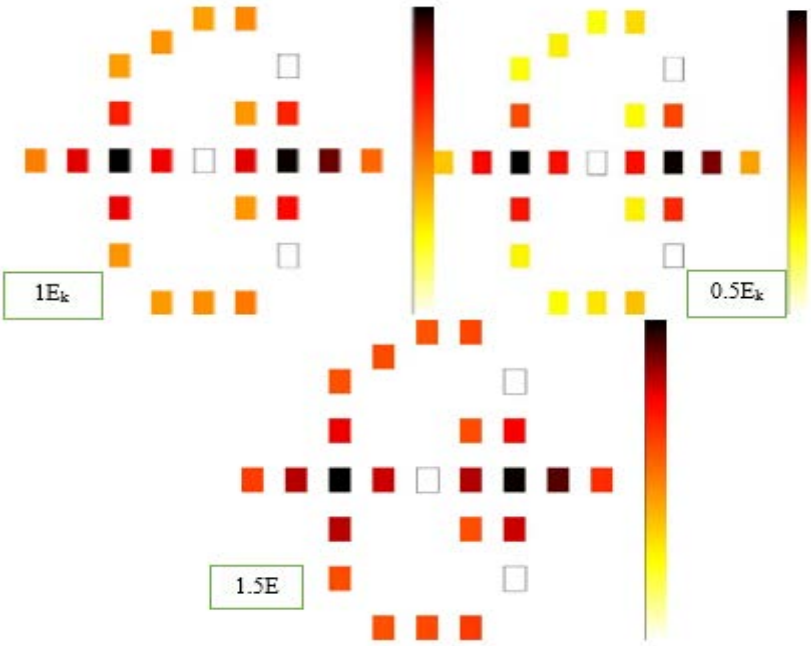

Figure 23. Map of wasted power for values of 0.5 E_k, 1E_k and 1.5 E_k.

As result of comparing the three maps and examining them it is clear that as the amount of kinetic energy increases the power drop in the cells increases.

This fact is characterized by the more colorful cells of the circuit. In addition to the power loss map, QCAPro software provides a text file containing three parameters including average leakage energy loss, average switching energy loss and finally total energy loss. These values are shown in table (3) for three variables E_K.

Table 3. Leakage, switch and total energy values

Full -subtractor	E_K	Proposed Design
Avg. leakage energy dissipation(mev)	0.5	8.96
	1	23.78
	1.5	40.06
Avg. switching energy dissipation(mev)	0.5	25.85
	1	22.28
	1.5	19.21
Total energy dissipation(mev)	0.5	69.63
	1	75.20
	1.5	83.87

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To compare these energies which are related to the proposed design with the three subtractor schemes introduced in the previous chapter table (4) has been prepared which shows the difference between the wasted energies of leakage, switch and total.

Table 4. Amounts of energy wasted for the previous three designs and comparison with the proposed design

Full - subtractor	E_K	[13]	[14]	[15]	Proposed design
Avg. Leakage energy dissipation	0.5	92.85	58.38	37.21	8.96
	1	246.89	160.30	98.50	23.78
	1.5	409.09	272.09	165.04	40.06
Avg. Switching energy dissipation	0.5	149.34	102.00	61.97	25.85
	1	114.32	83.83	50.90	22.28
	1.5	90.29	68.83	42.31	19.21
Total energy dissipation	0.5	242.19	160.37	99.18	69.63
	1	361.21	244.13	149.4	75.20
	1.5	499.48	340.92	207.35	83.87

As it is clear from the obtained values the significant superiority of loss energy reduction for the proposed proposal of full -subtractors in the values of leakage loss energy and switching loss energy as well as total loss energy has been achieved.

4-3-Check the average AOP [1]output polarity test

This test called output reliable, shows the thermal effects on changes in output polarity. In this test performed by QCADesigner software on the output subtractor circuit. In the software settings section, in the Coherence Vector Option section we check the output polarity by increasing the temperature from $1E_K$ to $11E_K$. By obtaining the output values at different thermal values we have drawn the corresponding curve which can be seen in figure (24). This curve shows the effects of changes in the output polarity relative to the increase in heat.

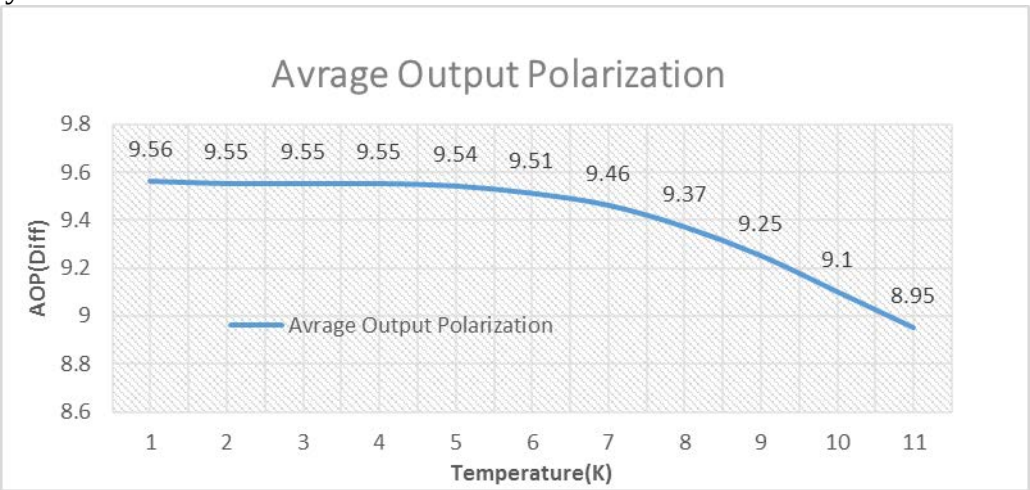

Figure 24. AOP test curve.

[1] Average Output Polarization

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As we have shown in the figure, up to 8 $E_K$outputs are fixed. From this value onwards, the average polarity of the output of the sharia decreases. An example of a temperature setting of $8E_K$ in the QCADesigner software is shown in figure (25).

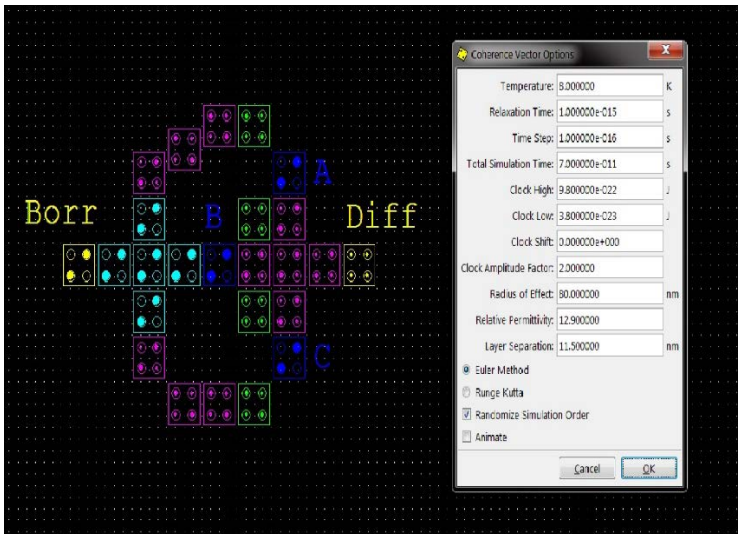

Figure 25. An image of the temperature setting in QCADesigner software.

4-4- Check AOP graphic map using QCAPro

QCAPro software detects polarization errors due to heat gain more accurately and faster than the Coherence method in QCADesigner software. Also by providing a polarity drop estimation map this figure can be read on any of the QCA cells so apply the proposed subtractor circuit in QCAPro. We obtained the graphic map of polarity changes and showed the results in figure (26).

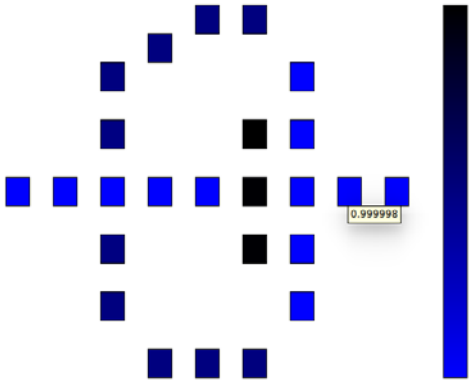

Figure 26. AOP test map in QCAPro software

As can be seen in the figure placing a cursor on one of the cells displays the amount of polarity error on it. It should be noted that light blue dots indicate the least polarity error and the more colorful the quantum dots the greater the polarity error.

5. Conclusion

In this paper, we examined the proposed subtractor detection diagrams by QCADesigner software. Analysis of two 000 and 111 inputs from these values was investigated in the output of full- subtractor. As the analysis of the subtractor detection diagram this orbit while reducing the number of quantum cells had a minimum amount of noise in the output compared to previous studied circuits. To simulate and analyze the energy of the proposed circuit and compare it with previous circuits by QCAPro

software Energy is optimal. In the QCA scheme, all these subtractors have tried to provide a round structure that is optimal in terms of cell number, latency, occupancy level and energy consumption. For this reason, in the proposed structure of 39.96 cells, 42.65 percent delays, 48.65 percent occupied area and 68.96 Percent energy consumption.

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