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*Article*

# The concept of designing BiJT operational amplifiers for anti-aliasing active LPF with a low level of systematic component of the zero offset voltage

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**Abstract:** The zero offset voltage in anti-aliasing low-pass filters (LPF) included at the ADC input has a significant effect on the effective bit rate of the ADC. The article discusses methods for minimizing the systematic component of the zero offset voltage ($V_{OS}$) of operational amplifiers (Op-Amp) in the structure of the LPF, due to the degradation of the current gain of the base (β) of bipolar transistors for an extremely common subclass of Op-Amp with one high-impedance node. The methods of matching a high-impedance Op-Amp node and a buffer amplifier with the help of special correcting $SCM^p$ and $SCM^n$ multipolars are proposed. Methods of description and formation of the given coefficients of weak current asymmetry of typical Op-Amp functional units (current mirrors, input DS, buffer amplifiers, SRC, etc.) are presented. As an example, the results of computer simulation of GaAs Op-Amp with small $V_{OS}$ performed on JFET field and p-n-p bipolar transistors are given.

**Keywords:** operational amplifier, compensation of the systematic component of the zero offset voltage, differential stage, buffer amplifier, current mirror, reference current source, BJT transistors, GaAs transistors.

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## 1. Introduction

Anti-aliasing LPF, which are switched on at the ADC input, are a mandatory element of many modern analog-to-digital automatic control and regulation systems [1]. The zero level of the LPF has a significant impact on the effective bit depth of the ADC [2-5]. This imposes certain restrictions on the circuitry of operational amplifiers in the LPF structure, which ideally should have $V_{OS}$=0. The reduction of $V_{OS}$ in the Op-Amp depends not only on advances in semiconductor

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technologies, but also on their structural and circuit solutions. The article proposes (through the introduction of special structural redundancy) to minimize the systematic component of the zero offset voltage $V_{OS}$ [6] of Op-Amps oriented to use in the LPF and associated with the influence of the current gain of the base β bipolar transistors.

The study of existing Op-Amp architectures with one high-impedance node of general application [6], focused on the use of low-frequency and bipolar-field technologies, as well as basic matrix and structural crystals, shows that reducing the offset voltage of Op-Amp of this class using the properties of classical prototype architectures of the world's leading microelectronic firms is quite an relevant task.

The purpose and novelty of this article is to develop and study architectural and circuit engineering methods for minimizing the zero offset voltage of the Op-Amp due to the influence of β transistors, as well as increasing its stability in widespread Op-Amp with one high-impedance node on bipolar transistors.

The relevance of the article lies in solving a significant problem of modern analog microcircuits associated with the development of circuit-engineering methods for minimizing the zero offset voltage ($V_{OS}$) of classical operational amplifier architectures, including GaAs p-n-p transistors designed for the design of anti-aliasing LPF.

## 2. Analysis of methods for minimizing $V_{OS}$ caused by the influence of β transistors

A well known method for constructing an Op-Amp with a high-impedance node consists in introducing a special structural redundancy into well known classical Op-Amp circuits, which allows minimizing the systematic component of the zero offset voltage $V_{OS}$ [6] associated with the influence of β transistors. The analysis of serial Op-Amp chips of leading microelectronic companies, as well as integrated into analog devices based on basic and matrix crystals and IP modules of the Op-Amp showed that most of their circuits are reduced to the architecture shown in Fig. 1

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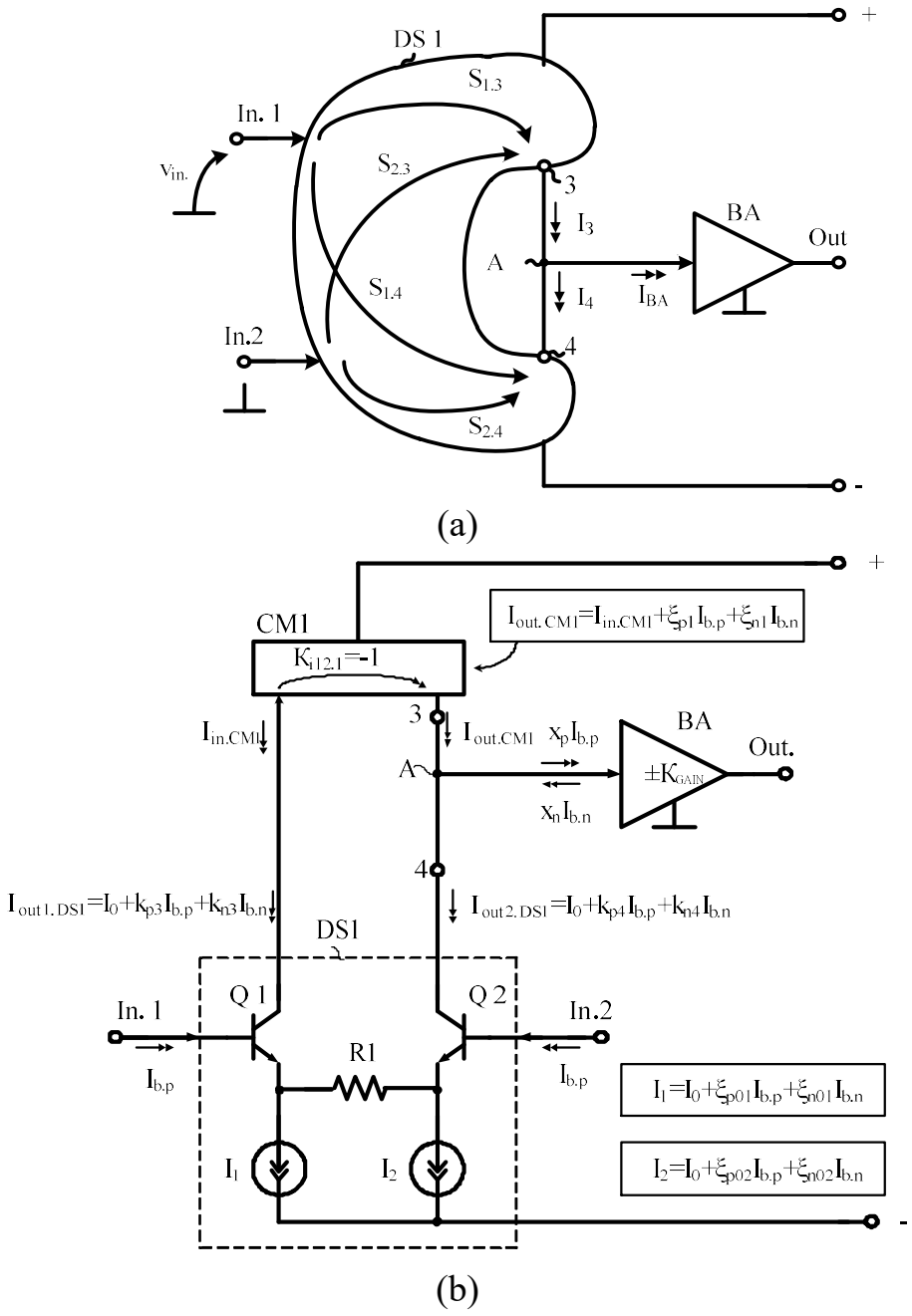


Fig.1 Generalized circuit of an Op-Amp with a high-impedance node (a) and an example of its practical implementation (b) [6]

In the diagram in Fig. 1a, a high-impedance node "A" can be distinguished, which provides summation of the output currents ($I_3$ and $I_4$) of the generalized input differential stage (IDS) and the input current ($I_{BA}$) of the output subcircuit (buffer amplifier, BA). Moreover, the difference current affects $V_{OS}$:

$$I_p = I_3\,(\beta_{i.n}\,,\,\beta_{j.p}\,,\,I_{ij}\,,\,u_{in.}) - I_4\,(\beta_{k.n}\,,\,\beta_{m.p}\,,\,I_{k.m},\,u_{in.}) - I_{BA}\,(\beta_{s.n}\,,\,\beta_{f.p}\,,\,I_{s.f}), \qquad (1)$$

where $I_{ij}$, $I_{k.m}$, $I_{s.f}$ – are the coordinates of current sources that are multiples of the reference current $I_0$, setting the static mode of the Op-Amp circuit transistors; $\beta_{i.n}$,

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$\beta_{k.n}$, $\beta_{s.n}$; $\beta_{i.p}$, $\beta_{m.p}$, $\beta_{f.p}$ – are the current amplification coefficients of the base p-n-p and n-p-n transistors affecting the currents of nodes 3 ($I_3$), 4 ($I_4$) and input current ($I_{BA}$) buffer amplifier.

In Fig.1b, each of the subcircuits DS1, CM1, BA differs from the ideal one and has current coordinates slightly shifted relative to their "ideal" (zero) level: $I_{CM.1} = k_{p3}I_{b.p} + k_{n3}I_{b.n}$, $I_{CM.2} = k_{p4}I_{b.p} + k_{n4}I_{b.n}$, $I_{CM1} = \xi_{p1}I_{b.p} + \xi_{n1}I_{b.n}$, $I_{BA} = x_nI_{b.n} + x_pI_{b.p}$, where $k_{p3}$, $k_{n3}$, $k_{p4}$, $k_{n4}$, $\xi_{p1}$, $\xi_{n1}$, $x_n$, $x_p$ – are scale coefficients (negative or positive integers) at base currents p-n-p ($I_{b.n}$) and n-p-n ($I_{b.p}$) transistors characterizing the shift of the zero levels of the DS1, CM1 and BA subcircuits due to the finite value of β, their temperature and radiation changes.

Analysis of methods for introducing current asymmetry into the basic functional nodes of the Op-Amp [6] showed that these functional nodes of the Op-Amp and the subcircuits forming it (current mirrors (CM), reference current sources (SRC), input differential stages (DS), buffer amplifiers (BA), etc.) should have one or another, but strictly defined current asymmetry. Such a construction allows you to select a certain set of specific functional nodes from the presented set, the connection of which provides a small level of $V_{OS}$.

In general, the asymmetry of the input differential stage of the Op-Amp is taken into account in the equations of its static output currents (Fig. 2) by the coefficients $k_{p3}$, $k_{n3}$, $k_{p4}$, $k_{n4}$, non-zero values of which indicate the difference between $I_3$ and $I_4$ from some ideal values of $I_0$.

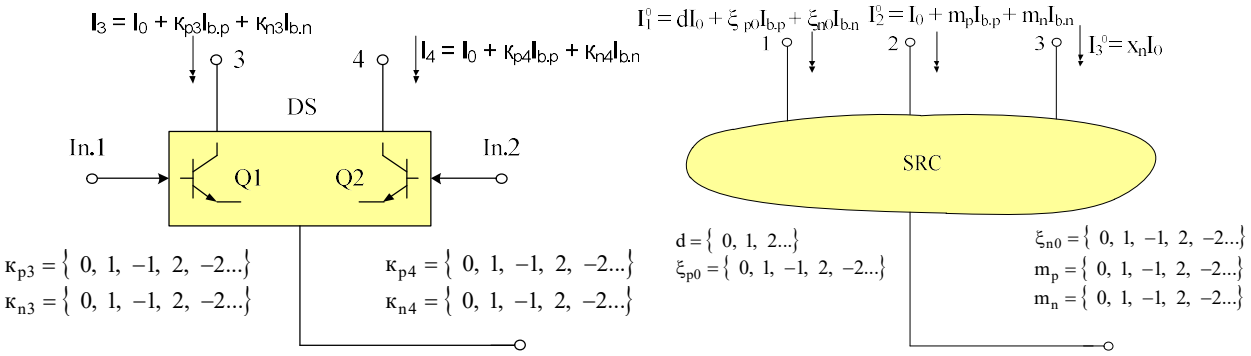


Fig.2 Differential stage (a) and its SRC (b) with weak such asymmetry [6]

The input current asymmetry of existing buffer amplifiers Op-Amp is usually described by an equation that generally takes into account two components of the input currents:

$$I_{BA} = x_pI_{b.p} - x_nI_{b.n}\,, \qquad (2)$$

where is $x_p$ = { 0, 1, 2, 3...}, $x_n$ = { 0, 1, 2, 3...} – the coefficients of the current asymmetry of the BA. For the synthesis of practical Op-Amp circuits, there are basic options for constructing a control unit with different coefficients $x_p$, $x_n$, as

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well as Op-Amp reference current sources, which can have several outputs and are characterized by individual coefficients of weak current asymmetry [6].

In a number of practical tasks, it is impractical to make any adjustments to the initial structure of the input DS prototype in order to ensure the necessary values of the coefficients of weak current asymmetry. In these cases, it is recommended to introduce special correcting multipolars of p- ($SCM^p$) and n-types ($SCM^n$) into the initial circuits, as shown in Fig.3.

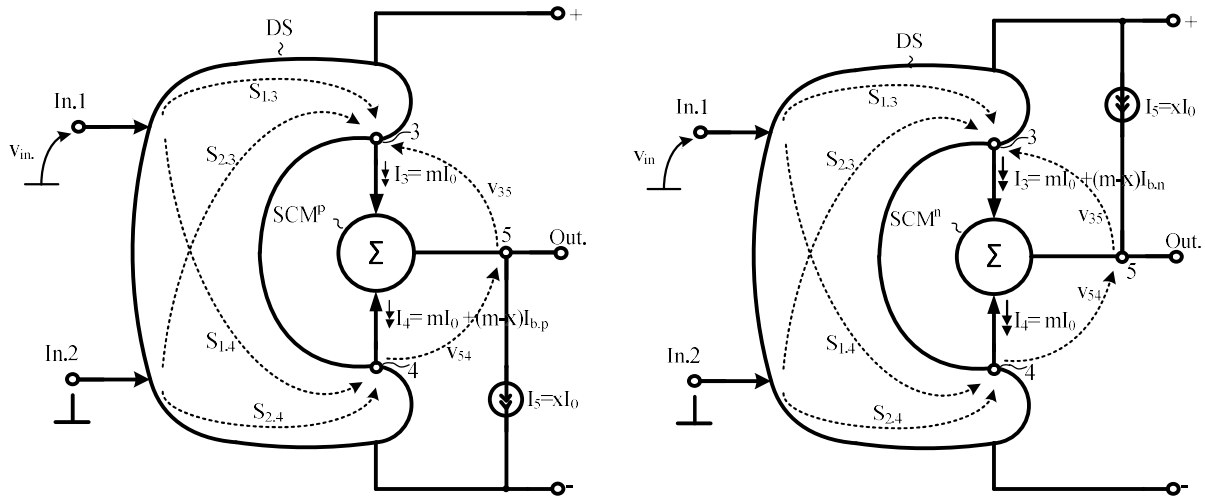


Fig.3 The method of $SCM^p$ (a) and $SCM^n$ (b) compensation

A schematic example of the use of special corrective $SCM^p$ - and $SCM^n$ - multipolars in the Op-Amp is shown in Fig.4.

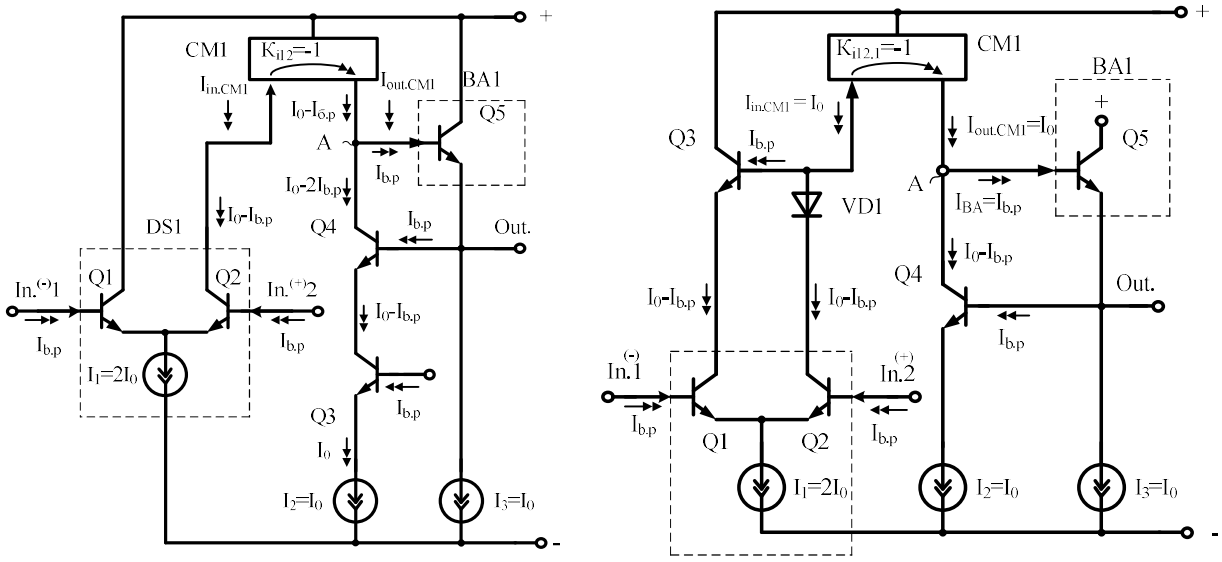


Fig.4 $SCM^p$ (a) and $SCM^n$ (b) – multipolars in the Op-Amp

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In this case, the currents of individual Op-Amp nodes can be calculated as:

$$I_{c2} = I_0 - I_{b.p} = \mathrm{I}_{c1},$$

$$I_{e3} = I_0,$$

$$I_{c3} = I_0 - I_{b.p} = I_{e4},$$

$$I_{e5} = I_0 + I_{b.p} \approx I_0,$$

$$I_{c4} = I_0 - 2I_{b.p},$$

$$I_{in.CM1} = I_0 - I_{b.p} = I_{\mathrm{out.gn1}},$$

$$I_p = \mathrm{I}_{out.CM1} - \mathrm{I}_{b.5} - I_{c4} = 0.$$

In this case , the systematic component of the zero offset is equal to:

$$V_{OS} \approx \mathrm{I}_p(r_{e1} + \mathrm{r}_{e2}) = I_p\left(\frac{2\varphi_m}{I_0}\right) \approx 0. \qquad (3)$$

The considered circuit technique is recommended to be used in the case when the structure of the input stage of the Op-Amp is not subject to modernization.

## 3. Synthesis of other modifications of precision Op-Amp

The solution of the equations for the coefficients of weak current asymmetry of the main functional nodes of the Op-Amp based on Darlington input transistors allowed us to synthesize a modified circuit [6] in which the systematic component of $V_{OS}$ is obtained two orders of magnitude less ($V_{OS}$ = 14 uV) than in the classical Op-Amp.

Fig. 5 shows a general case of mutual compensation of parasitic current coordinates of a high-impedance node in a three-stage Op-Amp.

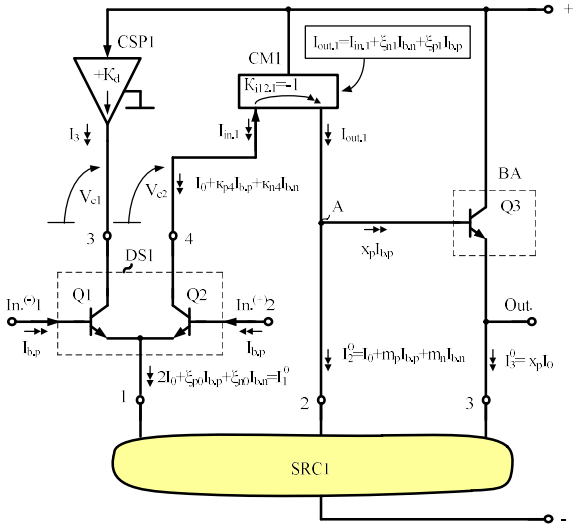


Fig.5 Architecture of a precision Op-Amp with an asymmetric inclusion of the input DS [6]

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For the case when the asymmetry coefficients of the input DS $k_{p4} = 0{,}5\xi_{p0}-1$, $k_{n4} = 0.5\xi_{n0}$, the condition for minimizing the zero offset voltage of the Op-Amp can be represented as:

$$\begin{cases} 0{,}5\xi_{p0} + \xi_{p1} = m_p + x_p + 1 \\ 0{,}5\xi_{n0} + \xi_{n1} = m_n \end{cases} . \quad (4)$$

Fig. 6 shows an Op-Amp with the architecture "Classical input DS – uncontrolled current mirror - output emitter repeater" [6].

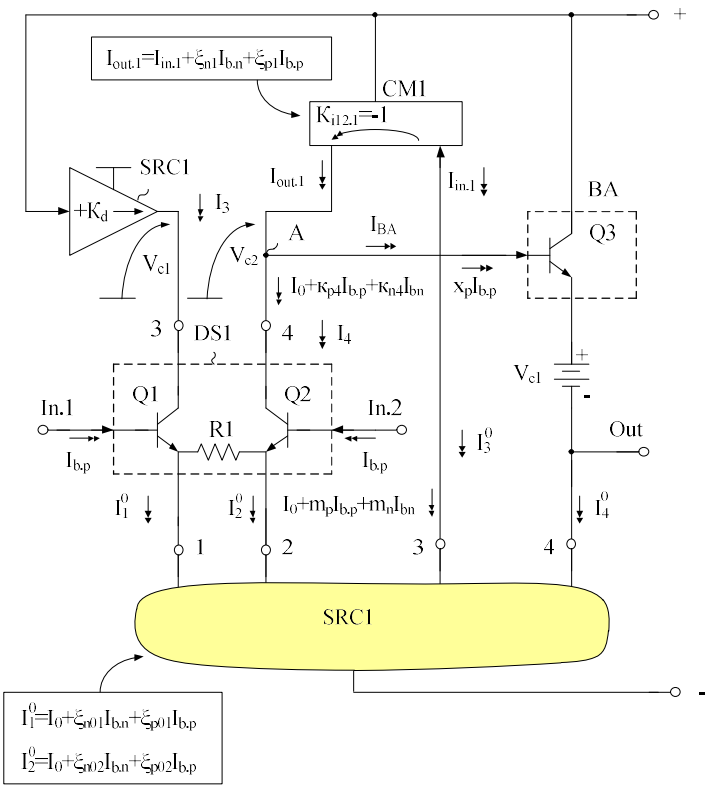


Fig.6 Architecture of precision Op-Amp with asymmetric inclusion of current mirror CM1

To minimize the $V_{OS}$ component under consideration, it is necessary to synthesize subcircuits DS1, CM1, BA, SRC1, whose scale coefficients $k_i$ , $\xi_i$ , $x_i$ , $m_i$ at known values of the base currents $I_{b.p}$ and $I_{b.n}$ of the applied n-p-n and p-n-p transistors satisfy the condition: $m_p + \xi_{p1} = k_{p4} + x_p$, $m_n + \xi_{n1} = k_{n4} + x_n$.

The use of buffer amplifiers with two common-mode outputs [6] significantly reduces the $V_{OS}$ of the Op-Amp of the corresponding subclass. Mutual compensation of errors of current mirrors in an Op-Amp with a complementary buffer [6] is provided if the coefficients of weak current asymmetry of the subcircuits CM1, CM2, CM3 satisfy the condition: $x_n = \xi_{n1} - \xi_{n2}$ , $x_p = -\xi_{p3}$.

Fig. 7 shows an equivalent circuit of the multi Op-Amp taking into account the input currents [6].

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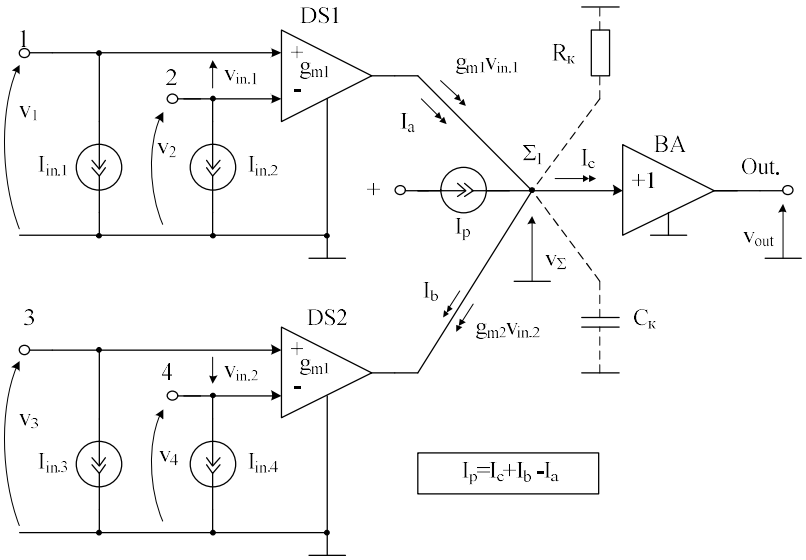


Fig.7 Equivalent scheme of the multi Op-Amp for calculating the zero level of analog devices based on it

The method of calculating the zero level in the multi Op-Amp and the main circuits of their inclusion is based on the use of an autonomous $I_p$ parameter characterizing the properties of a high-impedance node Σ1 (Fig. 7). The introduction of weak current asymmetry in typical multi Op-Amp [6], including multi Op-Amp with asymmetric reference current sources and three-stage multi Op-Amp with an inverting intermediate stage allows to reduce $V_{OS}$, at least by an order of magnitude.

Figure 8 shows the Op-Amp using an ideal BA.

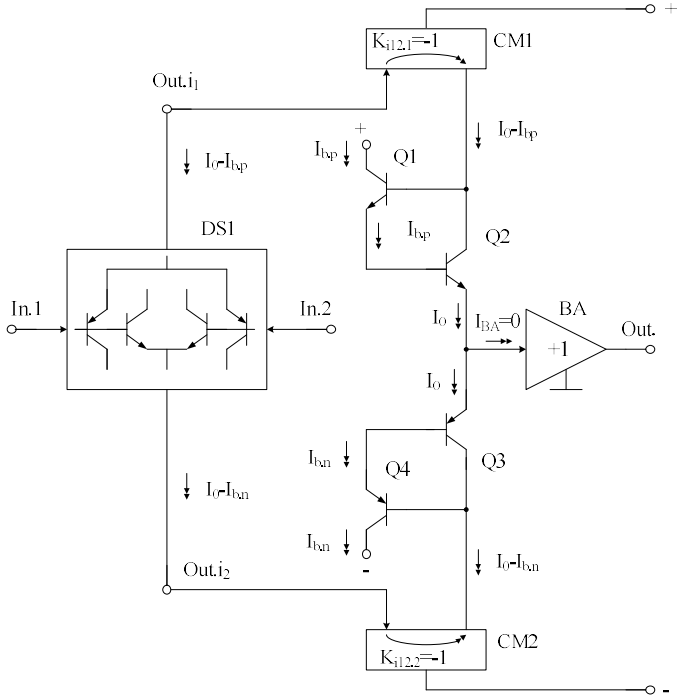


Fig.8 Op-Amp architecture with an ideal buffer [6]

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Based on the analysis of the circuit (Fig.9), it can be concluded that the methods of reducing the $V_{OS}$ of the Op-Amp based on complementary, "folded" and classical stage DS, can become the basis for the construction of many serial and promising analog microcircuits of the world's leading microelectronic firms [6], intended for use in anti-aliasing LPF.

Fig. 9 shows a complementary output stage and an example of its matching with the BA [6].

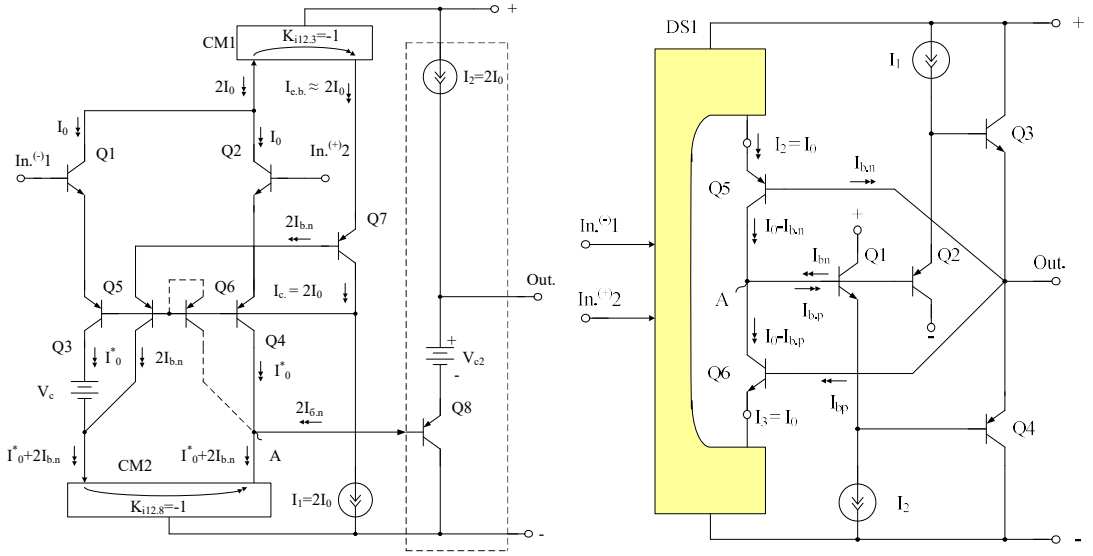


Fig.9 Complementary output stage (a) and an example of its matching with a complementary BA (b)

Fig. 10 shows the architecture of a precision Op-Amp based on a "folded cascode" and the practical implementation of the scheme [6].

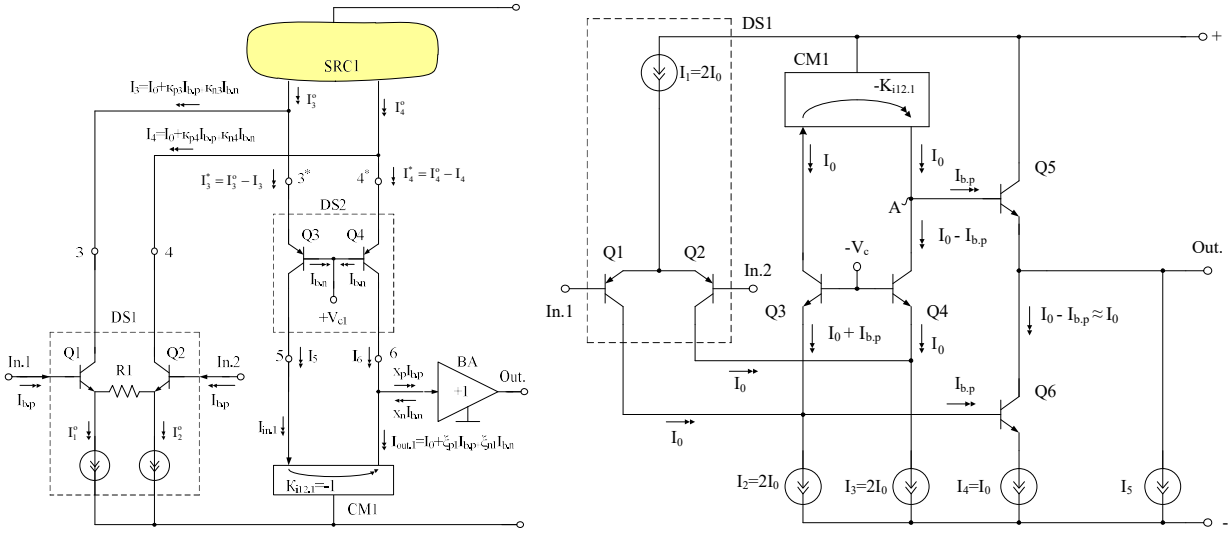


Fig.10 Generalized architecture of a precision Op-Amp based on an "folded cascode" (a) and an example of the implementation of a practical scheme (b)

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The developed circuitry of $V_{OS}$ compensation circuits and the formation of specified current asymmetry coefficients for classical stage Op-Amp prototypes [6] allows us to assert that the conditions for $V_{OS}$ compensation in precision Op-Amps based on classical stage DS can be represented as the following restrictions:

$$\begin{cases} k_{n3} + k_{n5} + \xi_{n1} + x_n = k_{n6} + k_{n4} \\ x_p + k_{p6} + k_{p4} = k_{p3} + k_{p5} + \xi_{p1} \end{cases}, \quad (5)$$

where k, ξ , x – are the scale coefficients at base currents $I_{b.n}$, $I_{b.p}$, characterizing the offset of the zero levels of subcircuits DS1, CM1 and BA, IS2.

## 4. Computer simulation of GaAs Op-Amp with $V_{OS}$ compensation

Fig.11 shows an operational amplifier developed by GaAs based on identical JFET current dynamic loads [7].

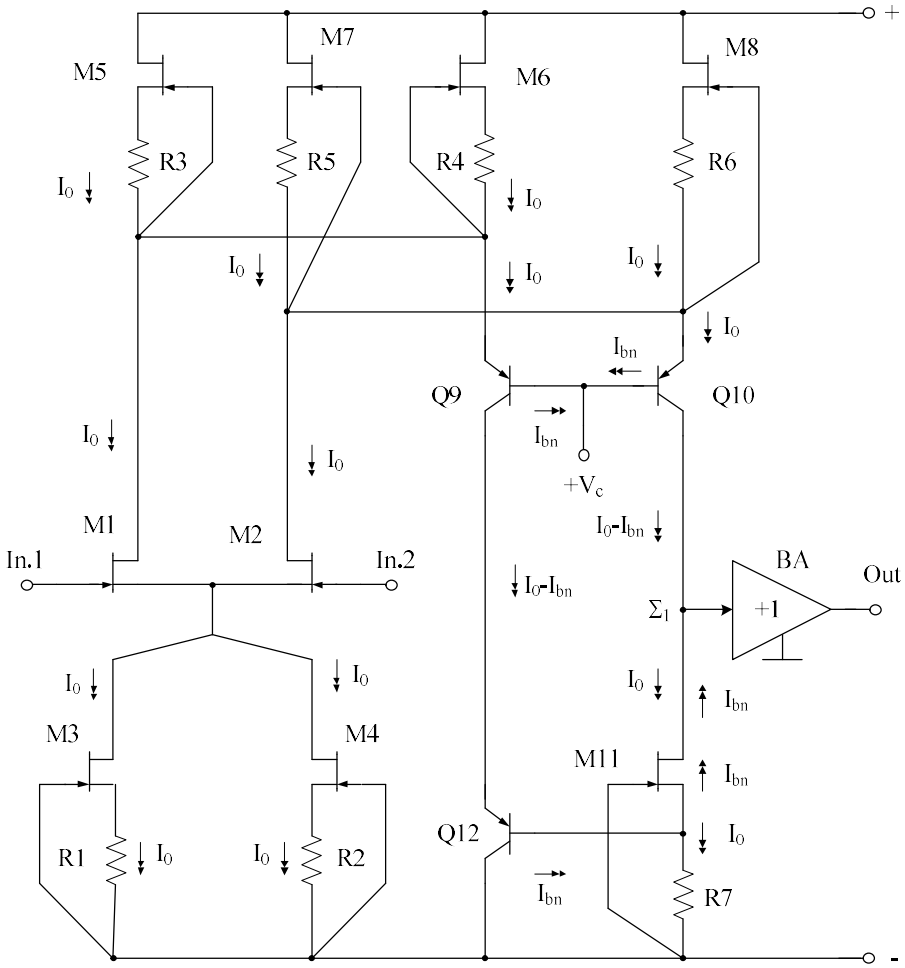


Fig.11 BiJT JFET GaAs operational amplifier

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For this Op-Amp circuit, the following basic static current equations can be written:

$$I_{d1} = I_{d2} = I_0 = \frac{U_{gs.3}}{R_1} = \frac{U_{gs.4}}{R_2} = \frac{U_{gs.5}}{R_3} = \frac{U_{gs.6}}{R_4} = \frac{U_{gs.8}}{R_6} = I_{e.9} = I_{e.10}. \quad (6)$$

$$I_{c.9} = I_{c.10} = I_0 - I_{bn}. \quad (7)$$

$$I_{s.11} = I_0 - I_{bn} = I_{d.11}, \quad (8)$$

where $I_{bn} = \frac{I_0}{1+\beta_n}$ – is the base current of the p-n-p transistor, $\beta_n$ – is the current gain of the base of the p-n-p transistor.

For a high-impedance node Σ1 based on the Kirchhoff equation can be written:

$$I_{c.10} = I_{d.11} - I_{BA} \approx I_p\ , \quad (9)$$

where $I_p$ – is the difference current in node Σ1, the presence of which affects the systematic component of the zero offset voltage of the Op-Amp:

$$V_{OS} = \frac{I_p}{S_\Sigma} = \frac{I_{c.10} - I_{d.11} - I_{BA}}{S_\Sigma}, \quad (10)$$

where $S_\Sigma$ is – the steepness of the conversion of the input differential voltage of the Op-Amp into the current of the high-impedance node Σ1, $I_{BA} = 0$ is the input current of the buffer amplifier:

$$S_\Sigma = \frac{I_{\Sigma 1}}{V_{in.}} = \frac{S_1 \cdot S_2}{S_1 + S_2} \cdot \alpha_{10}, \quad (11)$$

where $S_1 = S_2$ – is the steepness of the drain characteristic M11, $\alpha_{10} \approx 1$ is the base current gain Q10.

Substituting the values of the currents $I_{c.10}$, $I_{d.11}$ from equations (7), (8) into equation (10), we find that in the proposed Op-Amp circuit, the systematic component of the zero offset voltage is close to zero.

This conclusion is confirmed by the results of computer simulation of the Op-Amp in the LTSpice environment (Fig.12, Fig.13) on the gallium arsenide technological process of the Minsk Research Institute of NAN Radio Materials at R1÷R6 = 5 kOhm, V1 = 5 V, C2 = 3 pF, vcc = 10 V, vee = -10 V.

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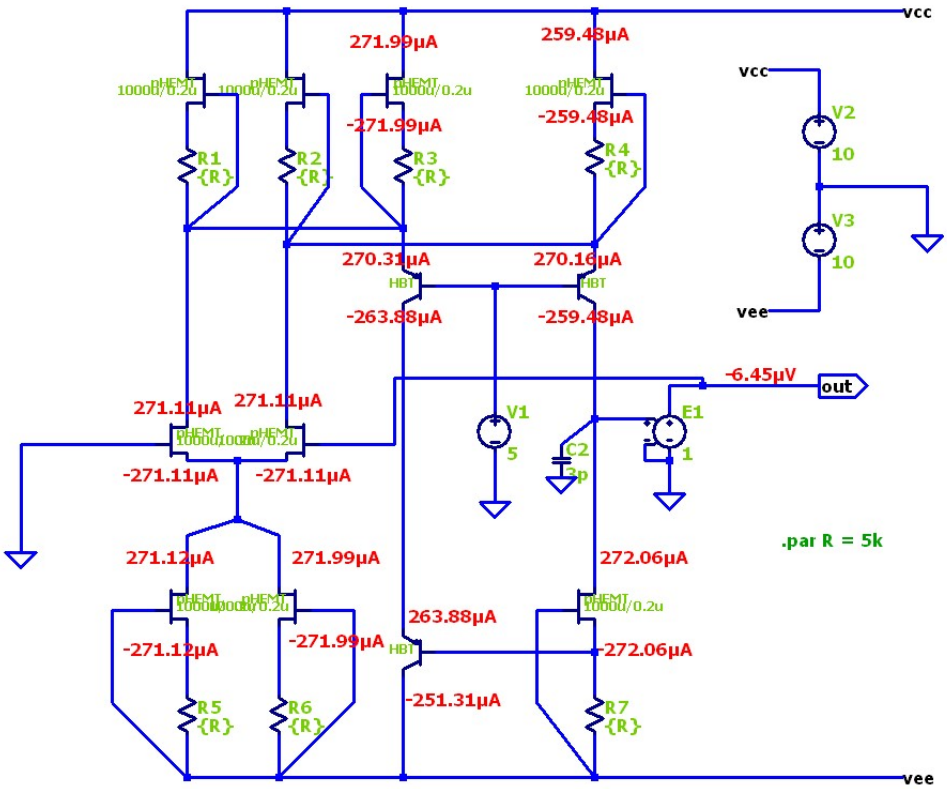


Fig.12 Static mode of Op-Amp transistors (Fig.5) in the LTSpice environment at R1÷R6 = 5 kOhm, V1 = 5 V, C2 = 3 pF, vcc = 10 V, vee = -10 V

Fig. 13 shows the frequency response of the coefficient gain (Gain) by the Op-Amp voltage in Fig.12 at R1÷R6 = 5 kOhm, V1 = 5 V, C2 = 3 pF, vcc = 10 V, vee = -10 V.

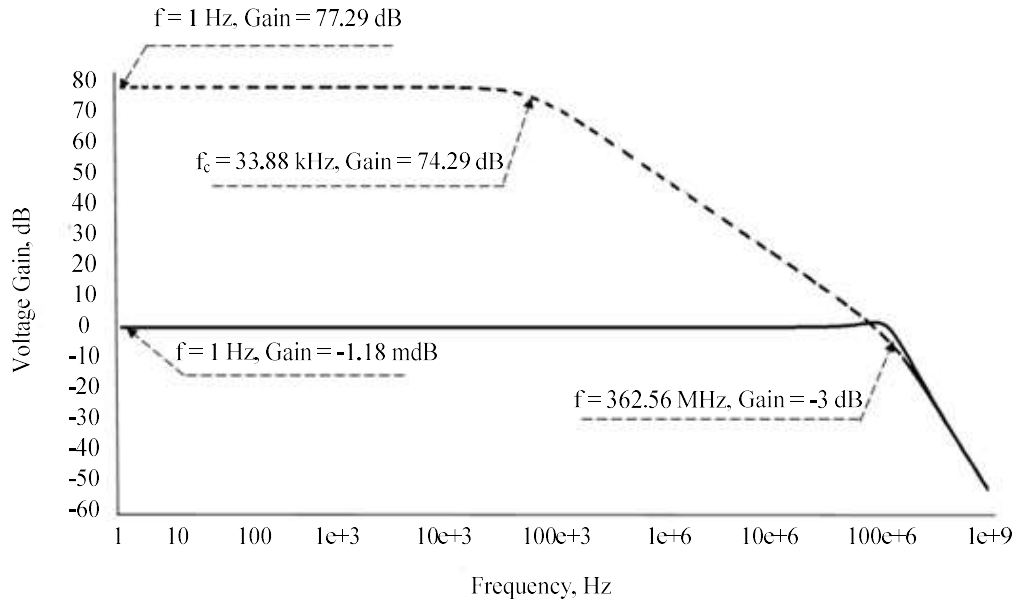


Fig.13 Frequency response of the Gain at the Op-Amp voltage (Fig.12) at R1÷R6 = 5 kOhm, V1 = 5 V, C2 = 3 pF, vcc = 10 V, vee = -10 V

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A comparative analysis of the graphs in Fig. 12 and Fig. 13 shows that the proposed circuit solutions (Fig. 11) give an increased gain of more than 77 dB. In addition, due to the developed approaches to minimizing $V_{OS}$ due to the influence of β transistors in the circuit in Fig.12, a sufficiently small value of the systematic component of the zero offset voltage (6.45 uV) is obtained (Fig. 12). At the same time, the bandwidth of the Op-Amp at the level of -3 dB is 33.88 kHz.

## Conclusion

The developed methods for describing and forming the given coefficients of weak current asymmetry of typical Op-Amp functional units and their study in precision LPF make it possible to minimize the component of the zero offset voltage due to the influence of β transistors. It is shown that the minimum value of $V_{OS}$ is realized only if the Op-Amp is "developed" from functional nodes with strictly defined coefficients of weak current asymmetry. The developed methods of matching the high-impedance node of the Op-Amp and the buffer amplifier with the help of special correcting $SCM^p$ and $SCM^n$ multipolars provide targeted formation of coefficients of weak current asymmetry in Op-Amp circuits with a specific construction of a buffer amplifier.

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