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Article

A Reliability-Enhanced Differential Sensing Amplifier for Hybrid CMOS/MTJ Logic Circuits

Chengzhi Wang ‡, Huiquan Wang ‡, Dongsheng Wang, Jian Fang, Lu Wang and Guangda Zhang *

National Innovation Institute of Defense Technology, Academy of Military Sciences, Beijing 100071, China; chengzhi_wang@buaa.edu.cn(C.Z.W.);

* Correspondence: zhanggd_nudt@hotmail.com; Tel.: +86-010-6671-6694

‡ These authors contributed equally to this work.

Abstract: Recently, hybrid logic circuits based on magnetic tunnel junctions (MTJs) have been widely investigated to realize zero standby power. However, such hybrid CMOS/MTJ logic circuits suffer from a severe sensing reliability due to the limited tunnel magnetoresistance ratio (TMR≤150%) of the MTJ and the large process variation in the deep sub-micrometer technology node. In this paper, a novel differential sensing amplifier (DSA) is proposed, in which two PMOS transistors are added to connect the discharging branches and evaluation branches. Owing to the positive feedback realized by these two added PMOS transistors, it can achieve a large sensing margin. By using an industrial CMOS 40 nm design kit and a physics-based MTJ compact model, hybrid CMOS/MTJ simulations have been performed to demonstrate its functionality and evaluate its performance. Simulation results show that it can achieve a smaller sensing error rate of 9% in comparison with the previously proposed DSAs with the TMR ratio of 100% and process variation of 10%, while maintaining almost the same sensing delay of 74.5 ps and sensing energy of 1.92 fJ/bit.

Keywords: hybrid logic circuits, magnetic tunnel junction, differential sensing amplifier, sensing margin

1. Introduction

As the technology node continuously scales down, the CMOS-based logic circuits suffer from high standby power consumption induced by the increasing leakage current. To address this issue, some researchers proposed the non-volatile logic circuits, which embed the emerging non-volatile memory (eNVM) devices into the CMOS-based logic circuits to realize zero standby power[1–3]. Among them, the magnetic tunnel junction (MTJ) is preferable, because of its high speed, long data retention, nearly infinite endurance, great scalability and good compatibility with CMOS process technology, in comparison with other eNVM devices[4–6]. Using the MTJs as the non-volatile storage elements, several non-volatile logic circuits, such as magnetic flip-flop, magnetic look-up-table and magnetic full-adder[7–10], have been proposed.

One critical issue in these hybrid CMOS/MTJ logic circuits is to correctly sense the information stored in the MTJ[11–14]. So far, various differential sensing amplifiers (DSAs) have been proposed, in which two MTJs with opposite resistance state are employed to represent one bit. For example, the pre-charge sensing amplifier (PCSA) circuit [15], as shown in Fig. 1(a), can achieve high sensing reliability (10^{-5} at 90 nm), small sensing delay (∼125 ps) and low sensing energy (∼1 fJ/bit). However, as the CMOS technology shrinks below 45 nm, the sensing reliability gets worse and worse (e.g., 79% at 40 nm) due to the increased process variation. To overcome this issue, a separated PCSA (SPCSA) [16] is proposed as shown in Fig. 1(b), which can improve the sensing reliability (82% at 40 nm) while retaining high sensing speed and low sensing energy dissipation. However, its sensing margin is still limited due to the small TMR ratio of the MTJ. To improve the sensing margin, a reliability-enhanced SPCSA (RESPCSA) [17] is proposed as shown in Fig. 1(c), which can further improve the sensing reliability (84% at 40 nm). However, it is still not sufficient for reliable logic circuits. In this paper, we propose a novel differential sensing amplifier based on the RESPCSA, in which two PMOS transistors are added to

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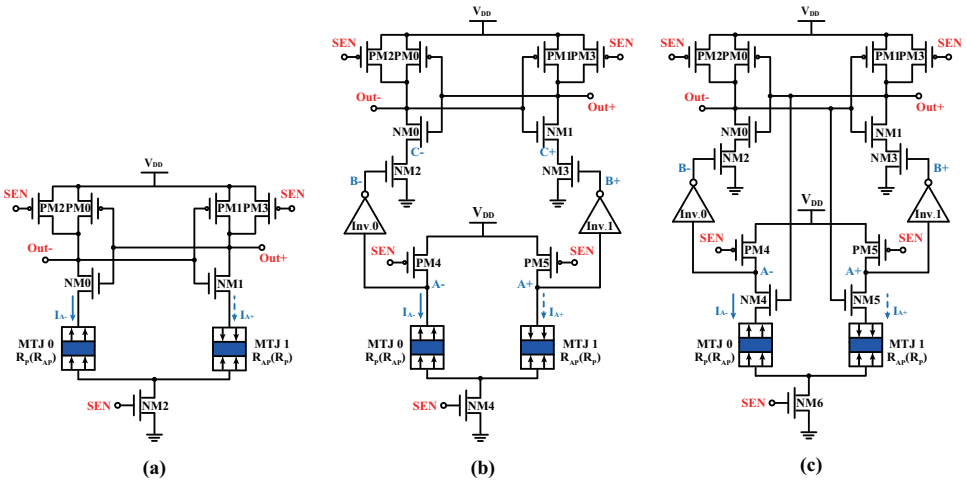

Figure 1. Schematics of (a) PCSA [15] (b) SPCSA [16] and (c) RESPCSA [17].

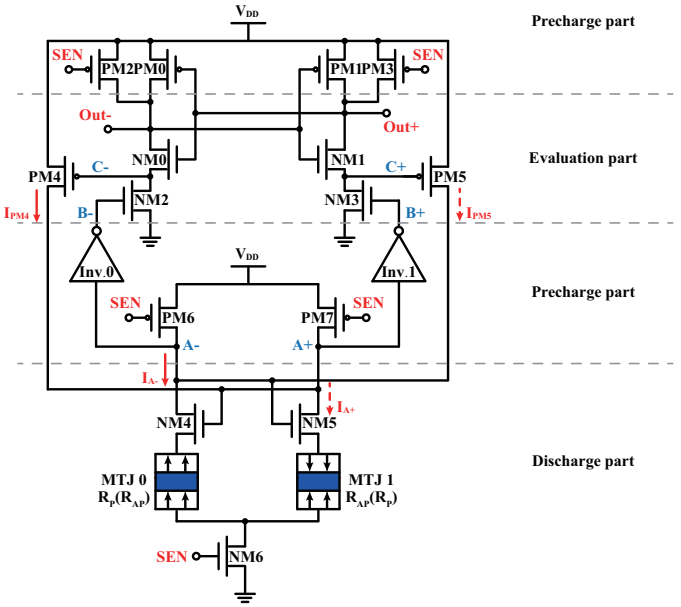

Figure 2. Schematic of the proposed sensing amplifier.

connect the discharging branches and evaluation branches. By using the positive feedback of two PMOS transistors, the proposed DSA is envisioned to obtain a large sensing margin, thereby achieving high sensing reliability.

The remainder of this paper is organized as follows. Section II describes the proposed novel differential sensing amplifier and its operation. Then, Section III demonstrates its functionality and evaluate its performance. Finally, we conclude this paper in Section IV.

2. Proposed Reliability-Enhanced Differential Sensing Amplifier Circuit

Fig. 2 shows the proposed reliability-enhanced differential sensing amplifier (REDSA) circuit. Similar to the previous RESPCSA, the proposed REDSA also includes three operation phases, i.e., pre-charging phase, discharging phase and evaluation phase, depending on the control signal "SEN". From the perspective of the circuit configuration, the main difference is that two PMOS transistors PM4 and PM5 are added to connect the discharging branches and evaluation branches. As a result, two positive feedback loops can be formed and a large sensing margin can be achieved, which will be demonstrated in Section III. In the following, we will introduce its sensing operation in detail.

When the "SEN" is set to '0', the proposed REDSA enters into the pre-charging phase. The PM2-PM3 and PM6-PM7 turn on and the NMOS transistor NM6 is in off state. As a

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result, the node A (A+ and A-), C (C+ and C-) and Out (Out+ and Out-) are charged to V_{DD}. When the "SEN" goes to '1', the proposed REDSA goes into the discharging phase. The NM6 turns on, and both the node A+ and A- begin to discharge but with different speed due to the resistance difference between their individual discharging branches, resulting in a voltage difference (ΔV_A) between them. Then, the ΔV_A can be inversely amplified by both the inverter 0 (Inv.0) and Inv.1, which enables the node Out+ and Out- to discharge with different speed as well as the node C+ and C-, leading to a voltage difference ΔV_{Out} and a voltage difference ΔV_C. Such voltage difference ΔV_C can in turn enlarge the ΔV_A thanks to the positive feedback of the PM4 and PM5. Once one of the node Out+ and Out- becomes less than the threshold voltage of the cross-coupled inverters (composed of the PM0-NM0 and PM1-NM1), the proposed REDSA enters into the evaluation phase. Finally, one of the node Out+ and Out- will continue discharging to GND, while the other one will be charged to V_{DD} eventually. For example, when the MTJ0 is in high resistance (R_{AP}) state and the MTJ1 in low resistance (R_P) state, the node Out+ will be discharged to GND and the node Out- will be charged to V_{DD} and vice versa.

3. Functional Verification

By using a physics-based MTJ compact model [18–20] and an industrial CMOS 40 nm design kit, hybrid CMOS/MTJ simulations have been performed to demonstrate its functionality and evaluate its performance. The key parameters of the compact MTJ model are listed in Table I.

Table 1. The Key Parameters of the MTJ in Simulations

Parameter	Description	Default Value
t_{ox}	Oxide barrier thickness	0.85 nm
t_f	Free layer height	1.3 nm
Area	MTJ surface	$40nm * 40nm * \pi/4$
V	Volume of free layer	$Area * t_f$
R.A	Resistance*Area product	$5.0\Omega \cdot \mu m^2$
TMR (0)	the TMR ratio with zero V_{bias}	100%
Δ TMR	the TMR ratio variation	3%
Δ tsl	Variation of free thickness	3%
Δ t_{ox}	Variation of oxide barrier thickness	3%

Fig. 3(a) shows the transient simulation waveforms of the proposed REDSA, where the MTJ0 is in low resistance state and the MTJ1 in high resistance state. As seen, during the pre-charging phase ("SEN" = 0V), the node (A+,A-) and (Out+,Out-) are charged to V_{DD}. When the "SEN" rises to '1', it enters into the discharging phase. And the node A+ and A- begin to discharge but with different speed, resulting in a voltage difference ΔV_A. Owing to the positive feedback of the added two PMOS transistors, the ΔV_A is enlarged after the point Ml (or M2). Then, this enlarged ΔV_A is amplified, inducing a large voltage difference ΔV_{Out}. As a result, the node Out- firstly becomes less than the threshold of the cross-coupled inverters. Then, the proposed REDSA enters into the evaluation phase, the node Out- continues discharging after the point M10 and the Out+ is charged after the point M9. As seen, the proposed REDSA can achieve a large sensing margin of 732.6 mV (the voltage difference between the point M9 and M10) and a small sensing delay of 74.5 ps (taken from the point M0 to M11). Since the sensing delay is less 75 ps, it can work with a high clock frequency up to 6.7 GHz. Fig. 3(b) confirms that there is no static current during the sensing operation, only dynamic charging and discharging current. The total power per bit sensing operation of the proposed REDSA is about 1.92 fJ.

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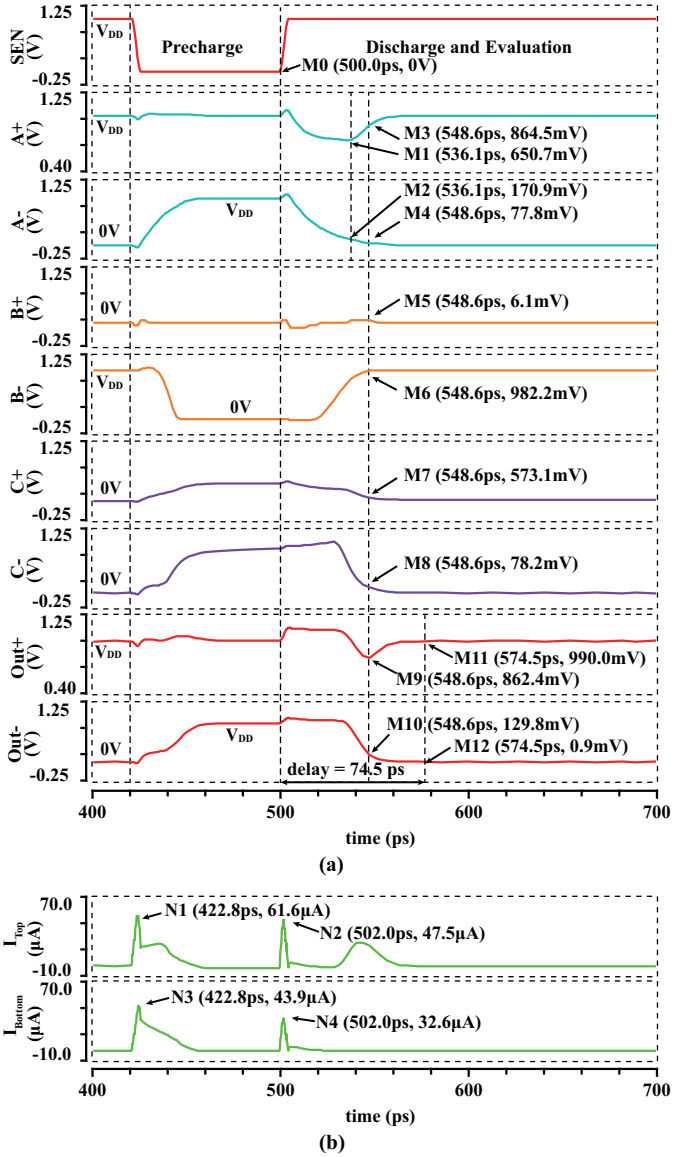

Figure 3. (a) Transient voltage simulation waveforms of the proposed REDSA. (b) Currents that flow through the proposed REDSA.

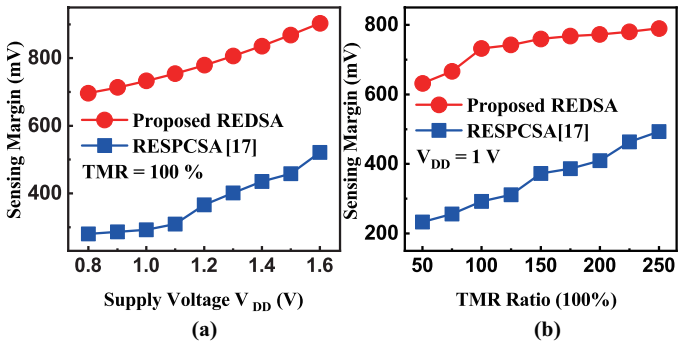

Figure 4. Comparison of the sensing margin of the proposed REDSA and the RESPCSA with respect to different supply voltages (a) and TMR ratios (b).

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4. Performance Analysis and Comparison

4.1. Reliability Analysis and Comparative Discussion

Firstly, we investigate the sensing margin of the proposed REDSA with respect to different supply voltages. As shown in Fig. 4(a), with the increase of the supply voltage, its sensing margin can be improved. Compared to the previous RESPCSA in [17], the proposed REDSA can achieve a very larger sensing margin, even with a small supply voltage. For example, the sensing margin can reach 696 mV when the supply voltage of 0.8 V, while it is only about 280 mV for the RESPCSA. Then, the influence of the TMR ratio on the sensing margin is also investigated as shown in Fig. 4(b). As seen, the sensing margin increases with the increase of the TMR ratio. However, even with a small TMR ratio of 50%, the sensing margin of the proposed REDSA can reach up to 632 mV, which is very larger than that of the RESPCSA.

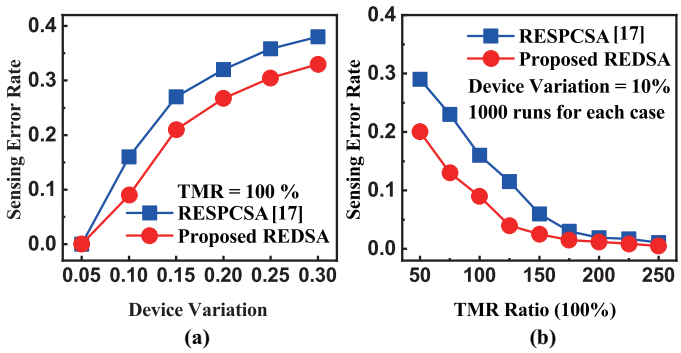

Figure 5. Comparison of the sensing error rate of proposed REDSA and the RESPCSA with respect to different device variation (a) and TMR ratios (b).

To evaluate the sensing reliability of the proposed REDSA quantitatively, Monte-Carlo statistical simulations (1000 runs per case) have been performed with consideration of the 1σ probability distributions of the CMOS transistors fixed by the CMOS process manufacturer and 3% process variations of MTJ, including TMR ratio, free layer thickness and oxide barrier thickness. Fig. 5(a) shows the impact of the device variation on the sensing error rate (SER), where the TMR ratio of 100%. As seen, the proposed REDSA exhibits a greater tolerance to device variation in comparison with the RESPCSA. Additionally, we also evaluate the SER with respect to the TMR ratio as show in Fig. 5(b). As seen, the proposed REDSA can provide a much higher sensing reliability in comparison with the RESPCSA when the TMR ratio is less than 150%.

4.2. Layout of the Proposed REDSA

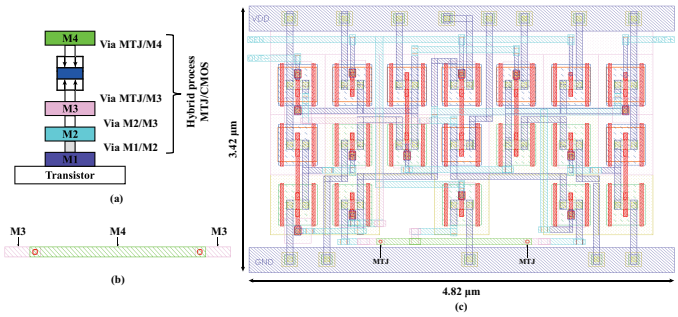

Figure 6. (a) The MTJ nano-pillar is implemented above CMOS logic circuit at 3D back-end integration process between the third metal level (M3) and the fourth metal level (M4). (b) The standard cell for one logic bit, which is composed of two complementary MTJs. (c) Layout of the proposed REDSA, where two MTJs in the layout are marked out in the figure.

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Hybrid CMOS/MTJ process can be used to fabricate MTJs as they can be embedded above CMOS circuits. As shown in Fig. 6 (a), the MTJ device can be fabricated between the third metal level (M3) and the fourth metal level (M4) using 3D back-end integration process. Fig. 6 (b) shows the standard cell for one logic bit, which is composed of two complementary MTJs. MTJ bottom electrode connects to the third metal level (M3) and MTJ top electrode connects to the fourth metal level (M4). Fig. 6 (c) shows the layout of the proposed REDSA, which is drawn with the 40 nm layout design rules. The effective area of the proposed REDSA is about 16.48 μm^2.

4.3. Performance Comparison

Table II summarizes the performance comparison of the proposed REDSA and the previous DSAs. As seen, compared to the previous DSAs, the proposed REDSA can achieve a smaller sensing error rate, while retaining almost the same sensing delay of 74.5 ps and sensing energy of 1.92 fJ per bit. Although the main drawback of the proposed REDSA is its relatively larger area, multiple non-volatile memory cells can share one sensing amplifier by using multi-context hybrid CMOS/MTJ logic circuits[21,22].

Table 2. Performance Comparison with TMR Ratio of 100% and Process Variation of 10%

	PCSA [15]	SPCSA [16]	RESPCSA [17]	This work
Technology [nm]	40	40	40	40
# of Transistor	7	15	17	19
Latency [ps/bit]	49.1	56.4	66.8	74.5
Sensing Error Rate	0.21	0.18	0.16	0.09
Sensing Energy [fJ/bit]	0.847	1.68	1.83	1.92

5. Conclusion

In this paper, we propose a novel reliability-enhanced differential sensing amplifier with a large sensing margin. Hybrid CMOS/MTJ simulation results show that it can achieve a smaller sensing error rate of 9% than that of the previous differential sensing amplifiers, while retaining almost the same sensing delay of 74.5 ps and sensing energy of 1.92 fJ/bit. Materials and Methods should be described with sufficient details to allow others to replicate and build on published results. Please note that publication of your manuscript implicates that you must make all materials, data, computer code, and protocols associated with the publication available to readers. Please disclose at the submission stage any restrictions on the availability of materials or information. New methods and protocols should be described in detail while well-established methods can be briefly described and appropriately cited.

Author Contributions: Conceptualization, G.D.Z.; methodology, H.Q.W.; software, H.Q.W. and C.Z.W.; validation, H.Q.W. and C.Z.W.; formal analysis, D.S.W.; investigation, D.S.W. and C.Z.W.; resources, G.D.Z.; data curation, D.S.W. and C.Z.W.; writing—original draft preparation, C.Z.W.; writing—review and editing, J.F., L.W. and G.D.Z.; visualization, C.Z.W.; supervision, G.D.Z.; project administration, G.D.Z.; funding acquisition, C.Z.W. and G.D.Z. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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