Article

A Switched Capacitor Memristor Emulator using Stochastic Computing

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Abstract: Due to the increased use of memristors, and its many applications, the use of emulators has grown in parallel to avoid some of the difficulties presented by real devices such as variability and reliability. In this paper, we present a memristive emulator designed using a Switched Capacitor (SC), this is, an analog component/ block and a control part or block implemented using stochastic computing (SCo) and therefore fully digital. Our design is thus a mixed signal circuit. Memristor equations are implemented using stochastic computing to generate the control signals necessary to work with the controllable resistor implemented as switched capacitor.

Keywords: memristor; emulator; analog design; switched capacitor; stochastic computing; mixed signal

1. Introduction

Leon Chua defined the memristor theoretically in 1971 [1]. The term "memristor" is constructed from the words memory and resistor and completes the relationships provided by the capacitor, inductor and resistor between current, voltage, flux and charge. Leon Chua introduces therefore this fourth passive component to complete the set, proposing that the memristor is defined by a nonlinear relation between charge and flux. However, it was not until 2008 that it could be implemented [2]. Since then, its use has been increasing and its fields of application have also increased. It is a promising but very recent device, this implying that there are many studies that must be carried out to understand well the operating mechanisms and develop new technologies to avoid some of the problems presented, such as the variability and life time. It is because of the problems that the real device presents that the development of memristive emulators is booming.

The emulators reproduce the operating characteristics of the memristor by eliminating the aforementioned problems and allow for the development of more complex and reliable systems [3]. The memristor behavior which is imitated can be ideal memristor or actual device, depending on the implementation. If we are focused on their field of application, emulators have different characteristics, although there are two main lines of study: analog emulators and digital emulators.

Many works develop fully analog emulators, for example, in [4] a memristive system is implemented and results very easy to fabricate it in academic laboratories through classical electrical components from circuit theory, in [5], the emulator is implemented with transistors, resistors and diodes and it operates in passive mode. Other examples like [6] and [7] use amplifiers in their models. In general, analog systems need more power consumption, the volatility of the system is worse than in the digital case, but they present a good implementation of the variable resistance with which the emulator memristance is described.

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On the other hand, digital memristors systems emulators can be implemented in in FPGAs (or ASICS)[8–10]. Their main advantages are that they present short simulation times and better control of the emulator, however, they present a problem when implementing the variable resistance. In digital emulators it's much easier to define the model, but precision is lost (limited number of bits) and usually needs more computational power than the analog equivalent.

For many years, the scientific community has been a great interest to develop different computer architectures. It seeks, among other things to change the structure of serial calculation and perform operations in parallel. A high degree of parallelism allows for faster execution using less complex elements or using approximations even if precision is lost. Due to the large number of data and operations that must be carried out by current computer systems, the well-known Von Neumann architecture [11] is not a good election to use due to a high consumption of time of computation and energy.

One of the alternatives, like mentioned above, is to use non-deterministic computing methods, Stochastic Computing (SCo) is one of them. The use of random variables is it main characteristic. In 1956, Von Neumann introduced probabilistic logic [12], his work was based on the work of R.S. Pierce in 1952 at the California Institute of Technology [13]. The advances in the field of electronics and computing have allowed to implement it during the sixties [14,15]. Nowadays, this approach has been used in many fields like image processing [16,17], data compression[18], mathematical calculations [19,20], control [21], image processing [22], or even A/D conversion[23], among others.

In this paradigm, the representation of data is performed in a probabilistic way using boolean quantities that are switching in random way during a time. The numbers are codified in a vector of random binary numbers, whose average value will be correlated to the number represented [24]. These vectors are referred to as stochastic logic number (SLN). This representation makes possible to reduce the area occupied since complex functions occupying a large space such as multiplication can be reduced to a single logic gate with great savings in terms of power and area[25]. To create the SLN, a Random Number Generator (RNG) is needed and for the designers it is a challenge to use the lowest number of these to not increase the area of the chip. The number of RNGs is related to the fact that the operations in SCo are different depending on the encoding of the number and if the signals are correlated or not (statistical dependent or not). To guarantee uncorrelated SLNs, different RNGs must be employed to generate each stochastic signals.

In this work, we design, simulate and implement a mixed-signal memristor emulator, improving the version presented in [26]. Specifically, in this paper we improve the theoretical discussion, including the description of the stochastic blocks, and we also present some experimental results. The proposed emulator consists of two blocks, taking advantage of the best features of each design part. In the analog block a Switched Capacitor is used to implement a variable resistor, and in the digital one, that is the control block, we use stochastic computation. The simulation is done with Matlab to implement the functionality of both the analog block, similar to that used in [27], and of the control block. For the experimental implementation a quadruple analog switch HCF4066FE and a DE0-Nano FPGA have been used.

This paper is organized as follows: the next section describes the generalities of memristors, memristor emulators and stochastic logic operations; in the third section the model is developed and simulated; the fourth section deals with the experimental implementation; and, finally, the last section discusses the work.

2. Theoretical Background

2.1. Memristor Mathematical Description

A memristor is a two terminal device whose resistance (conductance) can change its value when a voltage or current signal is applied. In addition, the value of the resistance (conductance) of the device also depends on its past history and is named memristance (M) (memconductance (G)). The concept of the memristor was extended by Chua in 1976

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to memristive systems to explain the behavior of observed systems [28], for instance, in nature. Nowadays the classification of memristors includes ideal, generic and extended memristor [29].

The most general class is the extended memristor, and include the others. The dynamic of this class is described using internal variables that determine the internal state of the memristor, these variables, can be for example, temperature or geometrical parameters depending on the system. The memristor can be voltage or current controlled depending of the input source. On the other hand, in [30] Corinto et al. proposed a mathematical description in the charge flux domain instead voltage and current domain. We use for our emulator the equations describing a voltage-controlled extended memristor in the charge flux domain, these are:

$$i = G(\phi, v, \mathbf{x}) \cdot v \tag{1}$$

$$\frac{d\mathbf{x}}{dt} = \mathbf{g}(\phi, v, \mathbf{x}) \tag{2}$$

$$\frac{d\phi}{dt} = v \tag{3}$$

The memconductance (G), which can be nonlinear, is the inverse of the memristance of the device, v is the applied voltage, i is the current, ϕ is the voltage first momentum or flux and $\mathbf{x}$ represents the extra state variables.

Finally, it is also important to mention that the memristors present some characteristic fingerprints distinguishing those of others dynamic systems [30,31]:

1. As Leon Chua noted in [32]: "If it's NOT pinched, it's NOT a memristor". The *i-v* curve obtained when a periodic signal with zero DC component (voltage or current) is applied to the memristor shows a pinched (at the (v=0,i=0) point) hysteresis loop.
2. The area of the hysteresis loop should tend to zero for higher frequencies, as noted in [30]. The behavior at low frequency depends on the specifics of the memristor, and it may even exist a frequency where the loop area is maximum [3].

On the other hand, the emulator function must be to mimic the memristor behavior, this is to show it fingerprints. The emulator can be implemented in analog, digital or mixed. It is crucial that the circuit implements, among others, the internal state variables, (vector $\mathbf{x}$) in Eq. (1) and (2). These internal variables must be included as electrical variables in the emulator and cannot interact with the outside and they are the used, along with the voltage and the flux, to determine the actual value of the equivalent memconductance (G) or memristance (M).

2.2. Stochastic Logic Operations

Four ways are used to encode numbers in SCo: Unsigned Classical Stochastic Encoding (UCSE), Signed Classical Stochastic Encoding (SCSE), Unsigned Extended Stochastic Encoding (UESE) and Signed Extended Stochastic Encoding (SESE) [33,34]. Depending of the encoding used, the functions will need to be implemented using different simple logical blocks. For instance, when using UCSE, an AND gate is used to implement the product of two inputs, while a XNOR gate performs that operation when using the SCSE encoding, as shown in Figure 1. Moreover, the same logical gate can perform different operations depending on whether the random signals generated are correlated or not. As an example, with USCE encoding, a two inputs AND gate is used to implement a multiplication for uncorrelated inputs, while it provides the minimum value of the two inputs it they are correlated. In the present work, we will be using SCSE and, thus, our numbers will lay in the real [-1..1] domain. Thus, multiplication requires the use of an XNOR gate.

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Figure 1. Basic implementation scheme of a SC multiplier in the [0..1] range (AND gate, left) and in the [-1..1] range (XNOR gate, right).

Performing an addition is slightly more complex, because numbers with a probability higher than one cannot be represented, and we may need to add 1+1=2. Thus, it is better to implement an alternate form as $(x+y)/2$, which at most will output a value of 1. This operation is usually implemented using a multiplexer, as shown in Figure 2 (a), where the p(0.5) means a signal with a probability of 0.5 to be '1' or '0'. This signal can be generated using one of the bits from the RNG, thus needing no additional circuitry. The same gate is used for the [0..1] and the [-1..1] domains.

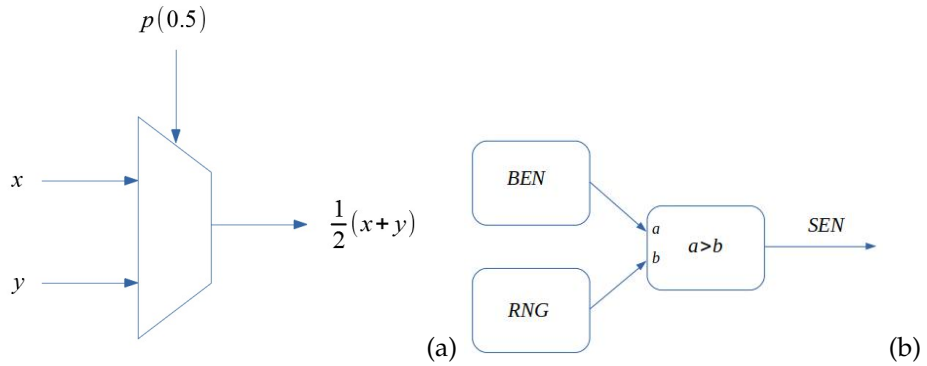

Figure 2. Basic implementation schemes (a) of a SC adder using a multiplexer and (b) a Stochastic Number Generator (SGN) which converts a Binary Encoded Number (BEN) to a Stochastic Encoded Number (SEN), using a Random Number Generator (RNG).

Other more complex operations (division[21], square roots[21], etc...) may also be found in the literature, but are not presented here for the sake of clarity. Finally, the conversion of a number encoded as a classical number can be translated to a stochastic representation using the schema presented in Fig. 2.

3. Memristor emulator design

3.1. Theoretical Design

As mentioned above, our system has been implemented using an analog block and a digital one. Figure 3 shows the analog block, which is a typical switched capacitor module (SC). The equivalent resistance R_{eq} is described by Eq. (4). In this case, both control external signals S_1 and S_2 are equal, with a lag of 180 deg. [35].

$$R_{eq} = \frac{1}{f_S C}\frac{1+e^{\left(\frac{D\,T}{\tau}\right)}}{1-e^{\left(\frac{D\,T}{\tau}\right)}} \tag{4}$$

T and f_s are the period and the frequency of the controlling signal S_1 and S_2, D is the duty cycle with values between 0 and 1, C is the capacitance value and τ is the time constant, this is, $R_{tot}C$ where C is the capacitor and R_{tot} is the total resistance of the circuit taking into account the parasitic ones.

For our design, in the charge flux domain, it is necessary to calculate the flux from the voltage of the terminals of the SC as a first step. Once this is done, then the relations between flux and charge are used to obtain the duty cycle (D) that varies the equivalent resistance of the SC. The digital block is the responsible for all these steps.

For this purpose, a series of approximations shall be done to Eq. (4). The conductance (G) ($G = 1/R_{eq}$) can be rewritten as:

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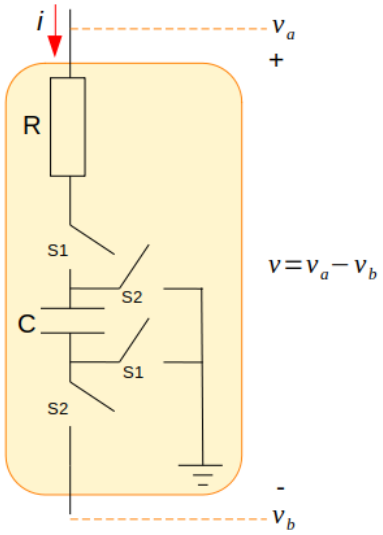

Figure 3. Switched capacitor (SC) circuit schematic.

$$G = f_S C \frac{e^{(-\frac{x}{2})} - e^{(\frac{x}{2})}}{e^{(-\frac{x}{2})} + e^{(\frac{x}{2})}} = f_S \cdot C \cdot tanh(\frac{x}{2}) \tag{5}$$

where x=DT/τ.

A first order Maclaurin expansion of $tanh(x/2)$ can be used, taking into account that the control signals used must be faster than the time the system takes to decay, so the final equation for the conductance G is:

$$G = f_S C \frac{DT}{2\tau} \tag{6}$$

It is important to notice that this last equation implies that conductance is linearly dependent on the duty cycle D.

To calculate the flux, the digital block converts previously each voltage terminal of the SC (v_a and v_b in Fig.3), to non correlated random values. Then, the corresponding value $v_a - v_b$ is accumulated into a counter, which acts as the integrator. Notice that since we are using stochastic computing this up/down counter needs to count only one up ($v_a > v_b$), one down ($v_a < v_b$), or remain the same ($v_a = v_b$). To implement the memristor device, it is necessary to use an equation to describe the relation between flux and charge. In this work the simplest relation is used:

$$Q = M\phi^2 \tag{7}$$

where M is a constant. This equation does not include any internal variables. Applying the firth derivative of the equation, the conductance is:

$$i = 2M\phi \frac{d\phi}{dt} = 2M\phi v \implies G = 2M\phi \tag{8}$$

Matching the Eq. (6) and the Eq. (8) the relation between the duty cycle and flux is:

$$D = \frac{4M\tau}{f_S CT}\phi = K\phi \tag{9}$$

K is therefore a constant value.

To control the analog block, it is the SC, the duty cycle (D) must be used. The duty cycle is calculated by the digital block from ϕ according to Eq. 9 as a stochastic value. To use it the average value of D is calculated to determine R_{eq} with Eq. 4.

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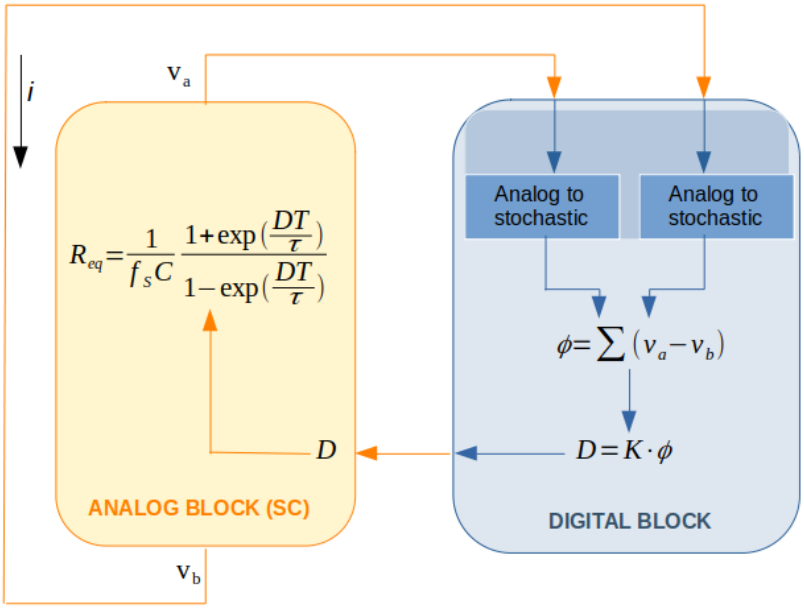

Figure 4. Swiched Capacitor Memristor Emulator (SCME) block diagram.

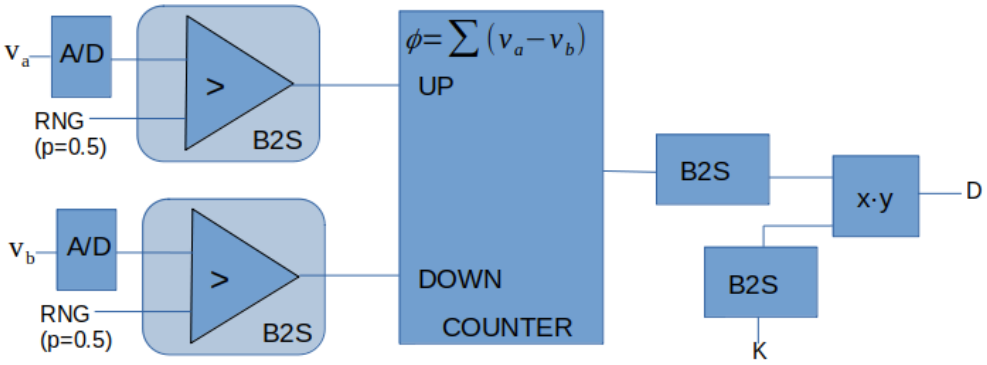

Figure 5. Control Block implementation using Stochastic Computing.

The emulator block design scheme including the two parts of the design, analog and digital, is shown in Fig. 4. The part corresponding to the digital block implemented in Stochastic Computing is shown as a circuit in Fig. 5.

3.2. Simulation Results

In order to be considered as a memristor, the emulator must present two characteristic fingerprints [3,31,32]: (1) a pinched loop, (2) whose area changes with frequency.

Figure 6 presents the $i - v$ of the emulator under inputs of different frequency, in arbitrary units. It is apparent from this figure that the curves are pinched at the origin and that the loop area changes with frequency. Thus, we can consider that the two fingerprints are present.

Because of the way it is constructed, the emulator reaches a saturation for the conductance. This is due to the maximum value of $D = 1$, and can be clearly seen at low frequencies, where the maximum value of flux is reached faster. This may also be seen in Fig. 7, where the behavior of the Q versus ϕ near the origin is quadratic, as can be expected from (7), but it is also seen that its behaviour changes to lineal after a maximum value for $D = 1$ is reached.

Finally, the current signal for different frequencies is shown in Fig. 8. As can be seen

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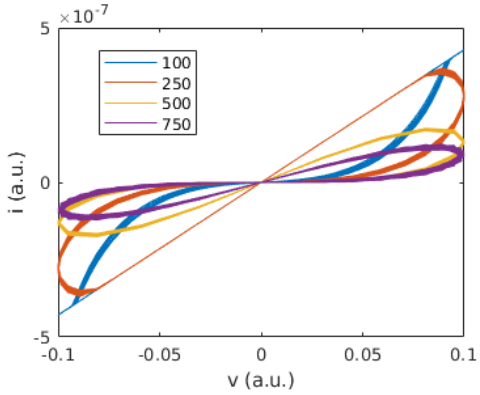

Figure 6. $i - v$ characteristic curve of the memristor implemented using Fig. 4. The different frequencies (in arbitrary units) are shown in different colors.

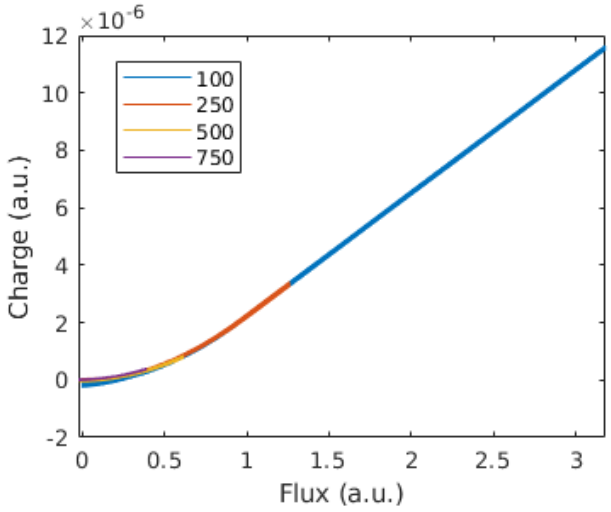

Figure 7. $Q - \phi$ characteristic of the memristor implemented using Fig. 4. The different frequencies (in arbitrary units) are shown in different colors.

there, the maximum conductance (related to the maximum value of the current) is lower for higher values of frequency, as expected.

4. Experimental Implementation

4.1. Experimental Setup

In order to test the proposed circuit, we have implemented using a setup similar to that of [27]. We have used a quadruple analog switch HCF4066FE, driven by a DE0-Nano FPGA. The analog switch has a working voltage between -0.5 V to 22 V, and can switch at a maximum frequency of 25 kHz, when the power supply is 3.3V. The FPGA generated the control signals S_1 and S_2, using two of its 3.3V digital output pins. Additionally, we have also used a 1kΩ shunt resistor, along with a 15μF capacitor. The implemented circuit is shown in Fig. 9. The conversion from analog to stochastic was performed by first converting from analog to digital using two of the on-board available A/D and then converting this digital value into stochastic, as described above.

An AFG320 arbitrary signal generator was used to generate the input signal, while two oscilloscopes where used to monitor the full system. An oscilloscope was monitoring the control signals of the HCF4066FE, while the other oscilloscope was used to monitor the voltage through the shunt resistance of 1kΩ to obtain the current, and also the input voltage.

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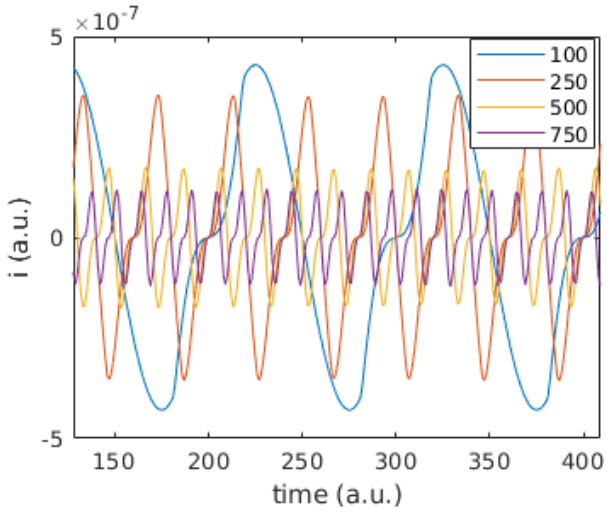

Figure 8. Current signal for different frequencies. The different frequencies (in arbitrary units) are shown in different colors.

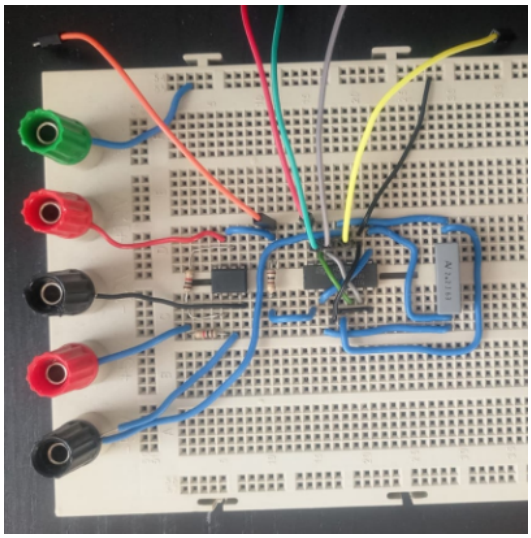

Figure 9. Physical implementation of the circuit on a prototyping board.

4.2. Experimental Results

The system has been tested using different input frequencies: 100, 200 and 400 Hz. The internal behaviour of the circuit is depicted in Fig. 10, that shows the waveform corresponding to the most significant bit of the counter and the control signal S_1 in one of these cases. It has to be noted that S_2 was generated to be exactly S_1 negated and is not shown.

The temporal behavior of the current in these three cases is shown in Fig. 11. The currents are clearly non linear because of memory: if they were nonlinear due to other effects, then they would be symmetrical, which they are not. In addition, they are showing a dependence on the frequency, as expected for a memristor.

The I-V loops are depicted in Fig 12, and they show the experimental fingerprint of a memristor: the pinched loop [32]. That means that the device has a resistive behavior (it's pinched, which means no current when no voltage is applied), and that this resistance has a memory effect (there is a loop, which means that there are two possible values of the resistance and, hence, the current, for each voltage input value).

It has to be noted that the area of the loop changes with frequency, with the higher area corresponding to the higher frequency. This behaviour is caused by the saturation of the internal counter that corresponds to the flux integral (eq. 3 and Fig. 5), which leads to a

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Figure 10. Stochastic signals generated by the control circuit. The upper signal is the most significant bit of the counter, while the lower waveform is the S_1 control signal.

linear behaviour once the maximum value is reached.

5. Discussion

In this work we have presented a flux controlled memristor emulator based on the extended memristor equations. We use a switched capacitor as the controlled resistor, this being the analog part of the design. The digital control is implemented using stochastic computing and its purpose is to calculate the flux and generate the control signal for the switched capacitor block. That is, we generate a stochastic signal whose average value is the duty cycle. This signal has been generated by using a simple nonlinear relation between flux and charge, that leads to a linear relation between the duty cycle and the flux. The emulator is thus a mixed emulator using the best properties of analog and digital emulators, showing excellent capabilities and a very easy implementation.

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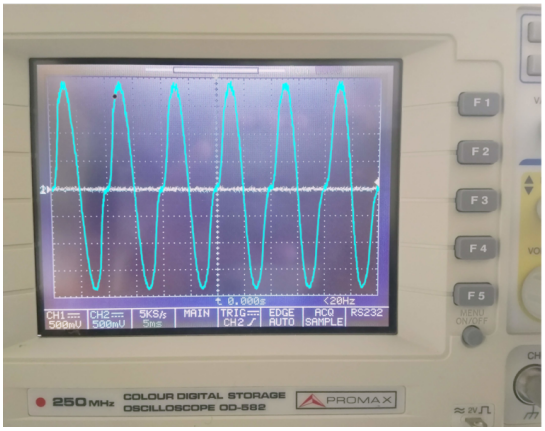
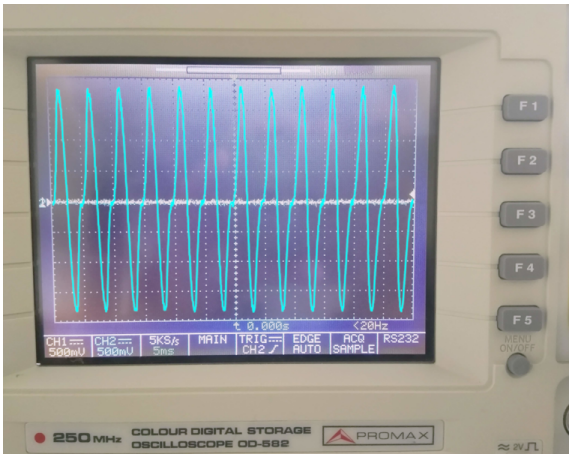
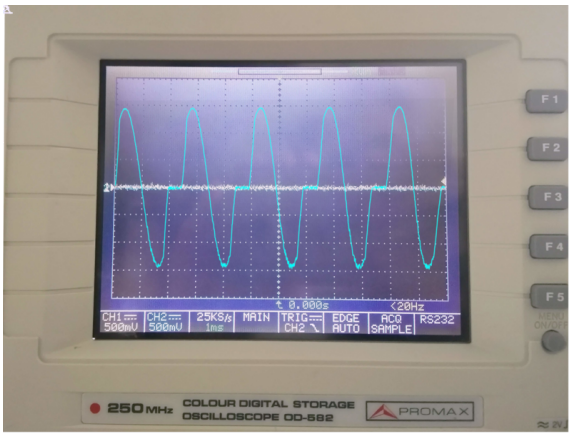


(a) 100Hz.



(b) 200Hz.



(c) 400Hz.

Figure 11. Measured current signals at different frequencies.

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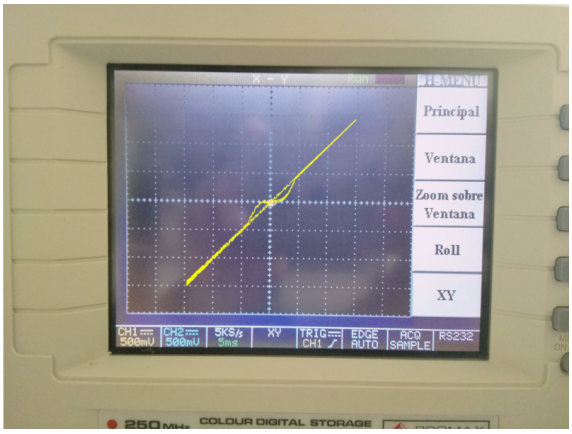
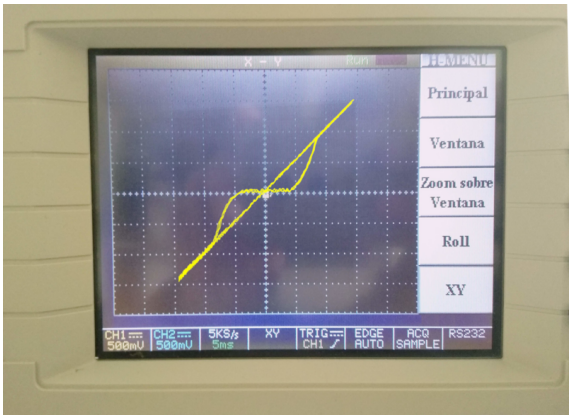


(a) 100Hz.



(b) 200Hz.

(c) 400Hz.

Figure 12. Measured I-V signals at different frequencies.

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