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# Evaluation and Improvement of a Transformerless High-Efficiency DC-DC Converter for Renewable Energy Applications Employing a Fuzzy Logic Controller

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**Abstract:** This article discusses a transformer-free, high-efficiency DC-DC converter besides renewable energy applications. The traditional buck-boost, classic Zeta, Sepic, and Cuk converter does have the benefits of a simple design, low cost, as well as the capacity to execute voltage step-up and step-down. Conversely, because of the detrimental consequences of the parasitic constraints of the device, the voltage conversion gain of the traditional DC-DC converter is much more restricted and the efficiency is also significantly smaller, whereas this proposed converter does have a higher voltage gain and efficiency because it is used in a single power switch, resulting in reduced switching losses and voltage stress. The said converter's design is very simple, which simplifies the operation control and reduces switching and conduction losses, leading to an efficiency of 97.4 percent. This converter seems to have the same capabilities as the Zeta converter, including continuous desired output current and desired buck-boost operation. Such an article offers the operation principle and steady evaluation, as well as a comparison with other existing high step-up configurations. The proposed converter employs a fuzzy logic controller, which improves the voltage level as well as reduces the time taken to set the voltage output of a conventional PI and ANN controller, especially in comparison to the FLC controller. For deployment, Experimental Result and MATLAB/Simulink has been used, and the modeling results indicate that the proposed controller performance has improved.

**Keywords:** High Voltage Gain, Transformerless, Zeta converter, Voltage stress, buck-boost, Fuzzy Logic Controller.

**Nomenclatures**

| Acronyms | Descriptions | Acronyms | Descriptions |
|---|---|---|---|
| $S$ | Semiconductor Switch | $r_{DS}$ | Switch on-state resistances (ohm) |
| $T_S$ | Time Period ($1/f_{switch}$) in Sec | $R_{F1}$ & $R_{F2}$ | $D_1$ and $D_2$ diode forward resistance(ohm) |
| $V_d, V_i, V_S$ & $V_o$ | Input & Output DC Voltage ( V ) | $V_{F1}$ & $V_{F2}$ | Diode $D_1$ and $D_2$ threshold voltages( Volt) |
| $D$ | Duty Ratio (%) | $R_{L1}$, $R_{L2}$ & $R_{L3}$ | The equivalent $L_1$ $L_2$ & $L_3$ inductor resistance (ohm) |
| $V_{C1}$, $V_{C2}$,$V_{C3}$ | Capacitor Voltage ( V ) | $r_{C1}$ $r_{C2}$ $r_{C3}$ $r_{C0}$ | The equivalent $C_1$ $C_2$ C3 Co capacitor resistance(ohm) |
| $V_{D1}$,$V_{D2}$ | Diodes Voltages( V ) | $P_{rDS}$ | The switch's condition is loss |
| $I_{L1}$,$I_{L2}$,$I_{L3}$ | Inductors Currents (A) | $P_{Sw}$ | Switching loss of the presented converter |
| $I_{C1}$,$I_{C2}$,$I_{C3}$ | Capacitor Currents(A) | $P_{Switch}$ | Total loss of the Switch |
| $M_{CCM}$ | Voltage transfer gain of CCM Mode | $P_{Loss}$ | Presented converter total loss |
| $CCM$ | Mode of Continuous Conduction | $\eta$ | Efficiency (%) |
| $DCM$ | Mode of Discontinuous Conduction | $\Delta V_{C1}$ | Capacitor voltage ripples ( V ) |
| $M_{DCM}$ | Voltage gain (in dcm mode) | $\tau_L$ | The normalized time constant of an inductor (Sec) |
| $\tau_b$ | Time constant of a boundary normalised inductor (Sec) | $FLC$ | Fuzzy Logic Controller |
| | | $ANN$ | Artificial Neural Network |

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|---|---|---|---|
| $D_{m2}$ | duty cycle (DCM Mode) | *e,de.du* | error, change in error, control output |
| *BCM* | Boundary Conduction Mode | *R Load* | Resistive |
| $K_P$ | Proportional gain | $K_i$ | Integral gain |
| $M_P$ | Maximum Overshoot | $e_{ss}$ | Steady State Error |
| $T_s$ | Settling Time | $T_p$ | Peak Time |

## 1 Introduction

The two most important energy sources seem to be fuel cells as well as photovoltaics. The voltage levels of these sources, even so, have become too small and uncertain, differing with weather patterns including solar irradiation and temperature. As a result, photovoltaic as well as fuel cell applications require high voltage gain converters [1]-[2]. The inherent voltage levels of such renewable energy sources were also considerably lower and uncertain. As a result, a high boost up converter requires maintaining and boosting the low voltage renewable input energy of the source to convert higher voltage into delivering the grid is illustrated in Figure 1. The conventional boost converter has been commonly used due to its low hardware complexity, compact configuration, and relatively cheap. Even so, this voltage gain is insufficient. While the output voltage of a standard boost converter may theoretically reach infinite as the duty ratio reaches one, the actual voltage gain is constrained by parasitic elements and gradually decreases as the duty ratio reaches one.Most of all, the main switch must limit a rising output voltage, necessitating the use of the main switch with a rising on-resistance, which tends to increase the conduction loss. Furthermore, the diode of a conventional boost converter must also obstruct the large output voltage, creating a severe major issue with reverse recovery current as well as conduction loss [3]-[6].

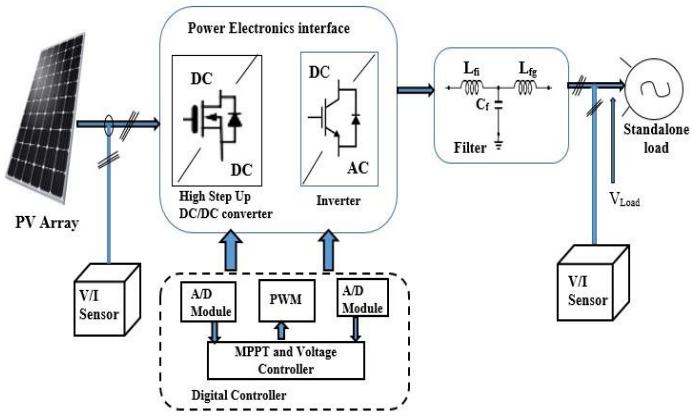


**Figure 1**. Renewable energy power conversion system general block diagram

These several improvements besides DC/DC converters are compared to provide higher voltage conversion ratios. Switched-capacitor converters are such an approach to increase the voltage gain in this case. Analyzed, the authors developed a few design guidelines helpful for achieving various switched capacitor converters. Therefore many modular multilevel inverters depending on a switched capacitor cell theory have been described, with a soft-switched scheme that is used to reduce electromagnetic interference and switching losses. The switched capacitor methodology, on the other hand, causes the switch to suffer from serious current transient and large conduction losses. Besides that, numerous switched capacitor cells have been necessary to accomplish the incredibly large step-up conversion, increasing the circuit complexity [7]-[9].

Combined inductor--based converter's are also another option for implementing high boost up gain, so the combined inductor's turn ratio could be used as further control independence to strengthen the voltage gain. Even so, when using single-phase single-stage coupled inductor-based converters, the current ripple of the input has been substantially higher. That may reduce the useful life of the insight electrolytic capacitor. However, this combined inductor converter would have had some issues with leakage inductance as well as pulsating input current [10]-[12].In [13], High voltage converters have been introduced in transformerless buck-boost converters. That although the converters should not use coupling inductors. The converter's switches and diodes had too much difficulty and stress. Thus the converter's losses are considerable. A high step-up converter without transformers has been addressed in [14], one main switch and capacitor technology would be used for such converters. This converter's main objective is to improve the voltage gain, the easiest way

is to cascade the boost converter. Although, the switching voltage stress has been an increase. The transformerless high voltage converters were also introduced

In [15], the converter has low voltage stress. The losses and high efficiency can thus be lowered. Transformerless cell-based converters were also displayed in [16], the converter has certain benefits, including greater voltage gain voltage gain, lower power diode's, and switches stresses, minimal ripples, and greater efficiency. The alternating transformer conversion method has been described in [17],Clamps, both active and passive are frequently utilised in those other converter topologies to lessen the burden on the switch voltage. Additional active clamping and passive clamping circuit designs were also conversely embraced to decrease the spike voltages around the active switches. A Zeta dc to dc converter of the active clamp has been displayed in [18] for zero voltage switching (ZVS). To minimize the transition, the flyback and Zeta converters in the presented converter use the same active switches in conveys. [19] Proposes a transformerless buck-boost converter, the converter's voltage gain is three times that of a traditional buck boost converter. A buck-boost converter, incorporating KY as well as a buck converter, was introduced in [20] transformerless, to lower the power switches number to two. However, all buck-boost converters achieve a high voltage gain of two. Besides, High step converter are constructed using KY converter. The biggest limitation of the KY converter is that there have been sudden charges of some condensers in some working modes. As a consequence, current stresses have also worsened on diodes, switches, and condensers. There are some problems with implementing this major issue. In [21], this same output voltage ripple decrease has been achieved by using two Zeta DC/DC converters. A high-step converter was indeed addressed at [22] with the connected inductor. Such a converter has one primary switch as well as the stress has been lowered through the main switch. However, the voltage stress of the converter's three diodes would be high. The leakage power could be reused in this converter.

A high-step converter was also described in [23], These same comprehensive study boost converters, as well as the voltage-double module, have been used for one such converter as well as the conversion has two main switches. High DC-DC converters are provided in [24], the version was released. Two main switches and highly stressful diodes and switching are used for this converter. The buck-boost converters were indeed described in [25],[26] transformerless. Three switches are located on this converter. The switch's voltage stress is equal to the converter's output voltage in this converter. The switching and conduction losses of the converter are extremely significant. A DC-DC converter was incorporated in [27] with a transformer-less buck-boost converter. There is a higher voltage gain from this converter than from the buck-boost, cuk, spice, and zeta converters, and only one active switch is used. The converter has three inducers and displays a pulse current of the input or output. The switch and converter diode are stressful. The converter's losses are thus high.

In [28]-[30] a non-coupled DC-DC inductor was introduced using two switches. In [28]-[29], there was a passive switched capacitor and an active DC-DC inductor. A SEPIC transformer with a continuous input current was also addressed in [30], which is a transformer-less high-stage. Compared with construction, such converters benefit from the decreased number of objects and low-voltage pressure throughout the switches. Even so, the control complexity is increased by using two switches in the configuration.

It is suggested in this paper that an unique transformerless buck -- boost converter be developed on the basis of the Zeta converter. The gain of the voltage converter is greater than that of the traditional buck--boost converter, as well as that of the Zeta, Cuk, and Sepic converters. The suggested converter topology is easy, and as a result, the converter function control also easy. There is only one primary switch on this converter. Due to the fact that the primary switches and diodes stress levels are lower than the output's voltage, the switching loss will be minimal, and increased efficiency also this converter. Buck–boost converters are utilised in a variety of applications, including led drivers, fuel cells, and electronic components in automobiles. An explanation analysis of the modes is provided, and experimental data are presented to verify that the converter is operating properly.

This paper is discussed as In Section 2, we detailed the presented converter buck and boost functions, the operation modes of Mode I, Mode II, and Mode III, the steady-state condition of the CCM and DCM modes, voltage gain, inductor voltage and current values, BCM, efficiency, voltage stress, and calculated inductors and capacitors values. In Section 3, we detailed the design of the FLC controller and membership functions. In Section 4, we discussed the proposed converter Experimental and simulation results of both boost and buck modes, and these converter results, such as efficiency and voltage gain, compared with another converter. The conventional PI

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controller is compared with this proposed converter. In section 5, describes the details of the presented converter and the conclusion remarks of the article.

## 2 The Proposed Converter

The topology of the converter's circuit is depicted in Figure 2 (topology). The converter is made up of a single primary (S) switch, also includes two ($D_1$, $D_2$) diodes, three ($L_1$, $L_2$, $L_3$) inductors, Four ($C_1$,$C_2$,$C_3$,$C_o$) capacitors, and a single (R)load.
The following criteria were taken into consideration in order to simplify the analysis of the new buck–boost converter.

a. As a result, the voltages of the capacitors may be considered constant since all capacitors are of sufficient size.
b. Semiconductor components, such as diodes and switches, are the best choice for this.

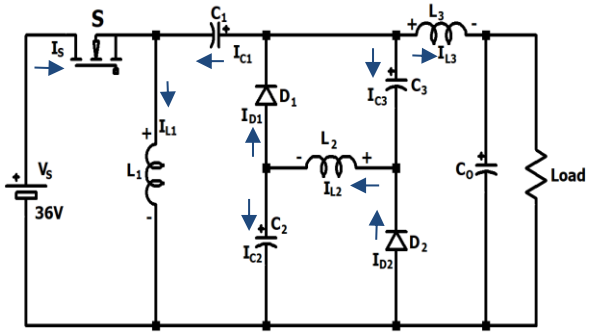
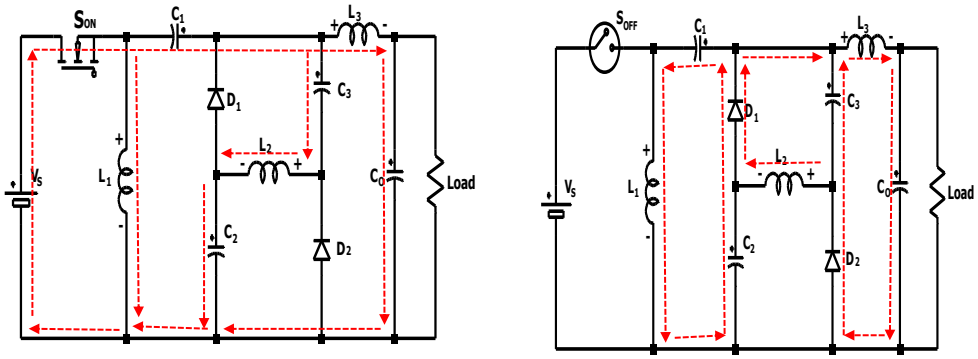



**Figure 2**. Circuit diagram of the presented converter

The suggested converter's works in both continuous and discontinuous conduction modes. The CCM has two modes. Following is a detailed examination of the CCM converter.




(i) (ii)

**Figure 3.** The presented converter modes (i) Mode 1 (ii) Mode 2

### 2.1 Mode of Continuous Conduction (CCM)

Mode 1 [$t_o$, $t_1$] The primary (S) Switch is ON and the diodes $D_1$ and $D_2$ are OFF throughout this time period. Figure 3(i), show the current flow direction. A magnetised inductor is $L_1$ followed by $L_2$, and $L_3$. capacitor $C_2$, and $C_3$ are charged while $C_1$ is discharge. As a result, the appropriate formulas are as follows:

$$V_{L1} = V_i \tag{1}$$

$$V_{L2} = V_i + V_{C1} - V_{C2} - V_{C3} \tag{2}$$

$$V_{L3} = V_{C1} + V_i - V_o \tag{3}$$

Mode 2 [$t_1$, $t_2$] as illustrated in Figure 3 (ii), the current flow direction is presented. Switch S is switched OFF throughout this period. The D1, and D2 diodes are switched on. The L1, L2, and L3 inductors are demagnetized. The inductor L1 charges the capacitor C1. The C2, & C3 capacitors discharge. Inductor voltages are derived as follows:

$$V_{L1} = V_{C2} - V_{C1} \tag{4}$$

$$V_{L2} = -V_{C2} = -V_{C3} \tag{5}$$

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$$V_{L3} = V_{C3} - V_o \tag{6}$$

2.2 The Presented Converter's Steady State Analysis

2.2.1 Gain in Voltage

In the case of $L_1$ and $L_2$, we can use the volt-sec balancing concept and use the equations (1), (2), (4), and (5), we obtain

$$\frac{1}{T_s}\left(\int_0^{DT_s} V_i dt + \int_{DT_s}^{T_s} (V_{C2} - V_{C1})dt\right) = 0 \tag{7}$$

$$\frac{1}{T_s}\left(\int_0^{DT_s} (V_i + V_{C1} - V_{C2} - V_{C3})dt + \int_{DT_s}^{T_s} (-V_{C2})dt\right) = 0 \tag{8}$$

The voltage of $C_1$, $C_2$, & $C_3$ ($V_{C1}$, $V_{C2}$, & $V_{C3}$) may be obtained by using (5), (7) and (8) as follows:

$$V_{C1} = \frac{2DV_i}{1-D} \tag{9}$$

$$V_{C2} = V_{C3} = \frac{DV_i}{1-D} \tag{10}$$

Using volt seconds balance $L_3$ and (9) &(10), get the voltages transfer gain ($M_{CCM}$):

$$\frac{1}{T_s} = \left(\int_0^{DT_s} (V_{C1} + V_i - V_o)dt \int_{DT_s}^{T_s} (V_{C3} - V_o)dt\right) = 0 \tag{11}$$

$$M_{CCM} = \frac{V_o}{V_i} = \frac{2D}{1-D} \tag{12}$$

As shown in (12), the suggested converter's voltages gain is double that of the Zeta converter. As a result, the converter's voltage gain is greater than the Zeta converter's. Figure 4, illustrates some of the suggested converter's main waveforms in CCM.

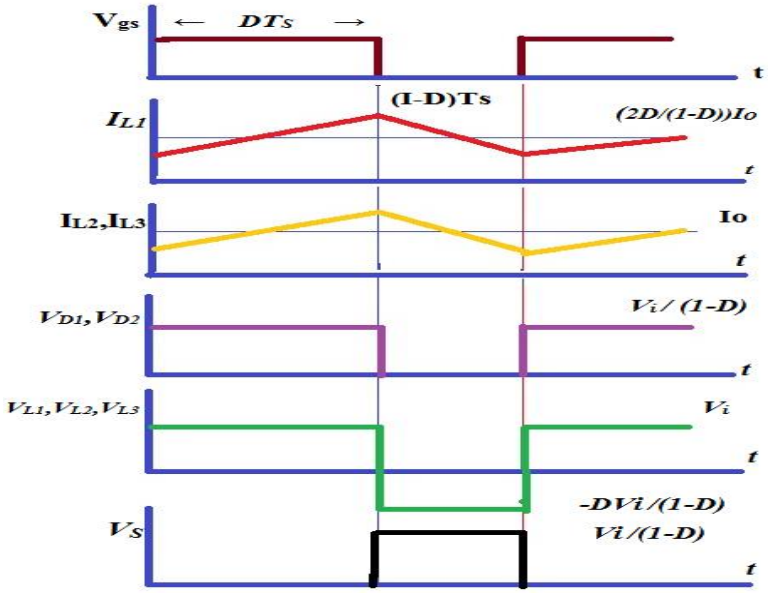


**Figure 4.** The presented converter's illustrated waveforms in the CCM

As illustrated in Figure 5, suggested converter, Zeta & traditional buck- boost converter's shows the gain of the voltage. As can be observed, the suggested converter's has a greater voltages transfer gain than the other converter.

2.2.2 Current Calculation

The average currents of the inductor $I_{L2}$, $I_{L3}$ of respective inductors $L_2$ and $L_3$ and the average currents move to the across capacitors $C_2$, C3 ($I_{C2,on}$, $I_{C3,\,on}$ ) during the switch ON period time in mode 1, the following expressions are obtained,

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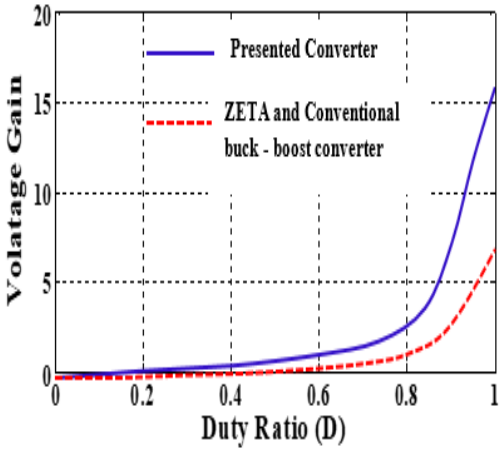


**Figure 5.** In CCM, the presented and conventional converter gain of the voltage curves

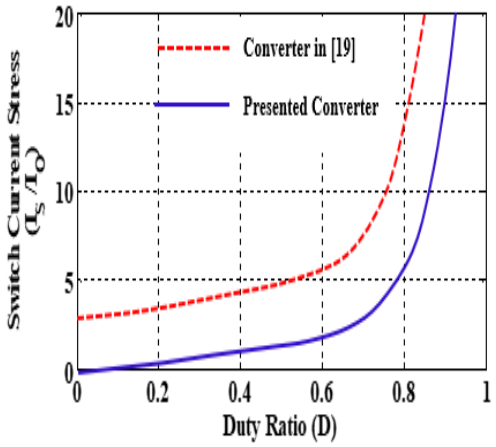


**Figure 6**. Duty Ratio Vs Switching Current Stress of the converter's

$$I_{L3} = \frac{(2D)V_i}{R(1-D)} \tag{13}$$

$$I_{C1,on} = -\left(I_{L2} + \frac{(2D)V_i}{R(1-D)}\right) \tag{14}$$

$$I_{C2,on} = I_{C3,on} = I_{L2} \tag{15}$$

Then, the mean current $I_{C1,off}$ of capacitor $C_1$ in mode 2, the following expressions are obtained,

$$I_{C1,off} = (I_{L2} - I_{C2,off} - I_{C3,off} - I_{L3}) \tag{16}$$

Here, $I_{C2,\,off}$ is the mean current of $C_2$ and $I_{C3,}$ off is the mean current of $C_3$ in mode 2 on the principle of ampere sec balance on $C_1$, $C_2$, $C_3$ the expression framed is,

$$\frac{1}{T_s}\left(\int_0^{DT_s} I_{C1,2,3,on}\, dt + \int_{DT_s}^{T_s} I_{C1,2,3,off}\, dt\right) = 0 \tag{17}$$

By applying the expressions (13),(14),(15),(16) in expression (17), the mean current $I_{C2}$, on, $I_{C3}$, on of capacitors $C_2$, $C_3$, and the current $I_{L2}$ of the inductor $L_2$ are framed as below,

$$I_{L2} = I_{C2,on} = I_{C3,on} = \frac{(2D)V_i}{R(1-D)} \tag{18}$$

Concerning the above-said expression (18), the mean current $I_{C1}$, on of the corresponding capacitor $C_1$ is framed as below,

$$I_{C1,on} = \frac{(-4D)V_i}{R(1-D)} \tag{19}$$

About the expression (19) and Figure 3 (ii), $I_{L1}$, which is the mean current of the inductor $L_1$, is framed as,

$$I_{L1} = I_{C1,off} = \frac{(4D^2)V_i}{R(1-D)^2} \tag{20}$$

Regarding Figure 3 (i), (ii) IS which is the stress of the current across the switch (S), and $I_{D1}$, $I_{D2}$ that is the current stress across $D_1$, $D_2$ diodes are framed as below,

$$I_s = I_{L1} - I_{C1,on} = \frac{(4D)V_i}{R(1-D)^2} \tag{21}$$

$$I_{D1} = I_{L2} - I_{C2,off} = \frac{V_i(2D)}{R(1-D)^2} \tag{22}$$

$$I_{D2} = I_{L2} - I_{C3,off} = \frac{V_i(2D)}{R(1-D)^2} \tag{23}$$

Figure 6, depicts the presented converter's, and [19] converter's switch current stress curves. As shown, the suggested converter's current stress is less than that of the converter in [19], implying that the given converter's conduction loss will be minimal.

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2.3 Mode of Discontinue Conduction (DCM)

In DCM consists of three modes.. DCM's mode 1 is identical to CCM's Mode 1. In Mode 2, the diodes' currents decrease. In Mode 3, the diode current decreases to zero. The diodes are switched off in these mode. The circuit equivalent is illustrated in Figure 7. The voltage across inductor $L_1$, $L_2$, & $L_3$ is zero in this condition.

About Figure 3(ii), the summation of the mean of the diode currents can be achieved with the following expression.

$$I_{D1} + I_{D2} = I_{L1} + I_{L2} + I_{L3} \tag{24}$$

The mean diode currents represented as ($I_{D1,av}$, $I_{D2,av}$) of $D_1$,$D_2$ can be found by

$$I_{D1,av} = I_{D2,av} = \frac{V_o}{R} \tag{25}$$

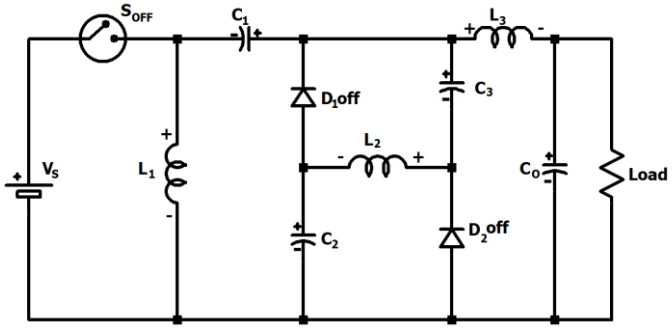


**Figure 7.** The presented converter, mode 3 circuit in DCM

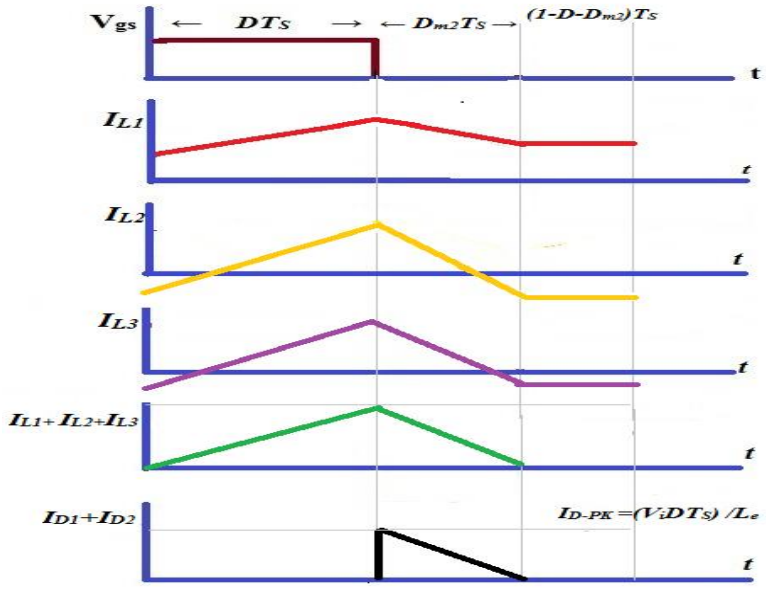


**Figure 8.** The presented converter's illustrated waveforms in the DCM

The total of the average diode D1 and D2 during one switching time may be calculated as follows, according to Figure 8:

$$I_{D1,av} + I_{D2,av} = \frac{1}{2} \times D_{m2} \times I_{D-PK} \tag{26}$$

The duty cycle is represented as $D_{m2}$ in Mode 2 in DCM. The summation of $L_1$, $L_2$, $L_3$ gives the peak value represented as.$I_{D\text{-}PK}$

$$I_{D-pk} = I_{L1-Pk} + I_{L2-pk} = \frac{V_i D T_s}{L_e} \tag{27}$$

Where,

$$\frac{1}{L_e} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} \tag{28}$$

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By applying an inductor volt-sec balancing $L_1$, $L_2$, & $L_3$ duty ratio to Mode 2 in DCM ($(D_{m2})$, the following expressions are obtained:

$$D_{m2} = \frac{2DV_i}{V_o} \tag{29}$$

The voltage gain ($M_{DCM}$) in discontinuous mode can be obtained using (24)-(29) and does $M_{DCM}$ is provided as

$$M_{DCM} = \frac{D}{\sqrt{\tau_L}} \tag{30}$$

*($\tau_L$)*, Which is the time constant for the normalized inductor is obtained as

$$\tau_L = \frac{2L_e}{RT_s} \tag{31}$$

*2.4 Analysis of Boundary Condition Mode (BCM)*

The gain of the voltage in CCM, and DCM becomes uniform during the working of the presented converter's in BCM. The time constant *($\tau_L$)* can be obtained using the equations (12) and (30) and it is represented as

$$\tau_b = \frac{(1-D)^2}{4} \tag{32}$$

*($\tau_L$)*, which is the time constant curve for the boundary normalized inductor indicated in Figure 9. The presented converter's operate in continuous conduction mode when $\tau_b$ is less compared to $\tau_L$. Figure 10, illustrates the proposed and ZETA converters' boundary normalised inductor time constant curves.

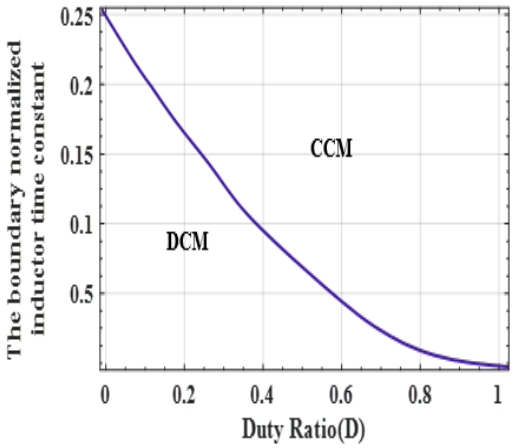


**Figure 9.** The presented converter duty cycle vs boundary constant inductor time

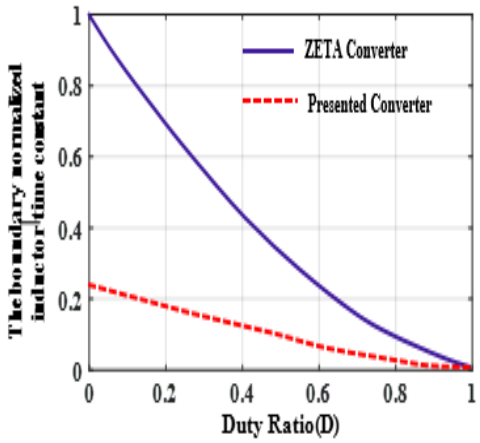


**Figure 10**. The Zeta and the presented converter's time-constant curves are represented

*2.5 Analysis of Efficiency*

The parasitic resistances listed below can be used to evaluate the efficiency of the converter under consideration. $P_{DS}$, $P_{SW}$, $P_{Switch}$, $P_{D1,2}$, $P_{C1,2,3,0}$, $P_{L1,2,3}$, $P_{Loss}$. The capacitor's inductor's voltage ripples are not considered. ($P_{DS}$), which is the switch (S) condition loss is given by,

$$P_{rDS} = r_{DS} I_{S,rms}^{\ 2} = r_{DS} \frac{4D}{(1-D)^2} I_o^{\ 2} \tag{33}$$

($P_{SW}$), which is the switch losses of the presented converter's is given by,

$$P_{Sw} = f_s C_s V_s^{\ 2} = f_s C_s \left( \frac{V_i}{1-D} \right)^2 \tag{34}$$

(PSwitch), which is the switch (S) the total loss is given by,

$$P_{Switch} = P_{rDS} + \frac{P_{Sw}}{2} \tag{35}$$

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($P_{D1,2}$), which is the loss of the diode D1 and diose Diode D2, is provided as

$$P_{D1,2} = R_{F1,2}\frac{1}{1-D}I_o^{\,2} + V_{F1,2}I_o \tag{36}$$

($P_{C1,2,3,0,}$),the capacitor loss of $C_1$,$C_2$, $C_3$,$C_o$ are obtained by,

$$P_{C1,2,3,o} = r_{C1}\frac{4DP_o}{(1-D)R} + r_{C2,3}\frac{DP_o}{(1-D)R} + r_{Co}\frac{(1-D)^2 RP_o}{48L_3^{\,2} f_s^{\,2}} \tag{37}$$

($P_{L1,2,3}$),the inductor loss of ($L_1$, $L_2$, $L_3$)are presented as,

$$P_{L1,2,3} = R_{L1}\left(\frac{2D}{1-D}\right)^2\frac{P_o}{R} + R_{L2,3}\frac{P_o}{R} \tag{38}$$

The presented converter's total loss ($P_{Loss}$) is obtained as,

$$P_{Loss} = P_{Switch} + \sum_{u=1}^{2}(P_{RF})_{Du} + \sum_{u=1}^{2}(P_{VF})_{Du} + \sum_{u=1}^{3}P_{RCu} + P_{RCo} + P_{rL1} + P_{rL2} + P_{rL3} \tag{39}$$

$\eta$ , which is the proposed converter of efficiency given by

$$\eta = \frac{P_O}{P_O + P_{Loss}} = \frac{1}{1+\frac{P_{Loss}}{P_O}} \tag{40}$$

$$\eta = \frac{1}{1+\frac{A_1}{R(1-D)^2} + r_{Co}\frac{(1-D)^2 R}{48Lf_2^{\,2}} + \frac{f_s C_s V_i^{\,2}}{2(1-D)^2 RI_o^{\,2}}} \tag{41}$$

Where,

$$A_1 = 4Dr_{DS} + (1-D)(R_{F1}+R_{F2}) + \frac{(1-D)^2}{I_o}(V_{F1}+V_{F2}) + 4D(1-D)r_{C1} + D(1-D)(r_{C2}+r_{C3}) + 4D^2R_{L1} + (1-D)^2(R_{L2}+R_{L3}) \tag{42}$$

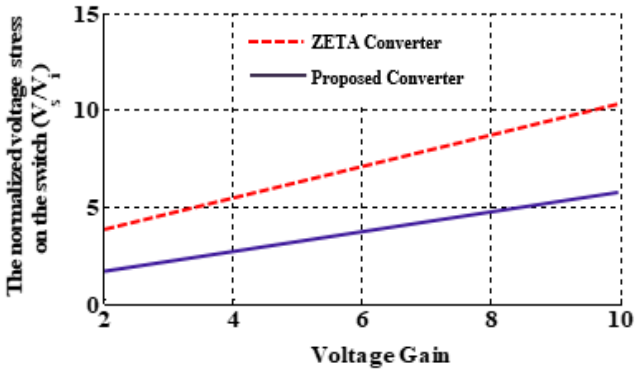


**Figure 11**. Modeled normalised switch voltage stress versus voltage gain

*2.6 Analysis of Voltage Stress*

The most important criterion in the circuit is the stress of the voltage. Here the switch (S) and diodes, the stress of the voltage is calculated as given below,

$$V_s = \frac{V_i}{1-D} \tag{43}$$

$$V_{D1} = V_{D2} = \frac{V_i}{1-D} \tag{44}$$

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According to (43) & (44), the diodes' and switch's voltage stresses are well below the output voltage. The suggested converter's normalised voltage stress is compared to the ZETA converter in Figure 11. Because the ZETA converter's normalised voltage stress is greater than that of the presented converter, it is possible to choose a switch with a low conduction loss.

*2.7 Capacitors across the voltage ripple calculation*

A voltage ripple is formed by $C_1$ ($\Delta V_{C1}$ , $\Delta V_{C1,ESR}$) from the current that is in equivalent series resistance (ESR) which is shown in Figure 12. Another voltage ripple ($\Delta V_{C1,cap}$) is formed by $C_1$ due to the discharging and charging mode of the capacitor. The capacitors $C_2$, $C_3$ of voltage &current waveform are shows in Figure 13.

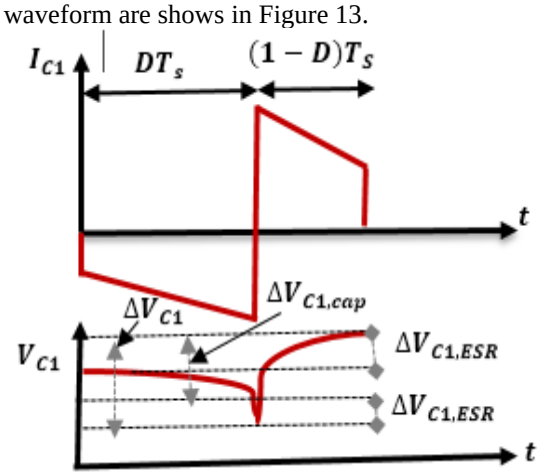


**Figure 12.** The capacitor C1 of voltage and current waveform

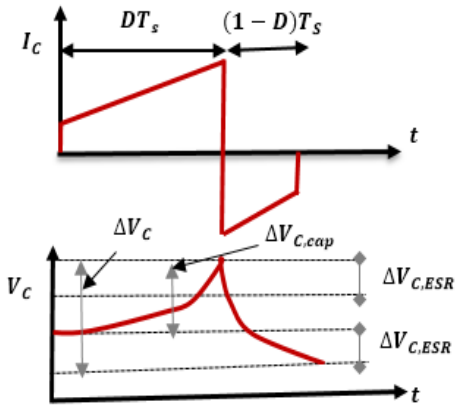


**Figure 13.** The capacitors C2, C3 of voltage and current

Thus, the capacitor $C_1$ voltage ripple can be framed as given below,

$$\Delta V_{C1} = \Delta V_{C1,ESR} + \Delta V_{C1,cap} \tag{45}$$

$\Delta V_{C1,ESR}$ is given by,

$$\Delta V_{C1,ESR} = ESR_{C1}\Delta I_{C1} \simeq ESR_{C1}(I_{C1,on} - I_{C1,off}) = \frac{ESR_{C1}(4D)V_i}{(1-D)^2 R} \tag{46}$$

Where,

$$ESR_{C1} = \frac{\tan \delta_{C1}}{2\pi f_s} \tag{47}$$

Capacitor $C_1$'s dissipation factor $\tan \delta_{C1}$

$\Delta V_{C1,cap}$ given by,

$$\Delta V_{C1,cap} = \frac{I_{C1,on}DT_s}{C_1} = \frac{2DT_sV_o}{RC_1} \tag{48}$$

likewise, $\left(\Delta V_{C2,3}\right)$ which is a capacitor $C_2$ and $C_3$ voltage ripple is given by,

$$\Delta V_{C2,3} = \Delta V_{C2,3,ESR} + \Delta V_{C2,3,cap} = \frac{ESR_{C2,3}(2D)V_i}{(1-D)^2 R} + \frac{DT_sV_o}{RC_{2,3}} \tag{49}$$

*2.8 Inductors and Capacitors Design*

In CCM, the theoretical $L_1$, $L_2$, $L_3$ inductors derived values as follows,

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$$L_1 \geq \frac{V_o(1-D)^2}{8DI_o f_s} = \frac{90(1-0.53)^2}{8\times 0.53\times 2.8\times 40\times 10^3} = 42\mu F \quad (50)$$

$$L_{2,3} \geq \frac{V_o(1-D)}{4I_o f_s} = \frac{90(1-0.53)}{4\times 2.8\times 40\times 10^3} = 94\mu F \quad (51)$$

In CCM, the theoretical $C_1$, $C_2$, $C_3$, $C_o$ capacitors derived values as follows,

$$C_1 \geq \frac{2DT_s V_o}{R\Delta V_{C1}} = \frac{2DV_o}{R\times 0.01\times V_o \times f_s} = \frac{2\times 0.53\times 90}{32\times 0.01\times 90\times 40\times 10^3} = 83\mu F \quad (52)$$

$$C_{2,3} \geq \frac{DT_s V_o}{R\Delta V_{C2,3}} = \frac{DV_o}{R\times 0.01\times V_o \times f_s} = \frac{0.53\times 90}{32\times 0.01\times 90\times 40\times 10^3} = 41\mu F \quad (53)$$

$$C_o \geq \frac{V_o(1-D)}{16L_3 f_s{}^2 \Delta V C_o} = \frac{100(1-0.53)}{16\times 0.001\times (40\times 10^3)^2\times 1} = 1.8\mu F \quad (54)$$

## 3 The Fuzzy Logic Controller algorithm (FLC)

FLC is a technique that is utilised in nonlinear systems. It derives the ideas of various experts and uses mathematical principles to resolve various complex issues with much simpler calculations. FLC completely depends upon linguistic control variables. FLC is similar to human thinking and thus it reduces the gap between mathematical calculation and human thinking. FLC has three steps. The first step is fuzzification, followed by fuzzy inference and finally by defuzzification.

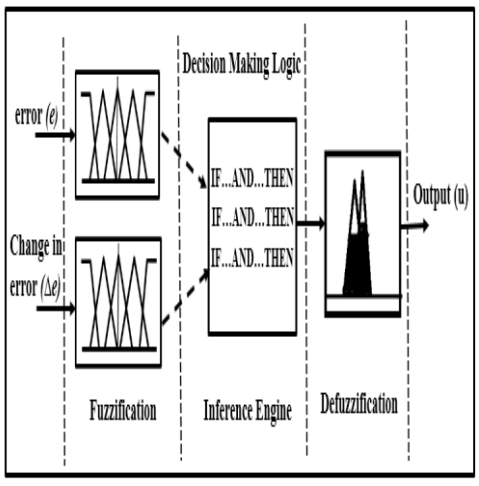


**Figure 14.** FLC controller simplified diagram.

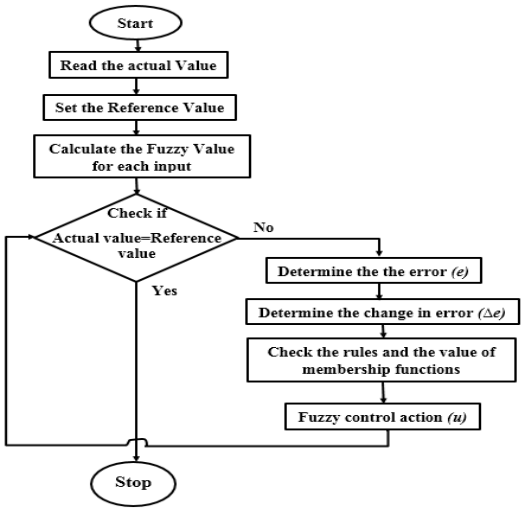


**Figure 15**. FLC controller Flow chart

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In the case of the PI controller, there are no orderly schematic procedures for the design of an FLC. However, the common schematic diagram of the FLC is shows in Figure 14.
By comparing the actual values with their reference values at every interval, the change in error (Δe) and error (e) are obtained for all loops which are provided as input for FLC to achieve the control output (u) [31]. For each regulator, the obtained output (u) acts as the control action which is generated by the FLC. Every loop undergoes the above-mentioned three stages of the FLC and the respective flowchart is shown in Figure 15. For the algorithm, the rule table depending upon the system variables is provided. By altering the duty cycle, the voltage of the output of a transformer-less high-efficiency DC to DC converter's is controlled. When compared with output voltage values with reference voltage values this time obtained by the error value. Here, the voltage of reference is given as r(k) and the obtained voltage of the output is given as y(k). From the following equation (55), the error voltage can be calculated.

$$e(k) = r(k) - y(k) \tag{55}$$

From the below equation, the change in the error voltage can be calculated

$$\Delta e(k) = e(k) - e(k-1) \tag{56}$$

In the first step, when $e(k)$ is positive ('+') and $\Delta e(k)$ is considered negative '−', the error becomes '+' and it lowers down to zero. To reduce the error, Δu is made positive. The error becomes negative and goes on decreasing when the e (k) is '−' and the $\Delta e(k)$ is made'+'. Δu is applied to stop the error from further decreasing from negative. [32]-[33]

### *3.1 The internal structure of the fuzzy controller*

Here, Mamdani-type fuzzy inference has been applied. The simulation circuit of the entire FLC is given in Figure 16. The two inputs (e, de) and output (du) are provided in the FLC as illustrated in Figure 16(a), Figure 16(b), & Figure 16(c).

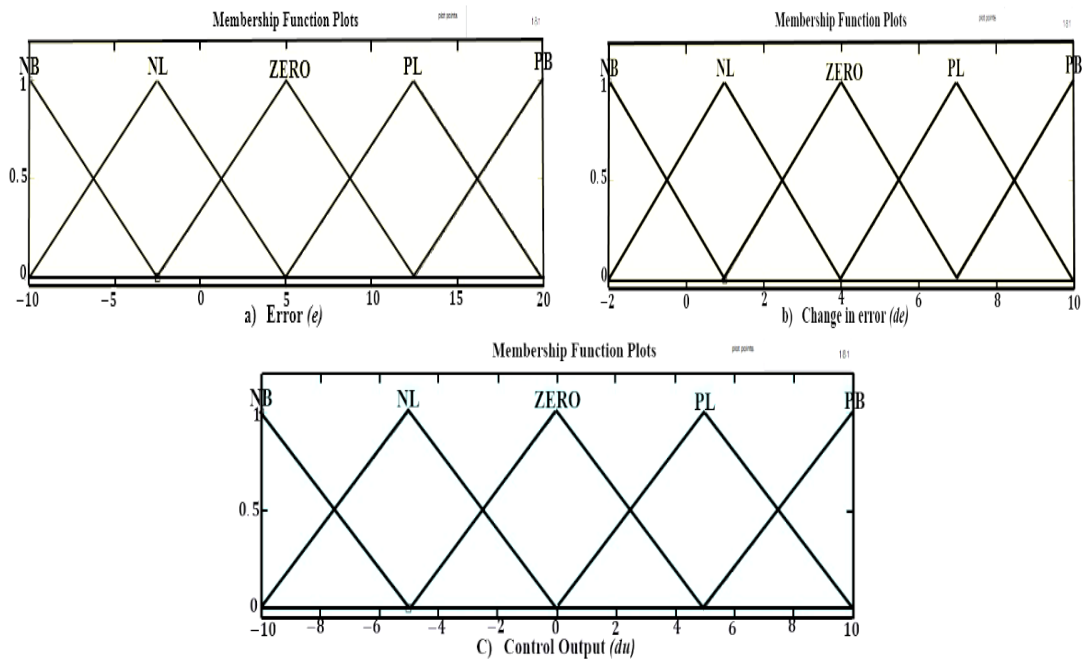


**Figure 16**. Membership functions, (a) e, (b) de, (c) du

Using the five membership function tables, the inputs (e, de) are framed as values of fuzzy. Trapezoidal and triangle methods of membership function are applied here because of their efficiency and simplicity in implementation. Below are the abbreviations of the membership functions explained.

1. NB◄► Negative Big
2. NL◄► Negative Low
3. Z ◄► Zero
4. PL◄► Positive Low
5 PB◄► Positive Big

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For the provided inputs, the membership functions that are designed are illustrated in Figure 16(a), & Figure 16(b) as PWM oscillations are suppressed by the trapezoidal function Z, it is used here and the output is shown in Figure 16 (c)

| (de)/(e) | NB | NL | Z | PL | PB |
|---|---|---|---|---|---|
| NB | NB | NB | NL | NL | Z |
| NL | NB | NL | NL | Z | PL |
| Z | NL | NL | Z | PL | PL |
| PL | NL | Z | PL | PL | PB |
| PB | Z | PL | PL | PB | PB |

**Table I.** Rule Board for Change in Error and Error

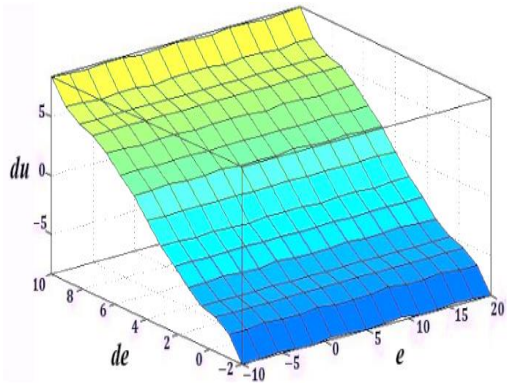


**Figure 17**. Control Surface of the FLC

Upon experience, the rules are framed for the fuzzy system. The rules are represented in symmetric matrix skew form in Table I. It has twenty-five rules derived from twenty-five input combinations

Some of the fuzzy rules are explained below,

When de and e are PB, then du is PB,
When de is PL and e is PB, then du is PB,
When de is NB and e is PB, then du is Z.
When de is NB and e is PL, then du is NL
When de is NB and e is Z, then du is NL.

One more rule is added to improve the transient response. The rule is given below

When e is PB, then du is PB

The proposed FLC-based converter error (u), change in error (de) Based on various combinations of inputs, the graphical output (du) is shows in Figure 17.

### *4 Simulation and Experimental Results*

The gate pulses to the active power switch S are generated by a PWM generator using Matlab/ Simulink 19 with a switching 40 kHz frequency of as shows in Figure 18. The simulation results show that the oscillation in the steady-state at the highest power point is minimal resulting in less energy loss and higher system efficiency, This section discussed the evaluation and performance of the FLC controller-based transformerless high-efficiency dc to dc converter. The Proposed converter results of the simulation's are given in both step up(boost) and step down(buck) modes, and a comparison between the PI,ANN controllers and the proposed FLC-based controllers is shown in the following sections.. Table II list the components utilised in the proposed converter.

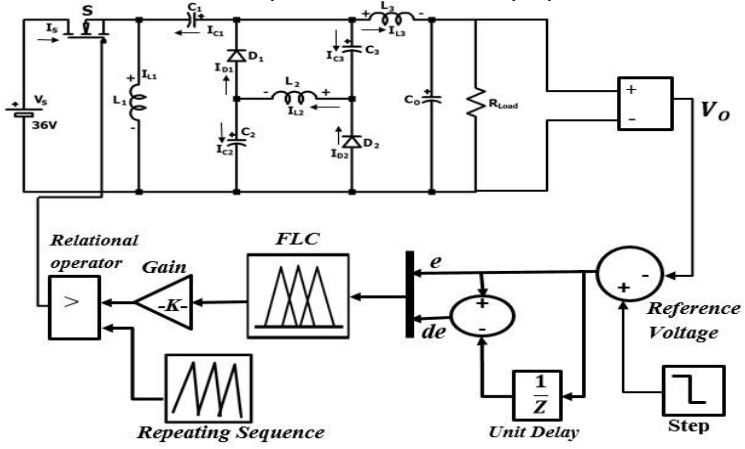


**Figure 18**. Simulation Circuit of FLC based proposed Converter with resistive Load

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*4.1 The Output of the Boost Mode*

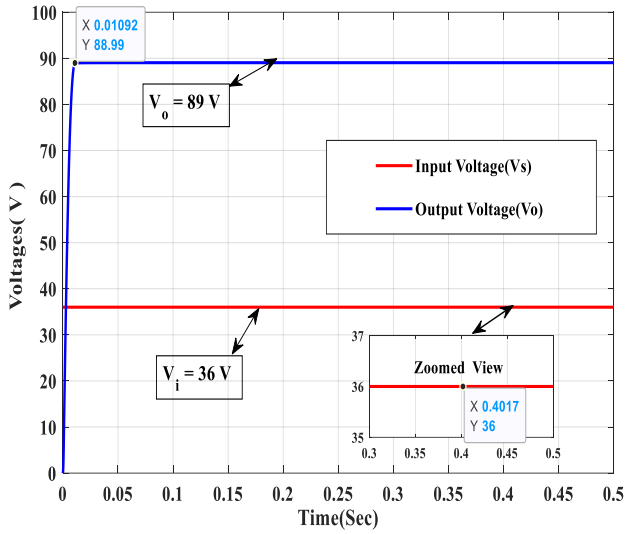
Figure 19 and 20 illustrate the waveforms of the voltages at the input and output, as well as of the input & output power, as well as of the input & output current, inductor currents, capacitor voltages, diode voltages, current and power switch voltages, in this case, the boost mode when triggering the switch at 40 kHz frequency with an input 36V voltage, the outputs voltage is obtained as 89V, as it is shows in Figure 19(i). The output current of 2.8A with the output power of 248 watts is shows in Figure 19(ii), and the input current of 7.06 A with the input power of 254.4 Watts is shown in Figure 19 (iii).

The switch is in ON time in the CCM mode, the energy is stored in the inductors $L_1$, $L_2$, $L_3$ by the input source, and while the switch is in the OFF position, the inductors discharge it. The inductor currents produced are 6.3A, 2.4A, 2.4A for inductors $I_{L1}$, $I_{L2}$, and $I_{L3}$ respectively, are shows in Figure 19 (i). The correspond inductor waveforms of period time of 0 to 0.5 sec and this inductor current from the zoomed viewpoint period time 0.3 sec to 0.3008 sec also shown in Figure 20(i).

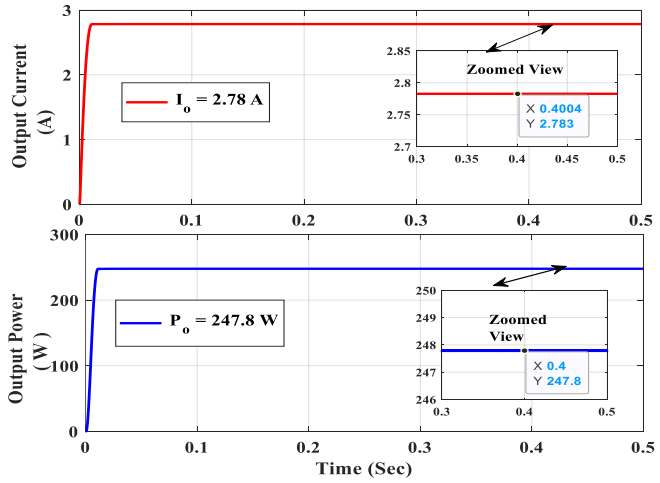
The voltage & current waveform of diodes $D_1$ and $D_2$ are similar and these respective diode voltages $V_{d1}$, $V_{d2}$ are 78V and diode currents $I_{d1}$, $I_{d2}$ is 6.5 A are shown in Figure 20 (ii), and this diode voltage & current of zoomed viewpoint waveforms also shown in Figure 20(ii). The various waveforms of capacitor $C_1$, $C_o$ & $C_2$, $C_3$ are Similar and these respective capacitors voltages $V_{c1}=V_{co}=90$ V and $V_{c2}=V_{c3}=44$ V are shown in Figure 20(iii). And this capacitor voltage of zoomed viewpoint is also shows in Figure 20(iii).The voltages waveforms across the switch voltages $V_S$ are 78V and this zoomed viewpoint is also shows in Figure 20(iv)

**Table II** - Converter system specifications

| System Parameter | Specifications |
|---|---|
| Input voltage $V_i$ | *36V* |
| Switching frequency $f_s$ | *40 kHz* |
| Duty cycle *D* | *53%* |
| Power MOSFET | *IRFP460A* |
| Diodes $D_1$,$D_2$ | *MUR860* |
| Inductors | $L_1$=41$\mu$F, $L_2$= $L_3$=93$\mu$F |
| Capacitors | $C_1$=83$\mu$F, $C_2$=$C_3$=41$\mu$F |
| Capacitor | $C_O$=1.8$\mu$F |
| Resistive load | *32 ohm* |
| Output power(Watts) | $P_o$=248 *W* |
| Output voltage (Volt) | Boost Mode $V_o$=89 *V*& Buck Mode $V_o$=17*V* |
| PI controller values | *23.171*, $K_i$=10 |




**(i)**

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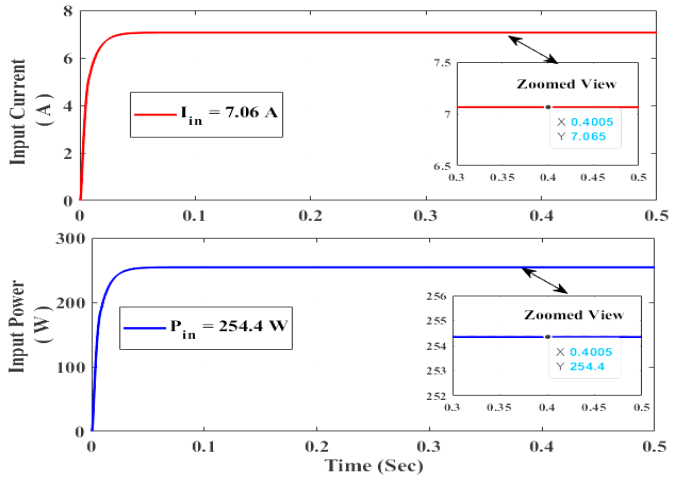


**(iii)**

**Figure. 19.** In Boost mode, (i) The proposed converter output and input voltages, (ii) current and power outputs, (iii) current and power inputs

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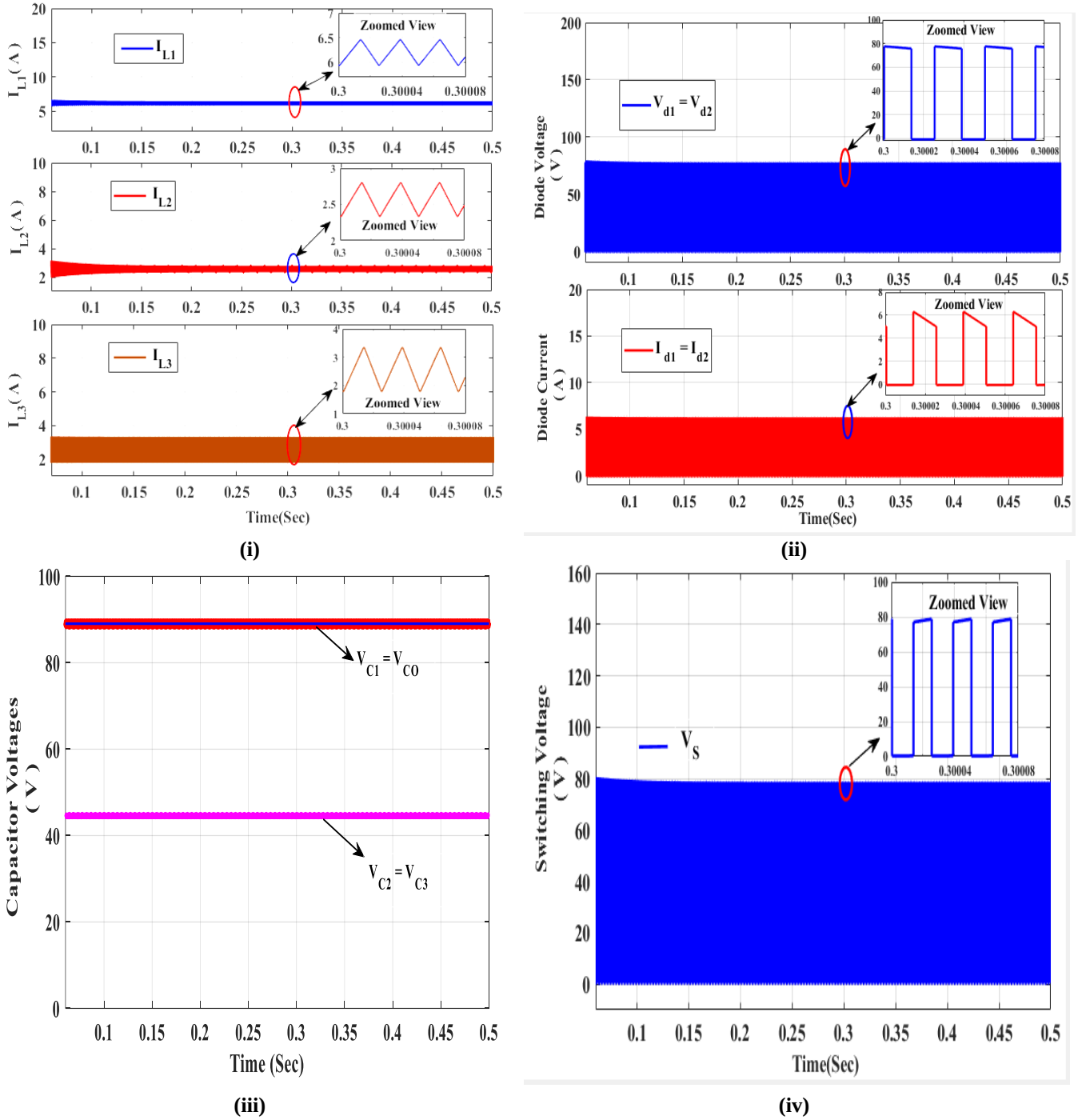


**Figure 20** In Boost mode (i) three inductor currents $I_{L1}$, $I_{L2}$, $I_{L3}$, (ii) two diode voltages $V_{d1}$,$V_{d2}$. and two diode currents $I_{d1}$,$I_{d2}$, (iii) $C_1$=$C_o$ ,$C_2$=$C_3$ capacitors across the voltage, (iv) voltage across the switch

*4.2 Waveforms of Buck Mode*

In the Buck mode, the output current and output voltage obtained are 0.54A and 17.3V, respectively, which is shown in Figure 21 (i). The three inductor currents $I_{L1}$, $I_{L2}$, $I_{L3}$ obtained are 1.3A, 0.6A, 0.6A, respectively, and the respective waveforms are shown in Figure 20 (ii) and this inductor's current zoomed view also is shown in Figure 21 (ii). The two diodes current & voltage waveform of $D_1$ and $D_2$ are similar and their respective voltages $V_{d1}$ and $V_{d2}$ are found to be 17V and currents $I_{d1}$ and $I_{d2}$ are 1.3 A is shown in Figure 21(iii).and these diodes zoomed viewpoint of the waveform is shown in Figure 21 (iii).

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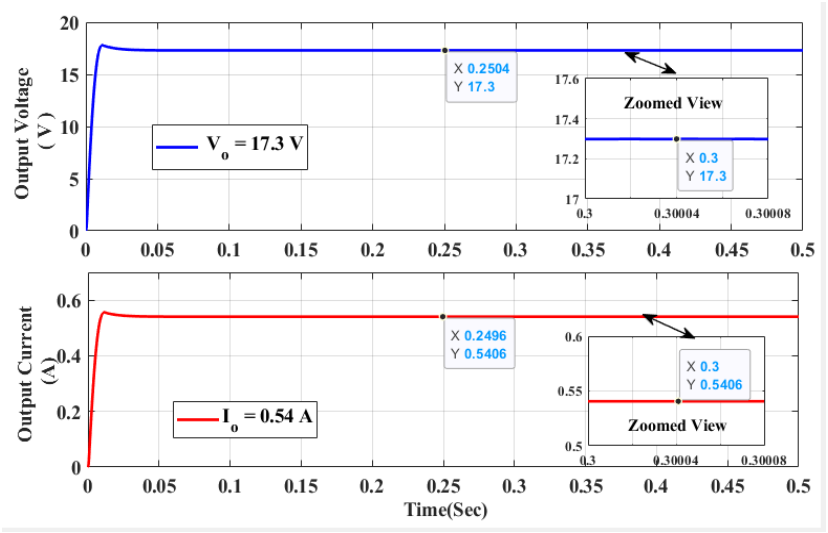
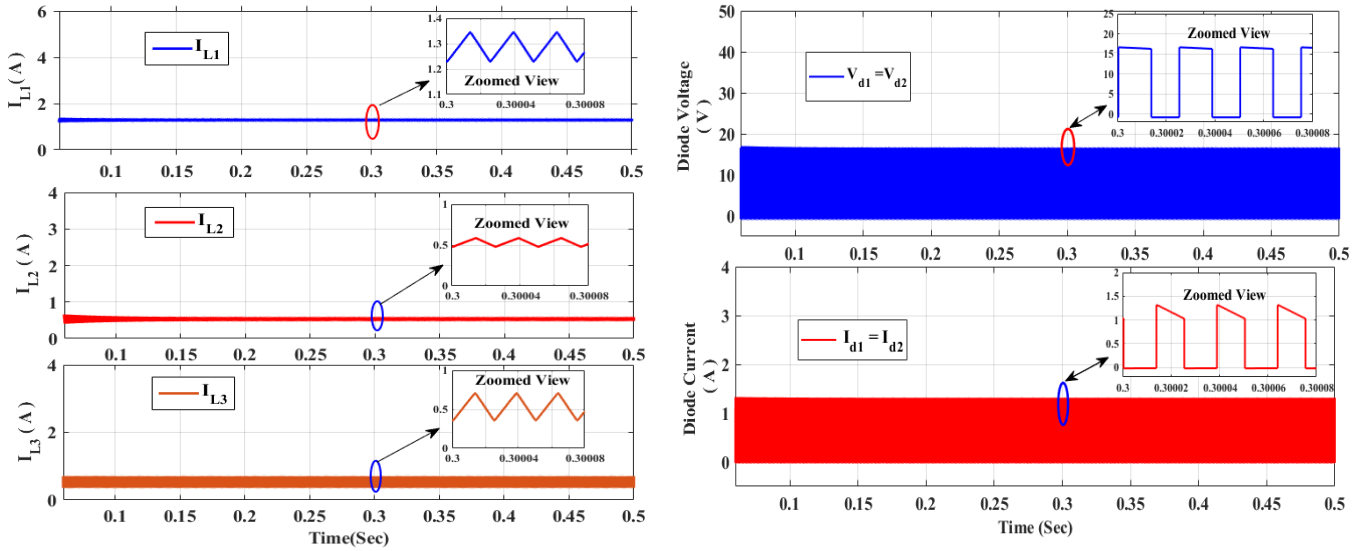



(i)




(ii) (iii)

**Figure 21**. (i) In Buck mode, the proposed converter output voltage and output current, (ii) three inductor currents IL1, IL2, IL3, (iii) two diode voltages Vd1, Vd2. and two diode currents Id1, Id2

*4.3 Comparison of the conventional PI controller, ANN and proposed FLC in CCM mode*

The proposed converter-based FLC controller's performance is compared with the performance of the conventional PI controllers and Artificial Neural Network (ANN), The output voltage waveform is illustrated in Figure 22. The various parameters of time specifications for the output voltage waveform of the proposed FLC controller, ANN controller and PI controllers are compared in Table III.

Table III ,analyzed the overshoot of maximum output voltage, the time settling point of output voltage, the output voltage of steady-state error, and peak value, the above-mentioned parameter values of the suggested FLC controller have better performance when compared with the ANN and PI controller is shown in Table III.

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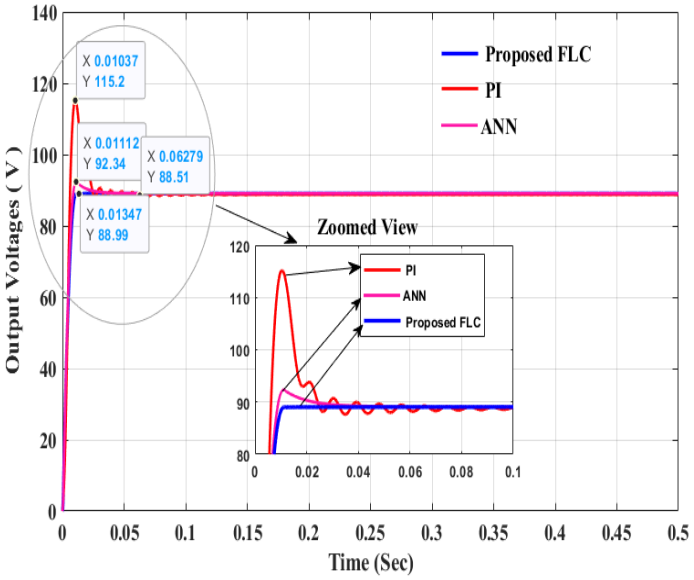


**Figure. 22**. Output voltage waveforms of the Proposed FLC,ANN, PI controller

| Parameter | PI | ANN | FLC |
|---|---|---|---|
| $M_{P,}$ Maximum Overshoot | 23% | 3.6% | 0 |
| $V_{o,}$ Output Voltage | 88.5 V | 88.9 V | 88.99 V |
| $e_{ss,}$ Steady State Error | 0.5 V | 0.1 V | 0.01 V |
| $T_s$ Settling Time | 0.062 S | 0.03 S | 0.01 S |
| $T_{P,}$ Peak Time | 0.01S | 0.01 S | 0 |

**Table III.** Three Controllers Time Domain Parameters

*4.4. Experimental Results*

Experimental data are included to validate the converter's performance. The step up and step down modes of operation are supported by the presented buck--boost converter. The converter's prototype is depicted in Figure 23. The converter shown here has been subjected to CCM performance.

The boost mode of the output voltage is displayed in Figure 24 (i)- (ii). There is an output voltage & output current 89V &2.8 Amps. And a power output of 248 W. Figure 24 (iii) –(v) displays the waveforms of the currents flowing through the inductors $L_1$, $L_2$, & $L_3$, correspondingly. As per (13), (18), & (20), the averaged currents through $L_1$, $L_2$, & $L_3$ inductors are 6.3, 2.4, and 2.4 A, correspondingly. The voltage waveform of diode $D_2$ is identical to that of diode $D_1$. Figure 24 (vi) shows the voltage across diode $D_1$ & $D_2$. The voltage from across diode $D_1$ & $D_2$ is similar to 78 V, as per (44). Figure 24(vi) shows the voltage across the switch S. As per (43),the voltage across the S switch is 78 V. Inductors $L_1$, $L_2$, & $L_3$ have a voltage of 36 V in mode 1 and –40 V in mode 2. The step down mode output voltage is depicted in Figure 25 (i)-(ii). 17 V is the output voltage. 0.5 A output current.

Figure 25(iii)-(v) depicts the waveforms of the $L_1$, $L_2$,& $L_3$ inductors current, respectively. As per (13), (18), & (20), the averaged currents through $L_1$, $L_2$,& $L_3$ inductors are 1.3, 0.6, as well as 0.6 A, correspondingly.

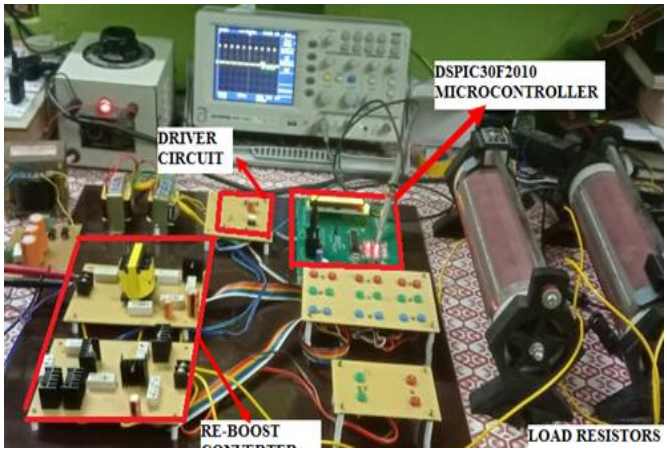


**Figure. 23** Experimental converter setup and prototype

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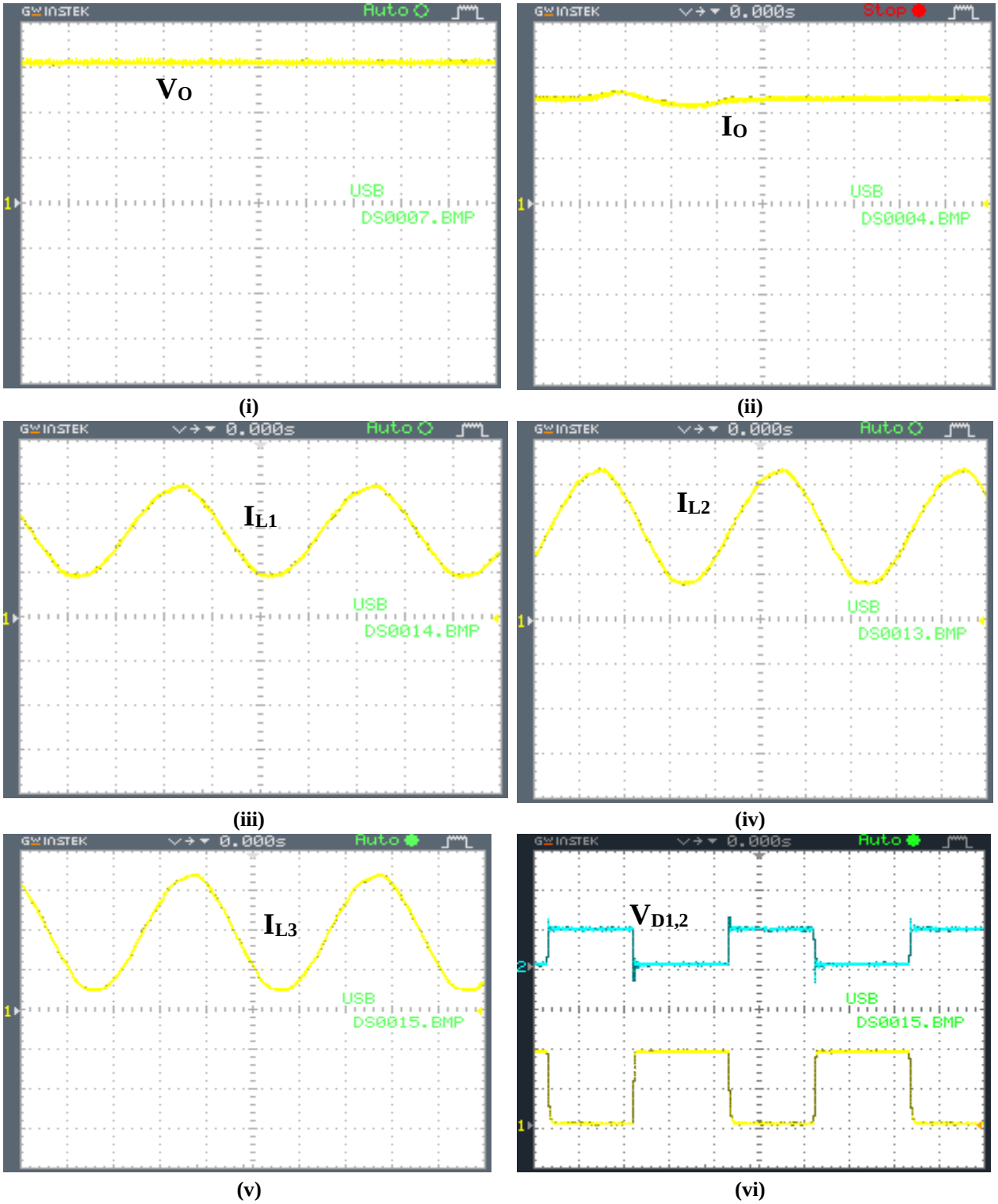


**Figure. 24.** Experiments performed in boost mode in CCM (Time: 50us/div) i) output voltage (20V/div),(ii)output current (1A/div) (iii)inductor L1 current(1A/div) (iv) inductor L2 current(1A/div) (v) inductor $L_3$ current(1A/div) (vi) Diode voltage $D_1$,$D_2$ , voltage across the switch $V_s$(10V/div)

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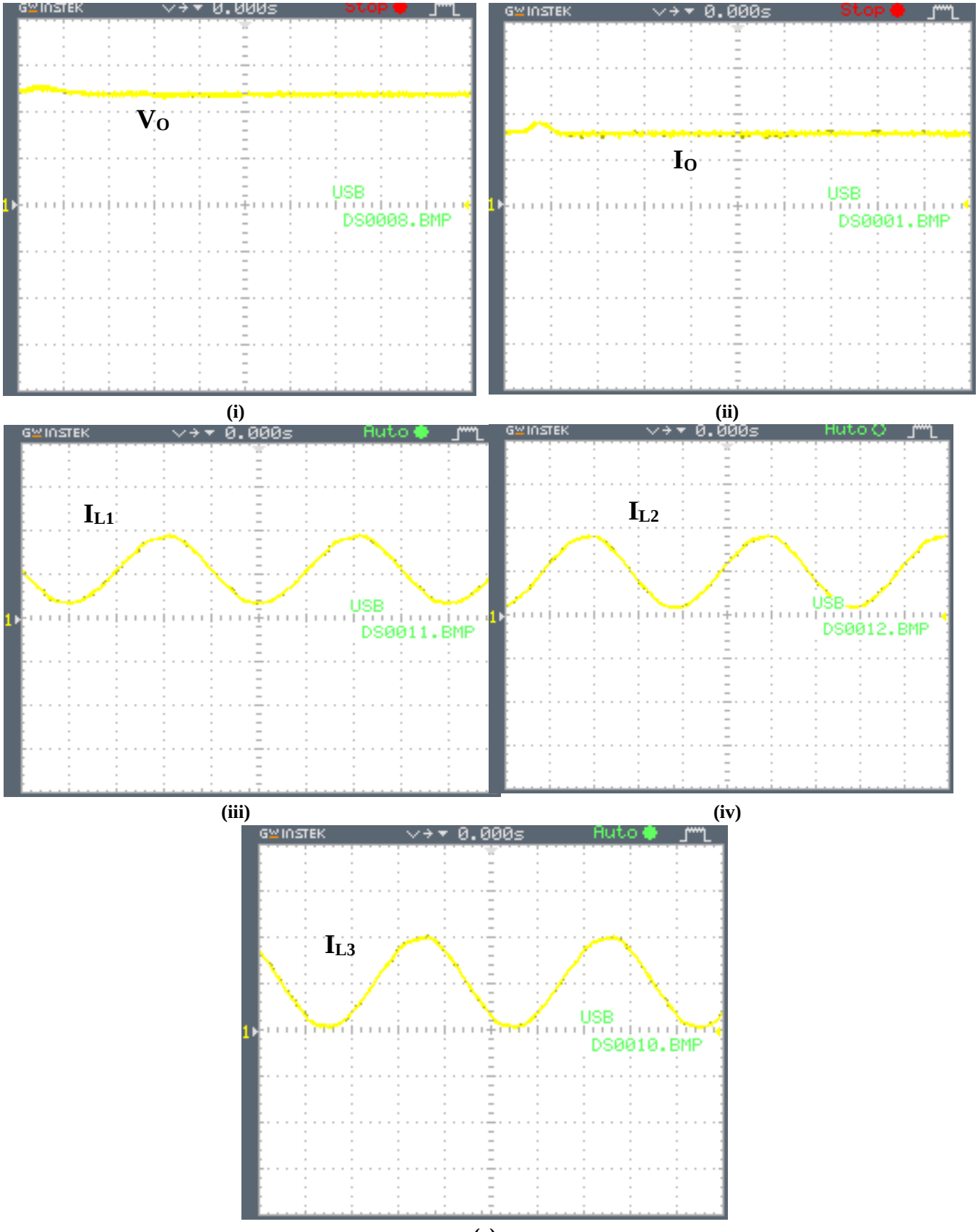


**Figure 25**. Experimental results in Buck mode (Time: 50us/div) .(i) output voltage(5v/div),(ii)output current(500 mA/div) (iii)inductor L1 current(500 mA/div) (iv) inductor L2 current(500 mA/div) (v) inductor L3 current(500 mA/div)

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*4.5 Efficiency Comparison of Presented Converter and other Converter in CCM Mode*

The proposed converter is much efficient with an output power of 248 W shown in Figure 19(ii) and this converter input power 254.4 W has shown in Figure19 (iii), so both (input and output) power are calculated and achieved by the highest efficiency of 97.4 %.It is observed from the efficiency output waveforms that the presented converter has a better dynamic response than the other converters which is clearly shown in Figure 26, It is demonstrated that the presented converter has a significantly greater efficiency when comparing to the Zeta converter's and other converter in [19] and [28]. When operating in boost mode, Figure 27.(i), shows the in step-up mode, efficiency vs output power, and Figure 27 (ii), shows the efficiency vs load currents in boost mode at a duty ratio of 0.53. Figure 27 (iii), plots the efficiency gains from 0.35 to 0.7 with IO =2.7 A vs duty ratio. As illustrated in Figure 10, the efficiency of the step-up mode is greater than the efficiency of the step-down mode, and the experimental maximum efficiency is 97.1 percent.

In Table IV, a comparison of efficiency, voltage gain, and stress of the voltage the count of the total components used are done between the proposed converter and other converters, the presented converter has a greater voltage gain, greater efficiency than the other conventional converters. The presented converter has a simple circuit diagram because this converter using total components is also less when compared to other converters is shows in Table IV

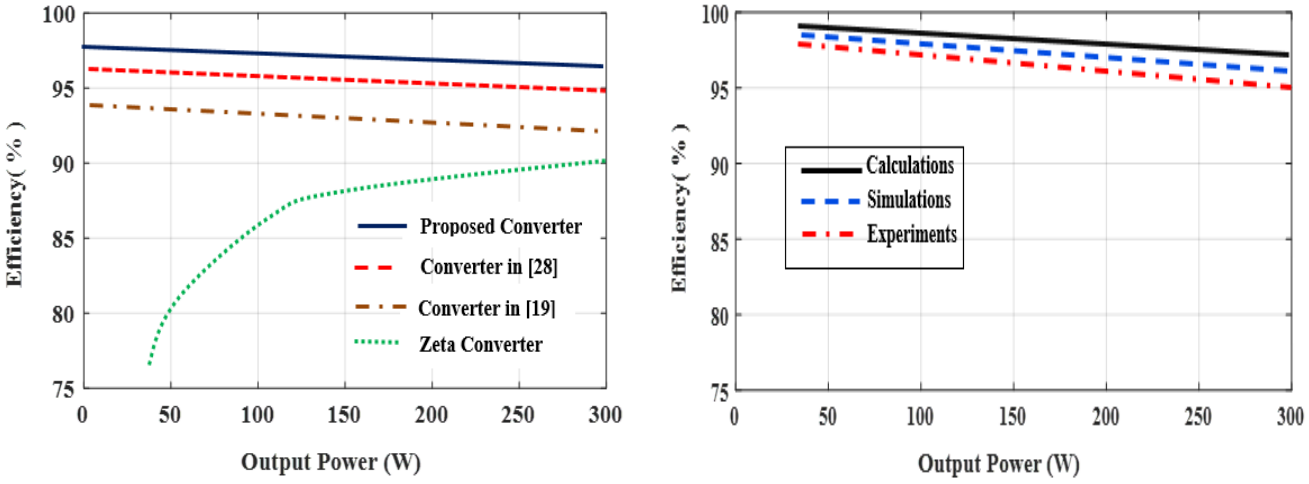


**Figure 26**. Efficiency against output power of the proposed converter

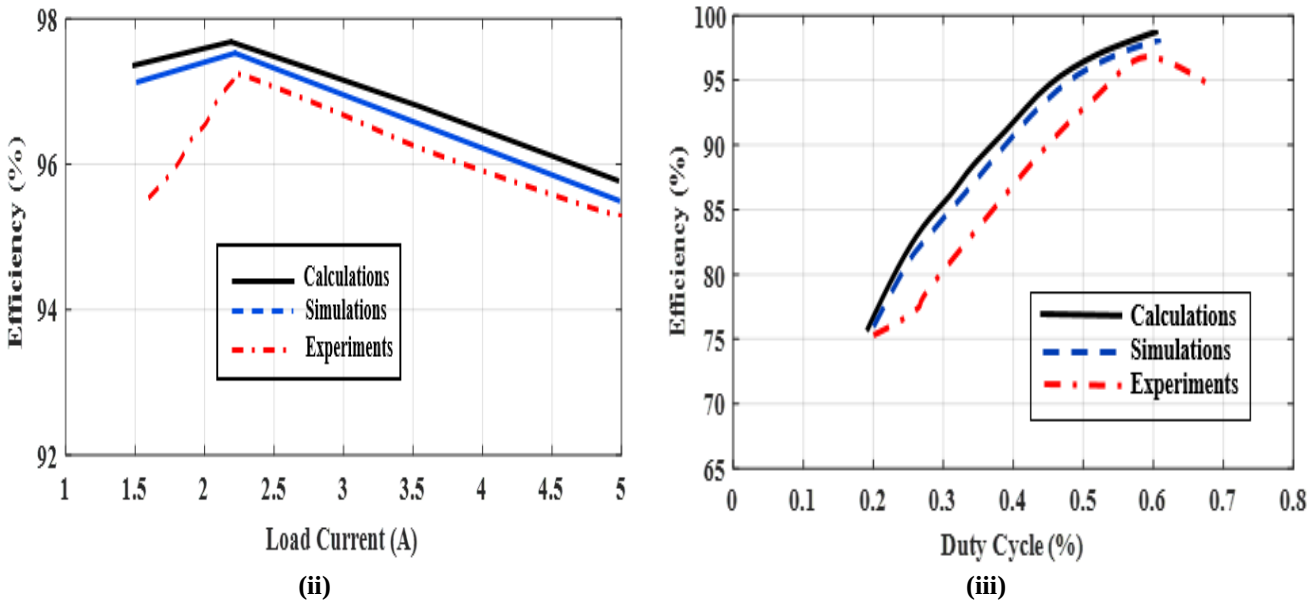


**Figure 27.** Evaluation of the efficiency of the proposed buck-boost converter by calculations, simulations, and experiments (i) In step-up mode, efficiency vs output power (ii) In step-up mode, efficiency vs load current, (iii)Efficiency vs duty cycle

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**Table IV -** A comparative analysis of the proposed converter to a range of different converters

| S. No | Converter [24] | Converter (14) | Converter [25] | ZETA Converter | Traditional Buck-boost converter | KY converter [21] | Converter (28) | Proposed converter |
|---|---|---|---|---|---|---|---|---|
| Switches used | 2 | 2 | 3 | 1 | 1 | 2 | 1 | 1 |
| Diodes used | 4 | 2 | 3 | 1 | 1 | 1 | 3 | 2 |
| Capacitors used | 4 | 2 | 1 | 2 | 1 | 3 | 5 | 4 |
| Inductors used | 4 | 2 | 2 | 2 | 1 | 2 | 3 | 3 |
| Total component count | 14 | 8 | 10 | 6 | 4 | 8 | 12 | 10 |
| Voltage stress of the switch($V_s/V_{in}$) | $\frac{V_o}{4N+4}$ | $S_1=\frac{1}{1-D}$ $S_2=\frac{D}{(1-D)^2}$ | $1\left[\frac{V_o}{V_i}\right]\frac{V_o}{V_i}$ | $\frac{V_0+V_i}{V_i}$ | $\frac{1}{(1-D)}$ | $\frac{V_o}{V_i}$ | $\frac{V_0+3}{3}$ | $\frac{V_0-2V_i}{2V_i}$ |
| Voltage Gain | $\frac{4N+4}{1-D}$ | $\frac{D^2}{(1-D)^2}$ | $\frac{2D}{(1-D)}$ | $\frac{D}{(1-D)}$ | $\frac{D}{(1-D)}$ | $2D$ | $\frac{3D}{1-D}$ | $\frac{2D}{1-D}$ |
| Efficiency (%) | 94.5 | 92.5 | 96.2 | 90 | 85 | 95 | 96 | 97.4 |

## 5. Conclusion

This article describes a transformerless DC-DC converter for high-efficiency applications requiring large voltage step-down and step-up ratios. Some of the attributes could be summarized in the following points. With a moderate duty cycle, a high step-up and step-down voltage conversion ratio has been enforced. High efficiency owing to the use of reduced MOSFETs throughout the consolidated single-stage and the use of low-voltage high-performance power switches, making it an accurate frequency operation. The non-pulsating current and decreased current ripple are the results of the alternative research. The article examines the envisaged converter's steady-state operational activities. To illustrate the effectiveness of the suggested configuration, modeling of 36 V to 89 V 248 W converters have been designed and developed, and it accomplished a peak efficiency of 97.4 percent. This same parametric study was verified by simulated and experimental results. The proposed converter employs an FLC controller strategy and has a 0 percent overshoot with an output voltage of 89 V. It compares with the performance of the Proportional integral (PI) controller, which has a 22 percent overshoot and ANN 3.6 percent overshoot. Existing converter technologies have an output power of 205W, whereas its proposed converter has an output power of 248W. Experimental Result and MATLAB/SIMULINK tools have been used for verification as well as evaluation.

## Reference


[1] Rajasekaran,R.;& Usha Rani, P. Bidirectional DC-DC Converter for Microgrid in Energy Management System. International Journal of Electronics 2020, doi:10.1080/00207217.2020.1793418

[2] Thakre, M.P.; Sayali,S.S.; & Jain,A.M. stability and total harmonic distortion analysis of performance of grid - tied PV systems. International conference on power Engineering, control and transmission system(ICPECTS), chennai, india 2020, pp 1-6. doi: 10.1109/ICPECTS49113.2020.9337036.

[3] Mohan,N.; Underland,T.M.; & Robbins, W.P. Power Electronics: Converters Applications and Design.Wiley,New York, USA 2002. 2nd Edition, ISBN: 978-0-471-22693-2.

[4] Usha Rani,P.; & Saravanan,S. Simulation and modeling Of SEPIC converter with high static gain for renewable application Asian Conference on Energy, Power and Transportation (ACEPT), Singapore 2017. pp. 1-6. doi: 10.1109/ACEPT.2017.8168573.

[5] Tao,H.; Duarte,L.J.; & Hendrix, M.A.M. Line-Interactive UPS Using a Fuel Cell as the Primary Source. IEEE Trans. Ind Electronics 2008. 55(8). 3012-3021. doi: 10.1109/TIE.2008.918472.

[6] James,P.; Forsyth,A.; Calderon, L.G.;& Pickert,V. DC-DC converter for hybrid and all electric vehicles.inProc. 24th Int. Battery, Hybrid Fuel Cell Elect. Veh. Symp. Exhib. Stavanger, Norway 2009, 13–16, 1462–1470.

[7] Chung, H.S.; Ioinovici, A.; & Cheung,L.W. Generalized structure of Bi-directional switched-capacitor DC/DC converters. IEEE Trans. Circuit & Sys. I: Fundamental theory apply 2003, 50(6), 743 – 753. doi: 10.1109/TCSI.2003.812615.

[8] Law, K.K.; Cheng, E.W.K.;& Yeung, B.P.Y. Design and analysis of switched-capacitor-based step-up resonant converters. IEEE Trans. Circuit & Sys. I: Regular papers 2005,52 (5),943–948.doi: 10.1109/TCSI.2004.840482.

[9] Zhang, F.; Du, L.; Peng, F.Z.; & Qian, Z. A New Design Method for High-Power High-Efficiency Switched-Capacitor DC–DC Converters. IEEE Trans Power Electronics 2008, 23(2),832-840. doi: 10.1109/TPEL.2007.915043

[10] Wu, T.; Lai,Y.; Hung,J.; & Chen,Y. Boost Converter With Coupled Inductors and Buck–Boost Type of Active Clamp. IEEE Trans. ind Electronics 2008,55(1),154 – 162. doi: 10.1109/TIE.2007.903925

[11] Tahavorgar, A.; & Quaicoe,E.J. A Dual Series-Resonant DC–DC Converter. IEEE Trans. Power Electronics 2017, 32(5), 3708 - 3718. doi: 10.1109/TPEL.2016.2593867

[12] Zhao, Y.; Li, W.; & He.X. Single-phase improved active clamp coupled inductor-based converter with extended voltage doubled doubler cell. IEEE Trans Power Electronics 2012, 27(6), 2869-2878. doi: 10.1109/TPEL.2011.2176752

[13] Miao,S.; Wang, F.; & Ma, X. A new transformerless buck-boost converter with positive output voltage. IEEE Trans.Ind Electronics 2016, 63(5),2965–2975. doi: 10.1109/TIE.2016.2518118

[14] Wu, G.; Ruan, X.;&Ye.Z. Non-isolated high step-up DC-DC converter adopting switched capacitor cell, IEEE Trans. Ind Electronics 2015, 62(1)383–393.doi: 10.1109/TIE.2014.2327000.

[15] Hwu,K.I.; &Jiang, W. Z. Analysis, design and derivation of a two-phase converter. IET Power Electronics 2015,8 (10), 1987 – 1995. doi: 10.1049/iet-pel.2014.0634

[16] Hou, S.; Chen,J.; Sun, T.;& Bi X. Multi-input step-up converter based on the switched diode capacitor voltage accumulator. IEEE Trans Power Electronics 2016, 31(1), 381 – 393. doi: 10.1109/TPEL.2015.2399853

[17] Dwari, S.;& Parsa, L. an efficient high step-up interleaved Dc-Dc converter with a common active clamp. IEEE Trans. Power Electronics 2011, 4(1), 66 – 78. doi: 10.1109/TPEL.2010.2051816.

[18] Lin, B.R.;& Chen, J.J. Analysis of an integrated flyback and Zeta converter with active clamping technique. IET Power Electronics 2009,2(4),355 – 363. doi:10.1049/iet-pel.2008.0038.

[19] Banaei, M. R., & Bonab, F.A.H. High-efficiency transformerless buck-boost DC-DC converter: High-Efficiency Buck-Boost DC-DC Converter. International Journal of Circuit Theory and Applications 2017, 45(8), 1129–1150. doi:10.1002/cta.2310

[20] Hwu, K. I.;& Peng, T. J. A Novel buck-boost converter combining KY and buck Converters. IEEE Trans power Electronics 2012, 27(5),2236–2241 .doi:10.1109/TPEL.2011.2182208.

[21] Sadaf, S.; Mahajan, B.; Meraj, M.; Iqbal.A.; & Alemadi. N. Transformer – less boost converter with reduced voltage stress for high voltage step-up application. IEEE Tras Ind Electronics 2021, doi: 10.1109/TIE.2021.3055166.

[22] Ai, J. ;& Lin, M. High Step-up Dc-Dc converter with low power device voltage stress for a distributed generation system. IET Power Electronics 2018,11(12),1955–1963. doi:10.1049/iet-pel.2017.0526

[23] Banaei, M. R.;& Ajdar Faeghi Bonab, H. A transformerless high step-up conversion ratio dc–dc converter with voltage multiplier. EPE Journal 2018, 1–11. doi:10.1080/09398368.2018.1548803

[24] Rajaei, A.; Khazan, R.; Mahmoudian, M.; Mardaneh, M.; & Gitizadeh. M.. A Dual inductor high step-up Dc/Dc converter based on the Cockcroft Walton multiplier. IEEE Trans Power Electronics 2018, 33(11),9699–9709. doi:10.1109/TPEL.2018.2792004

[25] Bonab, F.A.H.; & Banaei, M. R.. Enhanced Buck-Boost DC-DC Converter with Positive Output Voltage. Journal of Circuit, Systems and Computers 2019, doi:10.1142/s0218126620500723

[26] Banaei, M.R.; & Bonab, F.A.H. A novel structure for single switch nonisolated transformerless buck-boost DC-DC converter. IEEE Trans on Ind Electronics 2017. 64(1),198 -205. doi: 10.1109/TIE.2016.2608321

[27] Qin, Y.; Yang, S.; Li, Y.; Huang ,Y.; Tan,C-S, & Hui, Y.S. A high-efficiency Dc-Dc converter for high voltage gain, high current applications. IEEE journal Emerging & Selected Topics Power Electronics 2020, 8(3),2812-2823. doi: 10.1109/JESTPE.2019.2908416.

**[28]** Ansari, A.S.; & Moghani,S.J..A novel high voltage gain non-coupled inductor sepic converter. IEEE Trans on Ind Electronics 2019,66(9), 7099 -7108.doi: 10.1109/TIE.2018.2878127.

**[29]** Banaei, M. R.; & Bonab,H.A.F. A High Efficiency Nonisolated Buck–Boost Converter Based on ZETA Converter. in IEEE Transactions on Industrial Electronics 2020,67(3), 1991-1998. doi: 10.1109/TIE.2019.2902785.

**[30]** Khan, S.; Mahmood, A.; Zaid, M.; Tariq, M.; Lin, C.-H.; Ahmad, J.; Alamri, B.; Alahmadi, A. A High Step-up DC-DC Converter Based on the Voltage Lift Technique for Renewable Energy Applications. Sustainability 2021, 13, 11059. https://doi.org/10.3390/su131911059

**[31]** Leso, M.; Zilkova ,J.; & Girovsky.P. Development of a Simple Fuzzy Logic Controller for DC-DC Converter. IEEE 18th int. power electronics and motion control conference (PEMC) 2018, 86-93. doi: 10.1109/EPEPEMC.2018.8521896.

**[32]** Thakre, M.P.; Kumar, N. Evaluation and Control Perceptive of VSM-Based Multilevel PV-STATCOM for Distributed Energy System. MAPAN 2021.. https://doi.org/10.1007/s12647-021-00481-x

**[33]** Ramaprabha, R.; & Shanmuga Vadivu, K. Investigation on the performance of controllers for Three-Level PFC converter for a wide operating range. Advance in Electrical and Computer Engineering 2020, 20(1), 91-98. doi:10.4316/AECE.2020.01012