 doi:10.20944/preprints202109.0513.v1

Article

Back-channel etched In-Ga-Zn-O Thin-film Transistor utilizing Selective Wet-Etching of Copper Source and Drain

Rauf Khan [1,2,*], Muhamad Affiq Bin Misran [1,2], and Reiji Hattori [1]

[1] Department of Applied Science for Electronics and Materials, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Fukuoka 816-8580, Japan; muhamad.affiq90@gmail.com (M.A); hattori@gic.kyushu-u.ac.jp (R.H.)
[2] Transdisciplinary Research and Education Center for Green Technologies, Kyushu University, Fukuoka 816-8580, Japan
* Correspondence: rauful.karim@gmail.com

Abstract: The electrical performance of the back-channel etched Indium–Gallium–Zinc–Oxide (IGZO) thin-film transistors (TFTs) with copper (Cu) source and drain (S/D) which are patterned by a selective etchant was investigated. The Cu S/D were fabricated on molybdenum (Mo) layer to prevent the Cu diffusion to the active layer (IGZO). We deposited the Cu layer using thermal evaporation and performed the selective wet etching of Cu using non-acidic special etchant without damaging the IGZO active layer. We fabricated the IGZO TFTs and compare the performance in terms of linear and saturation region mobility, threshold voltage and ON current (I_{ON}). The IGZO TFTs with Mo/Cu S/D exhibits good electrical properties as the linear region mobility is 12.3 cm^2/V-s, saturation region mobility is 11 cm^2/V-s, threshold voltage is 1.2 V and I_{ON} is 3.16 x 10^{-6} A. We patterned all the layers by photolithography process. Finally, we introduced SiO_2-ESL layer to protect the device from the external influence. The results show that the prevention of Cu and introduced ESL layer enhances the electrical properties of IGZO TFTs.

Keywords: IGZO TFTs; Cu Thermal diffusion; Selective etching of Cu; Barrier layer; DC Sputtering

1. Introduction

Nowadays Indium–Gallium–Zinc-Oxide (IGZO) thin-film transistors (TFTs) have received considerable research attention as active-matrix backplanes for the next generation display technology [1]–[3]. Recently, IGZO TFTs are used as a switching device in the flat panel display such as active-matrix organic light-emitting diode (AMOLED) displays, active-matrix liquid crystal displays (AMOLCD) and Electrophoretic displays [4], [5]. Most of the studies are focused on the electrical, electronic, optical and thermal properties of IGZO thin films [6], [7]. As increasing the resolution (≥ 8 K), display size (≥ 110 inch) and high frame rate (≥ 480 Hz) for the flat panel display; the low-resistance metals are highly required for the source (S) and drain (D) electrodes of IGZO TFTs to reduce resistance-capacitance (RC) delay of display panel to avoid image distortion and shading [8]–[10]. However, several reports have been revealed that the diffusion of Cu into IGZO deteriorates the electrical performance because it is acting as acceptor-like trap states of IGZO TFT [11]–[15]. Recently, a low resistance stacked structure of S/D on IGZO was introduced to enhance the contact properties [16]–[18]. The Ti and Mo has used widely as an interfacial layer to protect the Cu diffusion into IGZO and to reduce the impact of the Schottky barrier. The work function of Mo and Ti is 4.7 eV and 4.3 eV respectively which are very closer to IGZO (4.5 eV). In this aspect, it is very difficult to pattern the Cu selectively with Cu etchant without damaging active layer.

In this study, we investigated the performance of IGZO TFTs with Mo/Cu/Mo S/D electrodes and a passivation SiO_2 layer. We selectively wet etched the Cu with non-acidic

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 30 September 2021 doi:10.20944/preprints202109.0513.v1

special Cu etchant. Two test samples were fabricated and measured transfer characteristics and mobility according to gate voltage (V_g) to compare their performance.

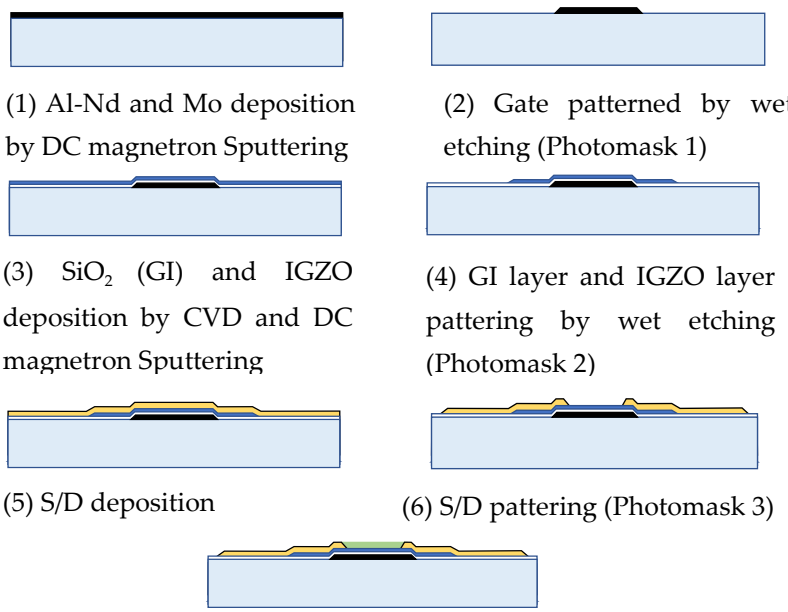


Figure 1. Process flow of bottom gate top contact IGZO TFTs.

2. Experimental Details

Figure 1 shows the process flow of the samples used in this report. An inverted staggered bottom-gate IGZO were prepared on a glass substrate. First, the gate electrode with Al-Nd (85 nm)/ Mo (15 nm) was deposited on a glass substrate by DC magnetron sputtering. Al-Nd alloy is deposited to avoid the electro migration and Mo is used as a barrier layer. The gate electrode was patterned using the photolithography process and wet etching. Subsequently, a gate insulator (GI) of 150-nm thick SiO_2 was formed using plasma enhanced chemical vapor deposition (PECVD). Then, a 15-nm IGZO thin film as an active layer was deposited by DC magnetron sputtering in the mixture gas of Ar and Ar-O_2 (90%-10%) at 150°C, from the ceramic target atomic ratio In:Ga:Zn = 1:1:1. The deposition chamber pressure was evacuated less than $1x10^5$ Pa and the working pressure was 1 Pa. Afterthat the active layer and GI layer was patterned. The oxygen partial pressure was calculated as [P (O_2) = O_2 / (Ar + O_2)] and fixed at 1%. A 40 nm of 99.999% pure Cu interlayer was deposited on patterned active layer for Sample A. Stacked films of 20 nm Mo and 40 nm Cu were deposited for sample B using thermal evaporation and patterned again the S/D contact for all samples. Thinner Cu layer was deposited to reduce contact resistance, but it is possible to deposit thicker one. The special Cu etchant etch the Cu layer only, which doesn't etch the IGZO active layer. S/D were patterned by photo mask and photolithography process. Active channel width and length were 10 μm and 20 μm, respectively. Finally, 200 nm SiO_2 passivation layer was deposited for both device with working pressure at 110 Pa at 200° C by chemical vapor deposition (CVD) process. Furuta et al. reported that certain amount of H_2 may diffused into IGZO active layer from passivation layer, which can act as a shallow donor in IGZO films [19]. The SiO_2 passivation layer was deposited at the partial pressure of SiH_4 of P[SiH_4] = 1.36 % using N_2, SiH_4 and N_2O gases.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 30 September 2021 doi:10.20944/preprints202109.0513.v1

This passivation layer was also patterned by photolithography process to make the contact. At the end, all the devices were annealed at 350° C at N_2 environment for 1 hour. The cross-sectional views of the TFT for Samples A and B are shown in Figure. 2(a) and (b). respectively, and the plane view is illustrated in Figure 2(c).

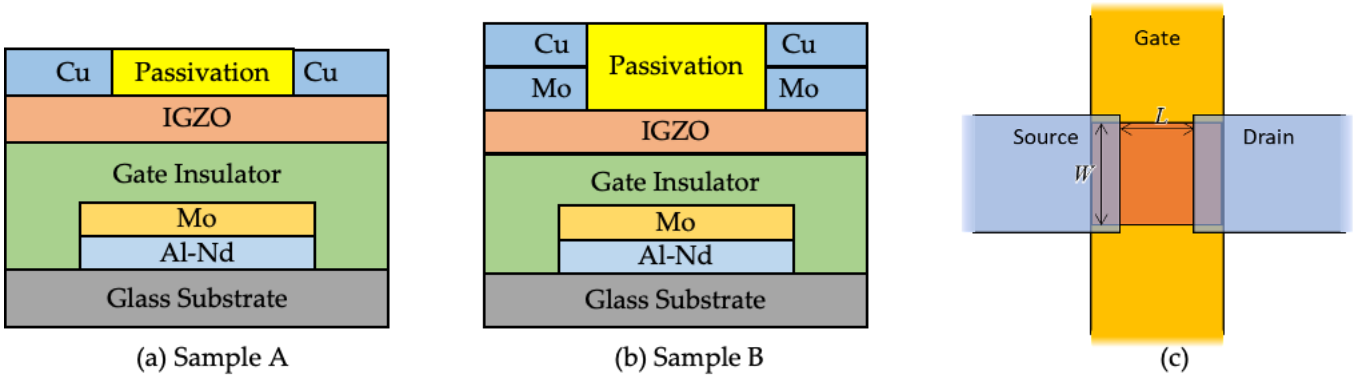


Figure 2. Schematic cross-section of IGZO TFT on a glass substrate with bottom gate top contact structure. (a) sample A, (b) Sample B , and (c) top view of IGZO TFTs.

3. Results

The active layer defines the channel width, and the separation of S/D electrodes defines the channel length. In this design, we can define the channel width correctly by the active layer width, but the edge of the active layer has a chance to be damaged by the etching. As shown later, we have problems with *SS* value and leakage current even after improving the mobility value. Therefore, there is still plenty of room for improvement in design the TFT layout. Figure 3 (a) and (b) show the microscopic image of IGZO TFTs samples with no defects after using Cu etchant.

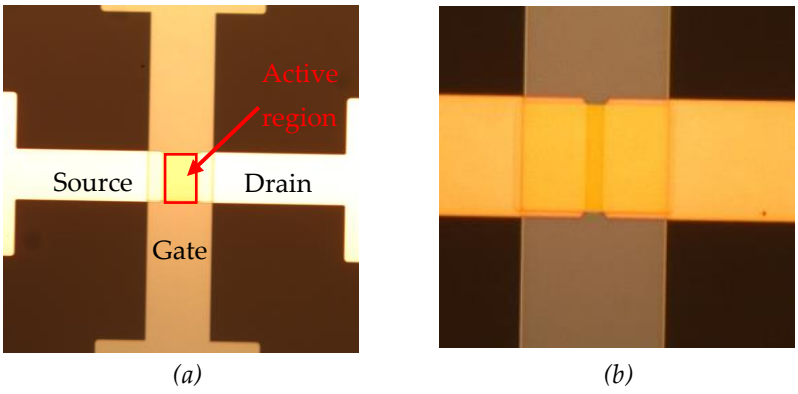
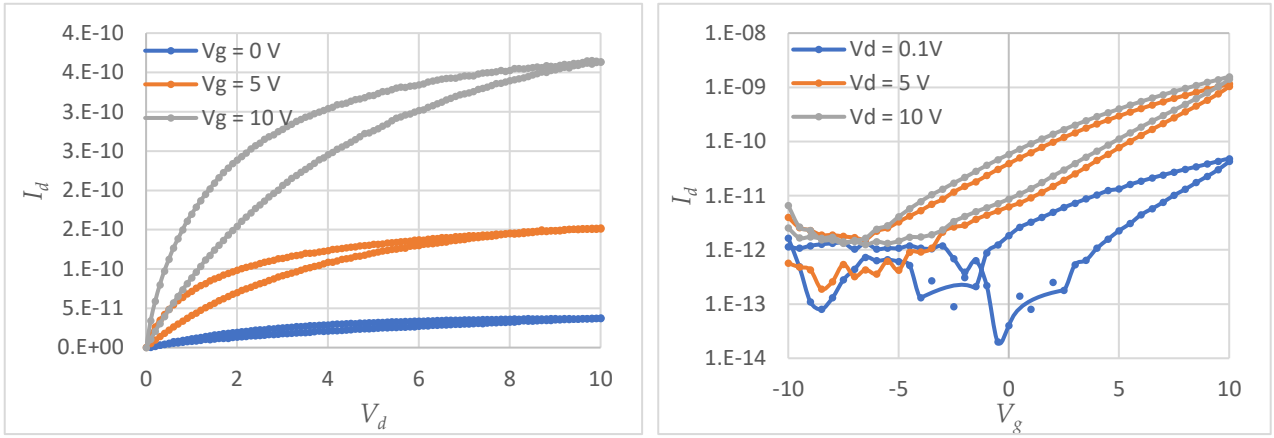


Figure 3. Microscopic image of bottom gate top contact IGZO TFTs after using the special Cu etchant.

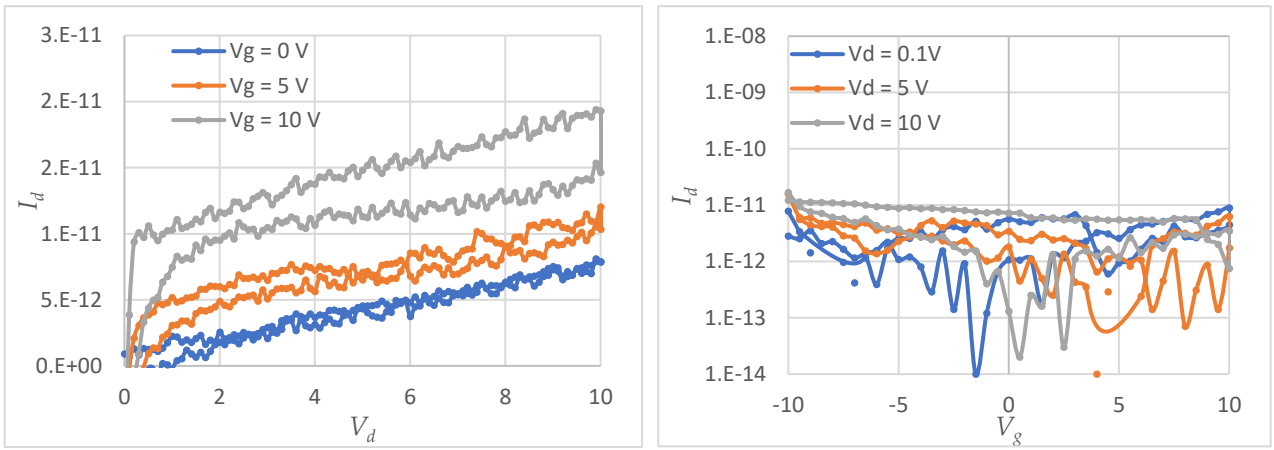
Ferric chloride ($FeCl_3$), Cupric Chloride ($CuCl_2$), Hydrogen peroxide - Sulphuric acid (H_2O_2-H_2SO_4), Chromic - Sulphuric acid (CrO_3-H_2SO_4), ammonium persulphate ($(NH_4)_2SO_4$) and Citric acid are widely used as a Cu etchant but all of them contains strong acid such as HCL and H_2SO_4 [20][21][22]. All the etchants have high etched rate, high Cu dissolved capacity and very acidic [23]. For this reason, those acidic Cu etchants can damage the IGZO layer and device structure easily and affect the device performance, respectively. Because of this reason, most of the researchers are using shadow mask to deposit S/D to avoid wet Cu etchant [18][24][25][26]. TFTs characteristics are usually presumed from the transfer characteristics, where the drain to source current (I_d) is plotted against gate to source voltage (V_g) for various drain to source voltage (V_d) and from output characteristics, where I_d is plotted against drain to source voltage (V_d) for various gate to source voltage (V_g) as shown in figure 4. The parameters of the output

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 30 September 2021 doi:10.20944/preprints202109.0513.v1

characteristics, transfer characteristics of sample A and B are as follows; the gate voltage (V_g) was 0 V, 5 V and 10 V and drain voltage was 0.1 V, 5 V and 10 V, respectively. At the value of drain voltage (V_d) at 1 V, threshold voltage (V_{th}) represents the gate voltage (V_g) corresponding to the drain current (I_d) of 1 x 10^{-9} A. The



(a)



(b)

Figure 4. Output (left side) and transfer characteristics (right side) of sample A (a) Pre-annealing and (b) post-annealing.

electrical characteristics of device performance are extracted by analyzing several parameters, such as saturation region mobility (μ_{SAT}), field-effect mobility (μ_{FE}), threshold voltage (V_{th}), On-Current (I_{ON}) and subthreshold swing (SS). The field-effect mobility is evaluated based on gradual channel approximation and the equation is as follows,

$$\boldsymbol{I_d = \frac{W}{L}\mu C_i[(V_g - V_{th})V_d - \frac{V_d^2}{2}]} \quad (1)$$

Here, μ is the channel carrier mobility, W and L are channel width and length, and C_i is the gate capacitance per unit area of the insulator layer. Furthermore, the saturation region mobility was obtained from the curve of the square root of the drain current versus the V_g in saturation operation region:

$$\boldsymbol{\sqrt{I_d} = (\frac{WC_i\mu_{SAT}}{2L})^{1/2}(V_g - V_{th})} \quad (2)$$

Another important parameter subthreshold swing (SS) reflects the change of V_g instead of increase I_d; is determined by,

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 30 September 2021 doi:10.20944/preprints202109.0513.v1

$$SS = \frac{dV_g}{dlog_{10}(I_d)} \quad (3)$$

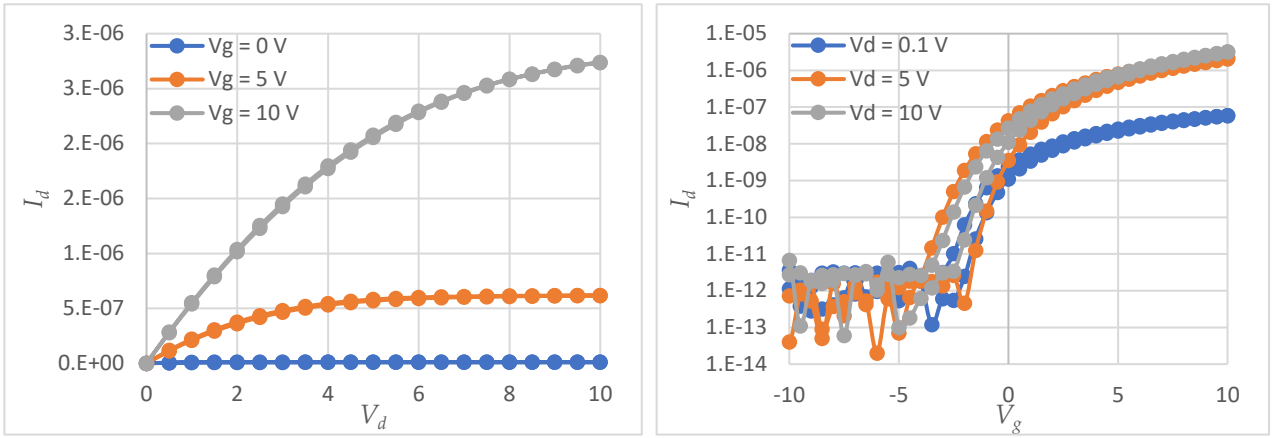


Figure 5. Output (left side) and transfer characteristics (right side) of sample B after annealing.

Figure 4 represents the output and transfer characteristics of sample A. The electrical characteristics of figure 4 (a) are better comparing figure 4 (b) though the mobility is tiny and threshold voltage is quite high. Figure 4 (a) is the electrical properties of sample A, which are calculated before annealing the sample. Moreover, the electrical characteristics of sample A are becoming worst after post-annealing. The reason might be described by the diffusion of Cu into the IGZO layer for post annealing after deposition Cu S/D contact or for depositing Cu onto the channel layer directly. Figure 4 (a) has been extracted before annealing. Therefore, it has less chance of Cu diffusion into IGZO layer. Sample B has a 15-nm-thick Mo layer at the S/D contact, which makes ohmic contacts after annealing and prevents the diffusion of Cu into the IGZO layer. Figure 5 shows the output and transfer characteristics of sample B after post-annealing. The sample B for W/L of 10/20 (μm/μm) achieves improved performance as follows: V_{th} of 1.2 V, μ_{SAT} of 11 cm²/V-s, and I_{ON} of 3.16×10^{-6} A. This experimental data assure that the non-acidic selective Cu etchant has no effect on IGZO layer. The hysteresis has minimized completely from the output characteristics, but still there is hysteresis at transfer characteristics. The SS value becomes high because the density of acceptor-like trap states of IGZO is also increased. Hu et al. reported the field effect mobility around 11.5 cm²/V-s with ITO barrier layer [25]. On the other hand, Kim et al. also reported the field effect mobility around 12.8 cm²/V-s with Mo-Ti/Cu S/D [26]. These results are quite similar to our experimental results. The H_2 atom from passivation layer may diffused into IGZO layer because of annealing which can enhance the electrical properties. Table 1 exhibits the details analysis between sample A and B after post-annealing.

The electrical performance of the TFTs is summarized in Table 1.

S/D	μ_{FE} (cm²/V-s)	μ_{SAT} (cm²/V-s)	V_{th} (V)	I_{ON} (A)	*SS* (V/decade)
Cu	9.2×10^{-5}	1.8×10^{-5}	5	1.6×10^{-9}	-
Mo/Cu	12.3	11	1.2	3.2×10^{-6}	0.58

4. Conclusion:

In summary, we have successfully fabricated a high mobility IGZO TFT with Mo-Cu S/D contact using special non-acidic Cu etchant, which can etch Cu properly and avoid the damage to IGZO layer. The electrical properties of IGZO TFTs with Mo/Cu S/D ensure the selectivity of Cu etchant. Post annealing treatment formed an improved the TFT characteristics and Mo interlayer prevent the Cu diffusion into active layer. Thus, the TFT with Mo-Cu S/D exhibited proper switching characteristics with saturation mobility at 11 cm²/V-s. The results suggested an effective fabrication method for fabricating high mobility metal oxide TFT based on Cu S/D.

Author Contributions: Conceptualization, R.K., R.H.; methodology, R.K., R.H.; software, R.K.; validation, formal analysis, R.K., M.A. and R.H.; investigation, R.K.; resources, R.K., R.H.; data curation, R.K., M.A.; writing—original draft preparation, R.K.; writing—review and editing, R.H.; supervision, R.H. All authors have read and agreed to the published version of the manuscript

Data Availability Statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

Acknowledgments: The support from Kyushu University and the Ministry of Education, Culture, Sports, Science, and Technology (MEXT), Japan, is highly appreciated.

Conflicts of Interest: The authors declare no conflict of interest.

References

[1] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors," *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers*, vol. 45, no. 5 B. pp. 4303–4308, 2006, doi: 10.1143/JJAP.45.4303.

[2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, 2004, doi: 10.1038/nature03090.

[3] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor," *Science (80-.).*, 2003, doi: 10.1126/science.1083212.

[4] J. S. Park, W. J. Maeng, H. S. Kim, and J. S. Park, "Review of recent developments in amorphous oxide semiconductor thin-film transistor devices," *Thin Solid Films*. 2012, doi: 10.1016/j.tsf.2011.07.018.

[5] J. Martins *et al.*, "Bias stress and temperature impact on InGaZnO TFTs and circuits," *Materials (Basel).*, vol. 10, no. 6, 2017, doi: 10.3390/ma10060680.

[6] Y. Fujimoto, M. Uenuma, Y. Ishikawa, and Y. Uraoka, "Analysis of thermoelectric properties of amorphous InGaZnO thin film by controlling carrier concentration," *AIP Adv.*, vol. 5, no. 9, p. 097209, Sep. 2015, doi: 10.1063/1.4931951.

[7] R. Khan, M. Ohtaki, S. Hata, K. Miyazaki, and R. Hattori, "Thermal Conductivity of Nano-Crystallized Indium-Gallium-Zinc Oxide Thin Films Determined by Differential Three-Omega Method," *Nanomaterials*, vol. 11, no. 6, 2021, doi: 10.3390/nano11061547.

[8] S. H. Lee *et al.*, "Improvement in Device Performance of a-InGaZnO Transistors by Introduction of Ca-Doped Cu Source/Drain Electrode," *IEEE Electron Device Lett.*, 2015, doi: 10.1109/LED.2015.2445348.

[9] M. Zhao *et al.*, "Method for Fabricating Amorphous Indium-Zinc-Oxide Thin-Film Transistors With Copper Source and

Drain Electrodes," *IEEE Electron Device Lett.*, 2015, doi: 10.1109/LED.2015.2400632.

[10] T. Arai, "Oxide-TFT technologies for next-generation AMOLED displays," *J. Soc. Inf. Disp.*, vol. 20, no. 3, 2012, doi: 10.1889/jsid20.3.156.

[11] W. S. Kim, Y. K. Moon, K. T. Kim, J. H. Lee, B. Du Ahn, and J. W. Park, "An investigation of contact resistance between metal electrodes and amorphous gallium-indium-zinc oxide (a-GIZO) thin-film transistors," 2010, doi: 10.1016/j.tsf.2010.02.044.

[12] J. R. Yim *et al.*, "Effects of metal electrode on the electrical performance of amorphous In-Ga-Zn-O thin film transistor," *Jpn. J. Appl. Phys.*, 2012, doi: 10.1143/JJAP.51.011401.

[13] S. Hu *et al.*, "Effect of post treatment for cu-cr source/drain electrodes on a-igzo tfts," *Materials (Basel).*, vol. 9, no. 8, 2016, doi: 10.3390/ma9080623.

[14] C. S. Youn and D. G. Lee, "Effects of post heat treatment on the mechanical properties of cold-rolled Ti/Cu clad sheet," *Metals (Basel).*, vol. 10, no. 12, 2020, doi: 10.3390/met10121672.

[15] I. Fisher and M. Eizenberg, "Copper ion diffusion in porous and nonporous SiO2-based dielectrics using bias thermal stress and thermal stress tests," *Thin Solid Films*, 2008, doi: 10.1016/j.tsf.2007.10.011.

[16] K.-H. Choi and H.-K. Kim, "Correlation between Ti source/drain contact and performance of InGaZnO-based thin film transistors," *Appl. Phys. Lett.*, vol. 102, no. 5, p. 052103, Feb. 2013, doi: 10.1063/1.4790357.

[17] L. Lan *et al.*, "Influence of source and drain contacts on the properties of the indium-zinc oxide thin-film transistors based on anodic aluminum oxide gate dielectrics," 2011, doi: 10.1063/1.3660791.

[18] S. Hu *et al.*, "Mobility enhancement in amorphous in-Ga-Zn-O thin-film transistor by induced metallic in nanoparticles and Cu electrodes," *Nanomaterials*, vol. 8, no. 4, 2018, doi: 10.3390/NANO8040197.

[19] T. Toda, D. Wang, J. Jiang, M. P. Hung, and M. Furuta, "Quantitative analysis of the effect of hydrogen diffusion from silicon oxide etch-stopper layer into amorphous In-Ga-Zn-O on thin-film transistor," *IEEE Trans. Electron Devices*, vol. 61, no. 11, 2014, doi: 10.1109/TED.2014.2359739.

[20] O. Çakır, "Review of Etchants for Copper and its Alloys in Wet Etching Processes," *Key Eng. Mater.*, vol. 364–366, 2007, doi: 10.4028/www.scientific.net/kem.364-366.460.

[21] K. R. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing - Part II," *J. Microelectromechanical Syst.*, vol. 12, no. 6, 2003, doi: 10.1109/JMEMS.2003.820936.

[22] M. Georgiadou and Richard Alkire, "Anisotropic Chemical Etching of Copper Foil," *J. Electrochem. Soc.*, vol. 140, no. 5, 1993.

[23] H. Noma and T. Nakanishi, "Etching process analysis based on etchant flow for high-density build-up substrate," 2004, doi: 10.1109/eptc.2004.1396620.

[24] S. Hu *et al.*, "Effect of Al2O3 Passivation Layer and Cu Electrodes on High Mobility of Amorphous IZO TFT," *IEEE J. Electron Devices Soc.*, vol. 6, 2018, doi: 10.1109/JEDS.2018.2820003.

[25] S. Hu *et al.*, "Effect of ITO Serving as a Barrier Layer for Cu Electrodes on Performance of a-IGZO TFT," *IEEE Electron Device Lett.*, vol. 39, no. 4, 2018, doi: 10.1109/LED.2018.2800725.

[26] L. Y. Kim and O. K. Kwon, "Effects of Stacked Mo-Ti/Cu Source and Drain Electrodes on the Performance of Amorphous In-Ga-Zn-O Thin-Film Transistors," *IEEE Electron Device Lett.*, vol. 39, no. 1, 2018, doi: 10.1109/LED.2017.2769669.