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Multi-channel Precision Bias Source for Experiments on Quantum dots

Yumei TANG [1], Kefu LIU [1], Haixing Sun[2*]

(1. School of Information Science and Technology, Fudan University, No.220 Handan Road, Shanghai, 200433, P.R. China

2.Hefei GoodTech Co., Ltd., Anhui, Hefei, 230088)

*Corresponding author: goodtek0551@163.com

Abstract:

To realize precise control of the quantum dots (Qdots) device, multi-channel precision bias source plays the key role. In this paper, the 16-channel high precision bias source with 18-bit resolution for Qdots device was designed. The prototype was made and its performance was tested. The short time fluctuations can reach 50μV. The step response time is less than 3μs. The resolution, stability, linearity and dynamic range of the bias source exhibits good performance. What's more, the bias source can be controlled locally and online. The results show that it is one effective and feasible topology for experiments in Qdots device application.

Keywords: quantum dots; bias source; multi-channel; high precision

Introduction:

Along with the rapid development of nanotechnology, quantum nano-electronics has been researched widely. Quantum dots(Qdots) is one of most significant basic structures of nano-electronics which is expected to replace traditional semiconductor technology[1, 2]. The Qdots device was widely investigated for quantum computing[3, 4], quantum detection[5, 6], quantum communication[7, 8] and quantum measurement[9-12].

Typically, a quantum dot is formed by using some surface gates to constrain electrons or holes within trapping regions in the hetero-structure samples (such as GaAs/AlGaAs) [13]. As is shown in **Fig.1[14]**, changing the gate voltages moderately will vary the various parameters of the dot, and then the conductance of this dot is measured versus the gate voltages in order to show interested features of the quantum dot[15, 16]. The bias voltage should be changed very slowly and gently so as to shuttle individual electrons into or out of the dot.

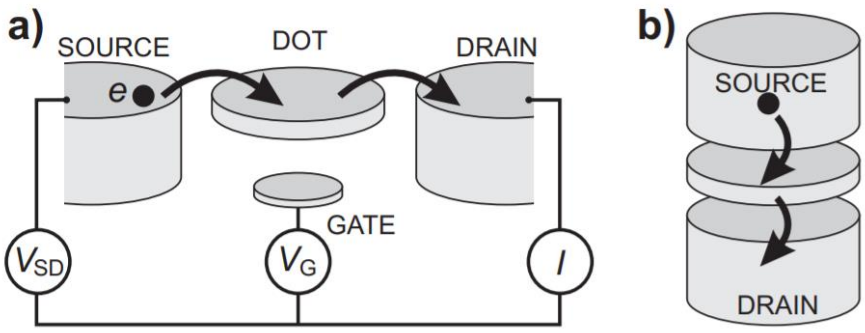

Fig.1.bias source on Qdots device application (a) a lateral geometry and (b)in a vertical geometry

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The resolution, stability, linearity and dynamic range of bias source are key factors to affect the Qdots device performance[17-20]. In order to realize precise control of single quantum dot and more complex quantum channels, it is meaningful to investigate on multi-channel bias source for Qdots device.

To our knowledge, the existing instruments are large volume with few channels or with limited accuracy[21, 22], meanwhile multi-channel and high precision bias voltage source is rarely reported in the literature. Recent years, semiconductor chip manufacturers recommend to use high resolution DAC chip to design the bias voltage source[23, 24]. Although precision DAC components are already on the market, building a multi-channel high-resolution system is not easy and cannot be treated hastily. The sources of system error must be fully considered, which occur at this level of accuracy. In high-resolution circuits, the main error sources are noise, temperature drift, thermoelectric voltage, and physical stress. The construction technology of precision circuits should be followed to minimize the coupling and propagation effects of such errors in the entire circuit and avoid external interference. To further complicate the issue, mixed-signal ICs have both analog and digital ports, and because of this, much confusion has resulted with respect to proper grounding techniques. In addition, some mixed-signal ICs have relatively low digital currents, while others have high digital currents. In many cases, these two types must be treated differently with respect to optimum grounding[25]. Finally, because the gate bias of the quantum dot is a capacitive load, which will change the phase of the system, it is necessary to design a compensation network to improve the stability of the bias voltage source.

Design and analysis:

1)system design

As shown in Fig.2, this system was consisted of digital circuit, analog circuit, LCD display & keys, linear AC-DC power and remote communication system. With the main controller (MCU, STM32F407VE) as the core, 18-bit DAC (AD5781, ADI) is used in the design of the bias source. The command of voltage value is transmitted to the MCU by ethernet or keys, and then the decoded data and synchronization signal are simultaneously input to the precision DACs after decoding and matching. With a buffer unit, the remote computer system gets the final voltage with a high-precision multi-meter (Agilent 3458A), and establishes a correction model to achieve the calibration of the offset voltage.

The bias source system is completely separated the digital circuit and the analog circuit, and uses independent power and ground processing. The signal transmission between the two is isolated from each other through the optocoupler, so as to ensure that the digital circuit noise does not enter the analog circuit.

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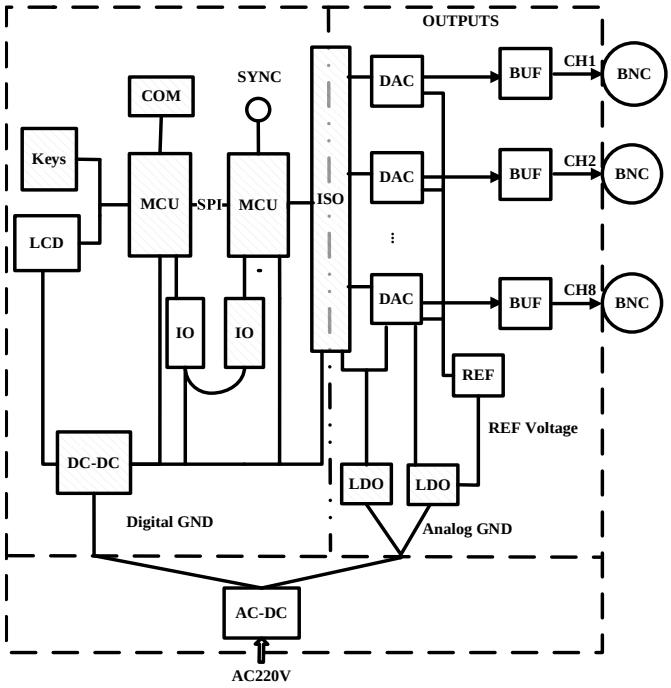

Fig.2. system block

The output voltage expression[26] of 18 bit DAC is:

$$V_{out} = \frac{(V_{refp} - V_{refn}) * D}{2^{18} - 1} + V_{refn} \quad (1)$$

where:

Vrefn provides a negative reference voltage for the DAC;

Vrefp provides a positive reference voltage for the DAC;

D is an 18-bit binary programming value.

2) Output voltage accuracy and temperature drift analysis

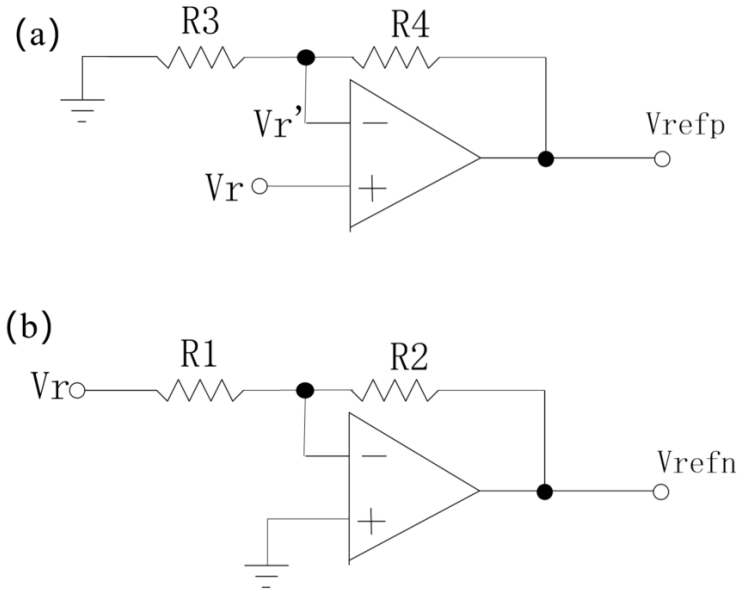

Fig.3. (a) positive polarity reference voltage ; (b) negative polarity reference voltage

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As shown in **Fig 3**(a), Vr is the reference voltage, we choose an ultralow noise, LDO XFET voltage references with current sink and source(ADR445B, ADI), temperature coefficient is 2ppm,the output voltage is 5V±2mV.

Regardless of the influence of the OPA bias current, assuming that the op amp offset voltage is Vos1, let Vr'=Vr+Vos1, according to the "virtual disconnection" principle, the following formula：

$$\frac{V_r'}{R3} = \frac{V_{refp} - V_r'}{R4} \qquad (2)$$

So that,

$$V_{refp} = \left(1 + \frac{R4}{R3}\right) V_r' \qquad (3)$$

As shown in Fig 3(b), assuming that the op amp offset voltage is Vos2, let Vr''=Vr+Vos2, and the same can be obtained:

$$\frac{V_r''}{R1} = \frac{-V_{refn}}{R2} \qquad (4)$$

$$V_{refn} = -V_r'' * \frac{R2}{R1} \qquad (5)$$

Where :

Vrefn provides a negative reference voltage for the DAC;

Vrefp provides a positive reference voltage for the DAC.

Substituting formula (2), (3), (4), (5) into formula (1), we can get:

$$V_{out} = \left(\left(1 + \frac{R4}{R3}\right) * (Vr + Vos1) + \frac{R2}{R1} * (Vr + Vos2)\right) * \frac{1}{2^{18}-1} * D - \frac{R2}{R1} * (V_r + Vos2) \qquad (6)$$

Assuming that R2/R1, R4/R3, Vr, Vos1, Vos2 do not change with temperature and time, Vout can be simplified to:

$$Vout = a * D + b \qquad (7)$$

Here, R1, R2, R3, R4 use Vishay bulk metal thin film voltage divider resistor series 300144Z and 300145, its resistance tracking temperature coefficient is 0.1 ppm/°C.

It can be seen from the above formula that the bias output voltage will be affected by the drift of the DAC, resistance, reference voltage, and operational amplifier.

The reference voltage source adopts ADR445BRZ to output 5V, and the temperature drift is about 2ppm/℃, which is 10 uV/℃.

The temperature drift of the voltage divider resistance is about 2ppm, and the temperature drift of the voltage divider resistance is required to be consistent, and the tracking temperature coefficient is less than 5 uV/℃.

The offset drift of AD8676 is about 0.6 μV/°C. AD5781 has a very low temperature coefficient of about 0.05ppm/°C, which is much lower than the drift of the reference voltage source.

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Ignoring the temperature drift of the op amp and DAC, it is mainly affected by the reference voltage source, and the drift is about 20 uV/°C.

Generally speaking, for a 20V voltage range, 18-bit system, the temperature drift is required to be controlled within 80uV, and the temperature cannot change more than 4 degrees.

3) Capacitive load analysis

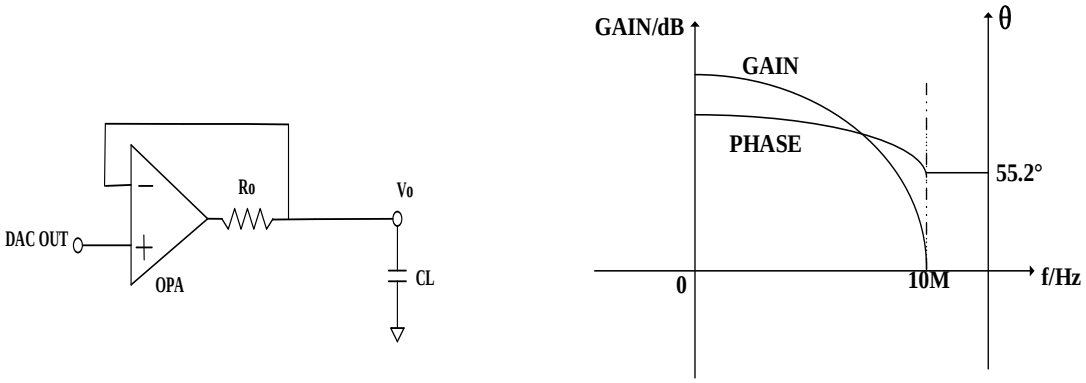

Fig.4. (a) DAC output buffer (b) Gain and Phase vs. Frequency (AD8676, ADI)

As is shown in **Fig.4(a)**, the ideal operation state of the amplifier is that the output voltage and the input voltage are in phase. However, the input and output phases of amplifiers with capacitive load are always different. When the phase difference between the output and the output is 180°, the negative input is exactly the same as the positive input, but the output that should be reduced is enhanced. It becomes a state of positive and negative collapse. If it falls into this state in a certain frequency band and remains the original amplitude, the output frequency and oscillation state will continue.

$$A_{CL} = \frac{U_O}{U_i} = \frac{Z_O}{R_O} = -j * \frac{1}{2\pi * C_L * f * R_O} \tag{7}$$

$$f_p = \frac{1}{2\pi * C_L * R_O} > 10MHz, \text{ while } A_{CL} > 10MHz \tag{8}$$

while $f_p > 10MHz, R_o > 40\Omega, C_L < 400pF$, there will be no shock in the circuit.

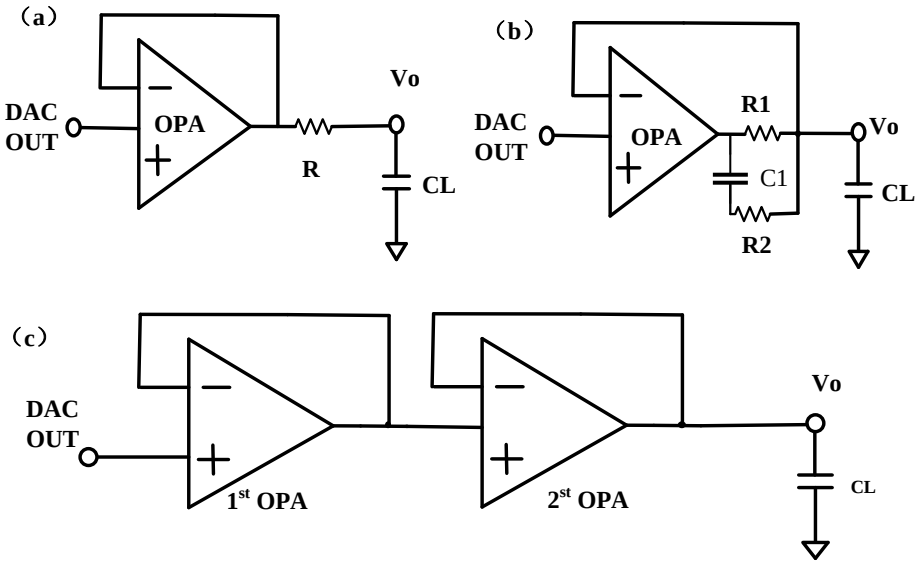

Fig.5 (a) insert resistance; (b)Miller compensation; (c) two stage OPA

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As is shown in Fig.5(a), insert series resistance R to eliminate the phase lag of feedback loop due to CL. In high frequency region, R is shown as the load of OPA. Although R is added to the outside of the feedback loop, the series resistance R can act on the transfer function of the feedback network by the additional zero frequency (FZ) generated by the load capacitance, thus reducing the phase shift of the high frequency loop. In order to ensure the stability of the circuit, the value of R should make the additional zero frequency at least 10 times lower than the closed-loop bandwidth of the OPA circuit. This method is feasible, but increasing the output impedance will reduce the power efficiency.

As is shown in Fig.5(b), the phase lag caused by CL is eliminated by pre-correction with C1(Miller compensation). This method is generally easy to implement in the chip, but difficult to implement on the circuit board.

As is shown in Fig.5(c), the phase delay caused by CL is compensated by the advanced correction, which is equivalent to adding a buffer at DAC output stage, and responding in time to the first stage OPA response. This method has obvious effect. If a small resistor is connected in series, the output stability is better.

Results and discussion:

The multi-channel precision bias source (MPBS-16) prototype was shown in Fig.6.The LCD screen and controller were distributed in the front panel layout. The input-power, power controller, multi-output, synchronous trigger port, RS232 interface and ethernet interface were distributed in the rear panel layout. The size of prototype is 437mm*420mm*133mm (3U chassis size).

Fig. 6. (a) the front panel layout of prototype (b) the rear panel layout of prototype

1) Linearity

Set the output of the voltage source in the program, from the minimum value that can be set to the maximum value that can be set, in steps of 10 mV. Wait for 0.5s after setting the voltage value each time, and then use the 8.5-digit digital multi-meter (Agilent 3458A) to read the actual output voltage value. The whole

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process is repeated 5 times. Save the data of the original set voltage value—the actual voltage value, and perform curve fitting as shown in Fig 7.

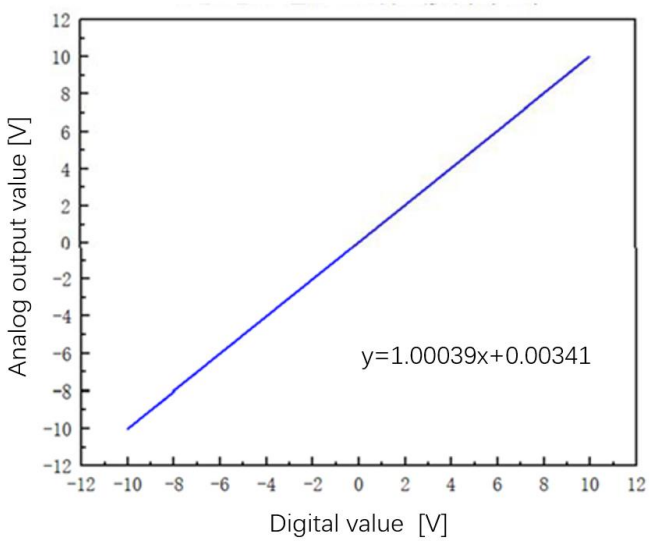

Fig 7 Linear fitting of output voltage

2）Short time fluctuations

Set different voltage output in the program, wait for 0.5s after setting the voltage value each time, and then read the actual output voltage value with an 8.5-digit digital multi-meter (Agilent 3458A), continuously measure 100 s, and count the peak-to-peak voltage jitter. The whole process is repeated 5 times.

Table 1. *Output voltage fluctuations under different voltage*

Vout/V	-10	-7.5	-5	-2.5	0	2.5	5	7.5	10
Fluctuations /μV	45.8	36.8	26.6	13.3	1.4	11.3	32.7	28.1	39.2

The voltage output range of this system is -10V~10V. For 18-bit system, 1 LSB is 76μV, and the maximum voltage jitter does not exceed 50μV in the full voltage range.

3) Uniformity between two channels

As shown in Fig.8, the two channels have the same set voltage of - 5.5V and -1.0V respectively, and read the actual output voltage value with an 8.5-digit digital multi-meter (Agilent 3458A)，continuously measure for a long time.

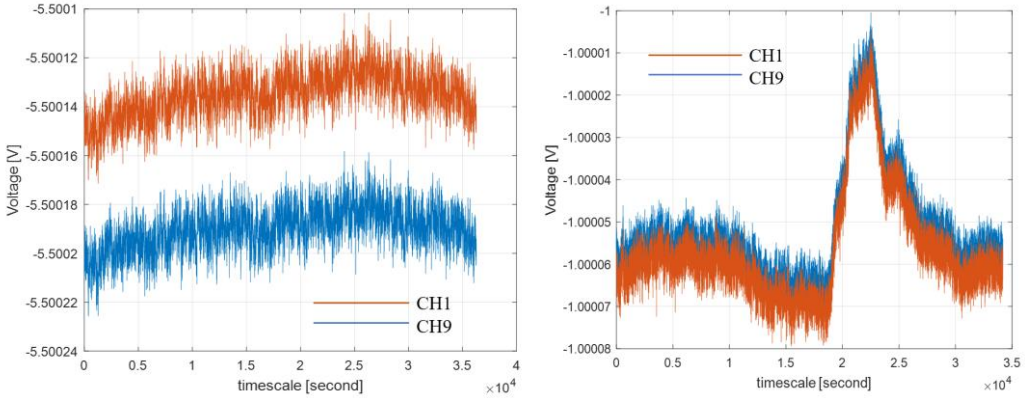

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Fig.8 the uniformity between different channels

4) Step response

As shown in Fig.9， The step is set from -5V to +5V. According to the test results of the oscilloscope, the 10V step has a settling time of about 2.4~2.7us.

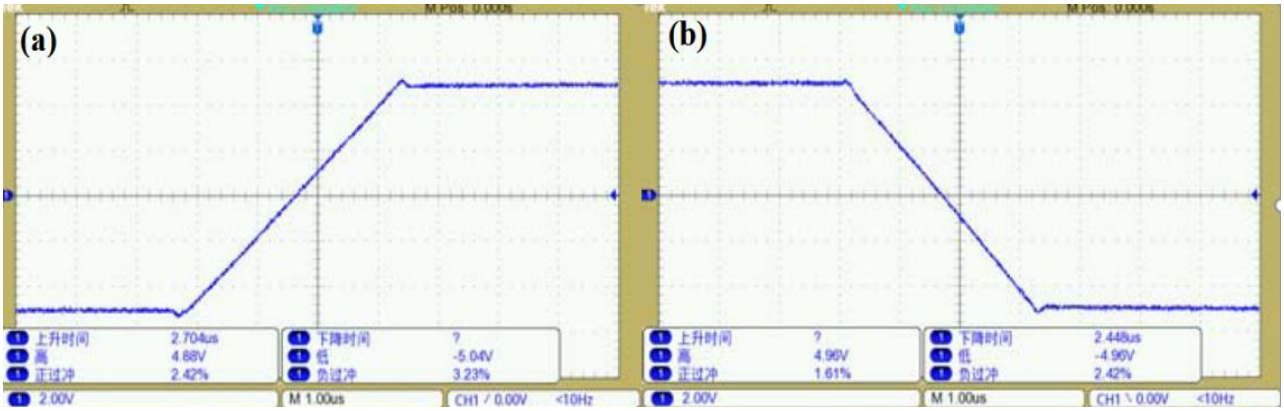

Fig 9 (a)-5V~+5V step response (b)+5V~-5V step response

5）Long-term stability

Turn on the output of 16 test channels at the same time and set their voltage output to 10 V at the same time, test the voltage value of random channels among them, read it every 10s, and the test duration is 24 hours.

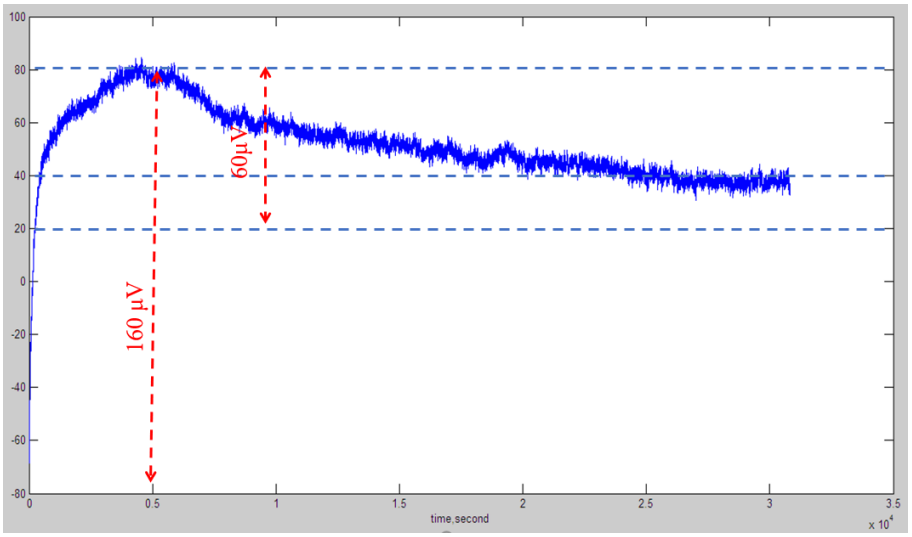

Fig. 10 the output voltage stability test

The output stability of the system was show in the Fig.10. After starting up and running for about 2 hours, the internal temperature of the instrument gradually rises, and the output voltage will drift by 160μV, and then the internal environment of the instrument gradually stabilizes. When multiple channels work at the same time, the system has excellent long-term stability of voltage output and maximum fluctuation. The range is less than 20 μV.

Conclusion:

Multi-channel bias voltage source is a typical technology with high resolution and low noise circuit design, involving resolution, noise, accuracy, linearity, temperature, channel consistency, long-term stability, low complexity and other aspects. This paper focuses on these problems closely, and achieves 4ppm conversion accuracy; Through scientific exploration, a series of low noise circuit design problems such as power supply, grounding processing and signal isolation are solved; Through closed-loop measurement and digital correction, accurate voltage output is obtained; The problem of capacitive load and linearity is solved by two-stage OPA output; Through careful heat dissipation, the whole machine controls the temperature change on the one hand; On the other hand, the temperature drift of components is very low, which minimizes the temperature drift coefficient of the system and improves the working temperature range through temperature compensation; Through careful structure design of the whole machine, the complexity of the system is reduced, and the humanized man-machine interface is realized. The results show that it is one effective and feasible topology for the high precision voltage bias source in Qdots device application.

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