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Article

A Five-Level Converter in a Three-Level Mode for Common-Mode Leakage Current Suppression in PV-Generation Systems

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Abstract: Power generation systems based on renewable energy sources are finding ever-widening applications and many researchers work on this problem. Many papers address the problem of transformerless structures, but few of them are aimed at conducting research on structures with multilevel converter topologies. In this paper a grid-tied transformerless PV-generation system based on a multilevel converter is discussed. There are common-mode leakage currents which act as a parasitic factor. It is also known that common-mode voltage is the main cause of the common-mode leakage current in grid-tied PV-generation systems. This paper considers the space vector pulse-width modulation (PWM) technique which is used to suppress or reduce common-mode leakage current. The proposed engineering solutions for a generation system based on the multilevel converter controlled with a pulse-width modulation technique are verified by experiment.

Keywords: converter; leakage current; common-mode; renewable

1. Introduction

Today renewable energy sources (RES) are widespread and are becoming more attractive compared with systems based on fossil fuels such as oil, coal and gas [1]. RES have some advantages such as harmless emissions into the environment, close location to the consumer and others. The use of RES technologies leads to saving conventional fossil fuels. RES technologies can be primarily attributed to photovoltaic energy production [2-3]. Power electronic systems (PES) are the key state-of-the-art development in these RES technologies. The most important part of PES is a power semiconductor converter. Increasing the installed power of a PV power generation system (PVPGS) leads to increasing power of a semiconductor converter that is an integral part of the system [2-10]. For these reasons, multilevel semiconductor converters are typically used. A PV power generation system usually has a transformer in its structure for voltage level conversion and galvanic isolation from the grid. But the use of a transformer makes the system less efficient and increases the weight and size parameters. References [11-13] include some research papers on transformerless PVPGSs. The elimination of the transformer leads to the following negative phenomena. The main negative phenomenon is the presence of the-so called common-mode leakage current (CMLC). This current is a flow through the loops made by the parasitic elements (capacitances and inductances) [14]. The leakage current worsens the power quality, creates emergency situations, for example faults of thin-film PV panels and, as a result, a system failure. Besides it creates unsafe operating conditions for the personnel [15].

There are various methods of CMLC suppression: schematic and algorithmic or both. There are: different types of converters and their modifications which allow suppressing CMLC for schematic methods [16]. And there are various pulse-width modulation (PWM) techniques and predictive control systems for algorithmic methods [15], [17]. Predictive control systems do not allow the elimination of CLMC in transformerless grid-tied PV-

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generation systems. Predictive control systems only reduce leakage currents and in some cases deteriorate converter efficiency.

The authors developed a possible solution to eliminate leakage currents in a single-phase system based on a multilevel power semiconductor converter. A schematic and algorithmic solution was reviewed in [18–19].

The paper is organized as follows. Section II gives a brief description of the leakage current in PV PVPGS. Section III presents the developed converter for PV PVPGS with the reduction of the leakage current. Section IV presents the results of experimental research.

2. Leakage current

The structure of the considered single-phase grid-tied transformerless PVPGS with the considered parasitic capacitances is illustrated in Fig. 1. The elements of PVPGS are discussed in [14], [18]. PVPGS consists of several parts. The most important of them are PV modules and the voltage source converter (VSC).

The voltage source converter has two components of output voltage v_{dif} and v_{cm} - terminals 1 and 2, Fig.1. v_{dif} is a differential mode voltage,. v_{cm} is a common mode voltage. VSC voltage components v_{dif}^{*} and v_{cm} are the main cause of the CMLC presence. The v_{dif}^{*} component is eliminated by equalizing the parameters of output filter inductances.

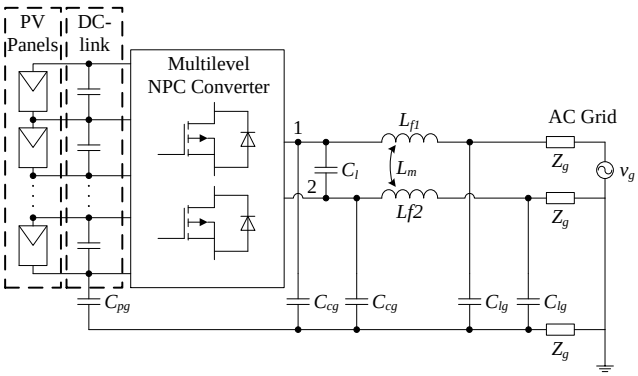

Figure 1. Structure of the PVPGS with parasitic components.

Therefore, the v_{cm} component produces CMLC i_{cm}. The circuit diagram in Fig.1 can be simplified as shown in [18–19].

The common-mode leakage current in this circuit diagram is found by Kirchhoff''s voltage law as:

$$\sum_{n=0}^{\infty}\dot{I}_{\mathrm{CMLC}(n)}=\sum_{n=0}^{\infty}\frac{V_{cm(n)}}{\frac{1}{j\omega_n C_{pg}}+X_{L_{12}}+\frac{Z_p}{j\omega_n 2C_{lg}Z_p+1}}, \quad (1)$$

where $V_{cm(n)}$ is the common mode voltage of the n-th harmonic, $\omega_n=2\pi fn$ is the angular frequency of the n-th harmonic, f is the frequency of PWM, C_{pg} is the equivalent parasitic capacitance (EPC) of the PV module. An average value of EPC is estimated as100 nF per 1 kW of the power of the PV module, Z_p is the parasitic loop impedance; C_{lg} is the capacitance of the EMC filter relative to the ground line, $X_{L_{12}}=j\omega_n\frac{L_1L_2}{L_1+L_2}$ is the equivalent reactance of the output inductors.

As you can see in the equation (1), the common-mode leakage current has a polyharmonic character with different frequency content. It is defined by the spectral composition of the common-mode voltage. It is obvious that the common-mode voltage acquires the character of a constant signal, and takes into account the capacitive character of the

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common-mode leakage current that will provide a CMLC value equal to zero. This condition is achieved when the current frequency is equal to zero. The idea of synthesizing a single-phase multilevel semiconductor converter to eliminate the CMLC suppression will be presented based on this condition.

Another way of common-mode leakage current suppression is achieved when $Z_p = \infty$, i.e. when breaking the leakage loop. This parameter depends on the type of grounding of the circuit and in some cases it can be neglected. The emergence of this parasitic factor is caused by the PVPGS area, soil specific resistance, etc. It becomes clear that an elegant way to provide PVPGS operation and suppress CMLC is to achieve a zero frequency of v_{cm}.

The magnitude of voltage pulsation is estimated by the expression $\Delta v_{cm} = \frac{V_{dc}}{m \cdot (N-1)}$, where V_{dc} the DC-link voltage, m is number of phase legs and N is the number of voltage levels. Here are the following assumptions:

a) The common-mode voltage is calculated as a mean value of all phase to ground inverter voltages.
b) The voltage level of v_{cm} is defined by a voltage step of the multilevel semiconductor VSI, that is $\frac{V_{dc}}{N-1}$.

3. A single–phase multilevel converter with current cancelation

Low-power systems (3-5kW) usually work in single-phase AC grids. Thus, PVPGS has a single-phase power converter. Multilevel converters are often used in different power generation systems. A three-level NPC converter is one of the widely spread types of single-phase multilevel voltage source converters (Fig. 2). In these multilevel VSCs several types of PWM are usually used, namely space vector (SV) and carrier-based or hysteresis PWM. The best way of using the space vector PWM for common-mode leakage current reduction is proposed in [18].

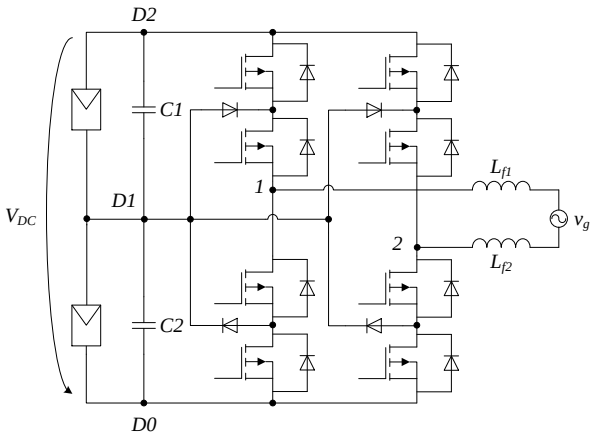

Figure 2. Single phase NPC converter.

In this topology the differential voltage v_{dif} can take five voltage levels depending on the switching states of the multilevel semiconductor converter: $v_{dif} = \left\{ V_{DC}; \frac{V_{DC}}{2}; 0; -\frac{V_{DC}}{2}; V_{DC} \right\}$. Common-mode voltage takes the following values: $v_{cm} = \left\{ 0; \frac{V_{DC}}{4}; \frac{V_{DC}}{2}; \frac{3V_{DC}}{4}; V_{DC} \right\}$.

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In order to eliminate CMLC common-mode voltage must be maintained at any value of v_{cm} proposed previously. In the reference paper [16] a three-level NPC converter operates in a two-level mode.

To work in the N level output voltage mode a $(2N-1)$ level converter is needed.

It is clear that a five-level converter is needed for three-level output voltage generation with CLMC suppression. There are two types of NPC converters that allow CLMC suppression and three-level output voltage generation [18–19]. The diagram of SV PWM state switching for both converters is shown in Fig. 3. The five-level NPC converter is shown in Fig. 4. A modified five-level NPC converter proposed in [18] is shown in Fig. 5.

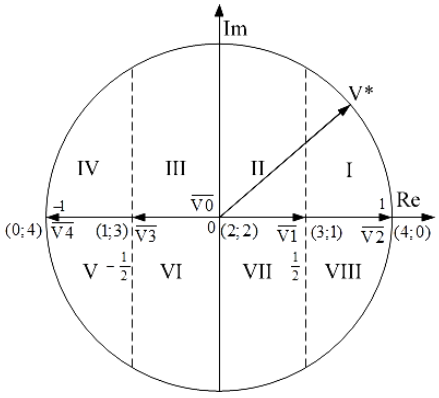

Figure 3. Single-phase converter switching in the state diagram.

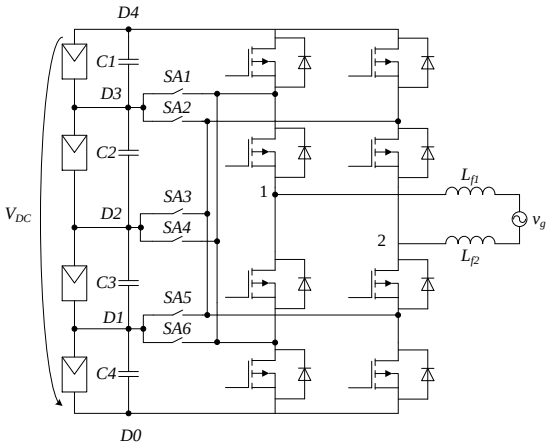

Figure 4. A modified single-phase converter.

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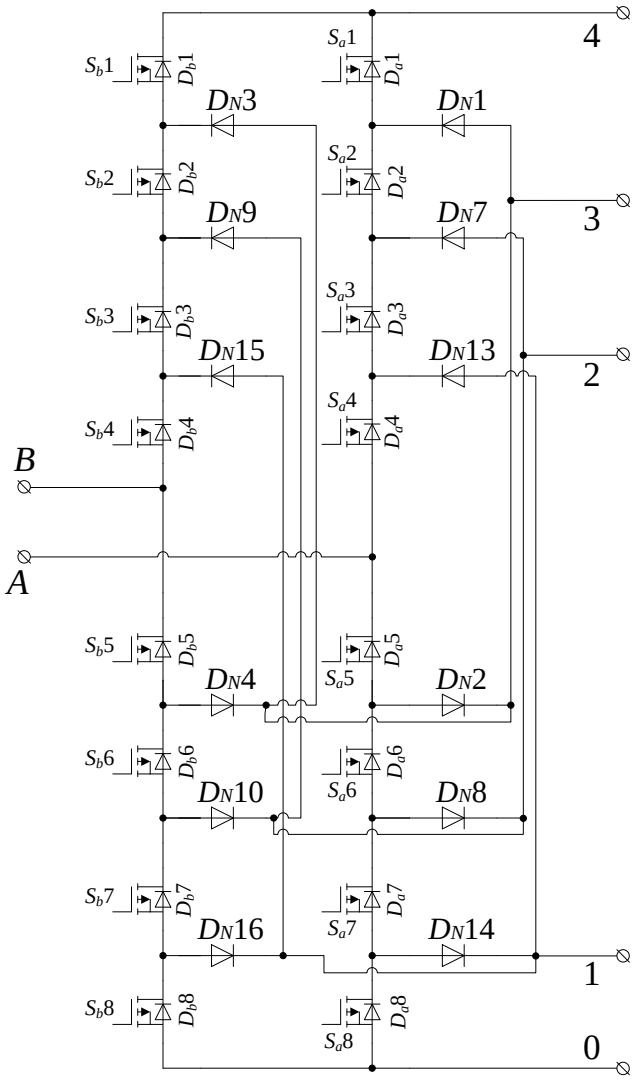

Figure 5. A five-level NPC converter.

Although the modified NPC converter has a five-level topology it still operates in the three-level mode to maintain the leakage current suppression.

In the case of the DC-link unbalance the choppers providing the voltage balancing must be implemented.

The efficiency of MOSFET transistors and SV PWM of the same switching pattern was calculated in percent for both converters. The results of efficiency calculation for the modified single-phase five-level semiconductor converter and for a single-phase five-level semiconductor converter were obtained for them to operate in the CMLC suppression mode (Fig. 6) for different A values. A is the ratio between grid frequency and PWM frequency. As can be seen in Fig. 6, the modified converter has an advantage in efficiency up to A more than 2000.

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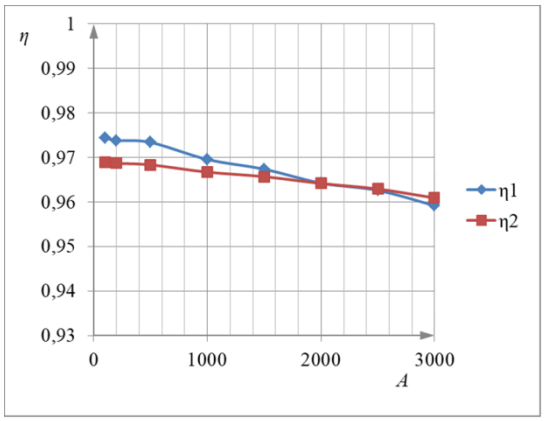

Figure 6. A five-level NPC converter (η1 is the proposed converter, η2 is a standard five-level converter).

This is explained by the fact that the modified semiconductor converter has fewer static power losses than the converter (Fig. 6), and dynamic power losses are higher, up to a given frequency multiplicity. Static power losses prevail over dynamic power losses up to the range of 2000. Thus, the range up to the frequency multiplicity is the range of energy-efficient operation of the modified single-phase semiconductor converter.

4. Experiment results

Figure 7 presents an experimental model of a single–phase PVPGS with the function of reducing the leakage current presented in Fig. 9. The control system was implemented on the Discovery kit with MCU STM32F407VG. A galvanic isolated power system for drive power was made on the International Rectifier IR2153. MOSFET IRF740S was used as power transistors.

The experimental model has the following parameters:

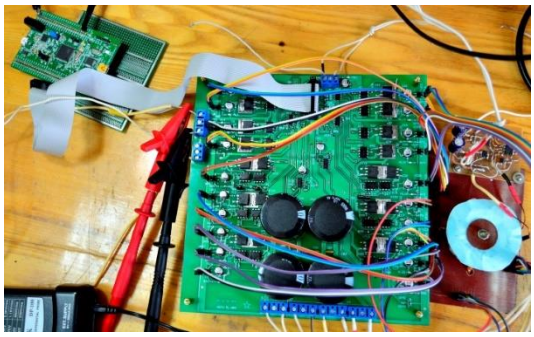

Figure 7. An experimental model.

Figures 8 and 9 represent experimental results of PVPGS operation with the modified converter.

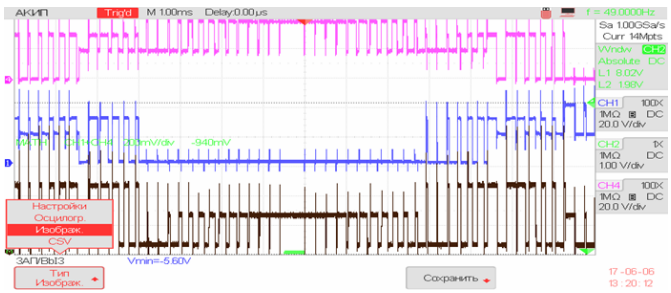

Figure 8. Experimental results. Leakage current A no-suppression mode. Top to bottom v_1, v_2, v_{cm}.

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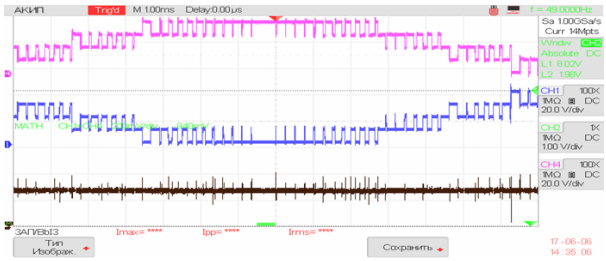

Figure 9. Experimental results. A leakage current suppression mode. Top to bottom v_1, v_2, v_{cm}..

As shown earlier, the main common-mode current source is a common-mode voltage source. Fig. 8 shows the voltage oscillograms of a five-level inverter, where you can see that there is an alternating common-mode voltage. As seen from Fig. 9, the common-mode voltage has the character of a constant signal. This was achieved through the use of the proposed converter and control algorithm.

- Rated power: 1.2kW;
- DC-link voltage: 400V;
- Filter inductances: L_{f1}=65uH;
- Filter inductances: L_{f2}=72uH;
- PV leakage capacitance: $C_{pg} = 240\text{nF}$;
- Parasitic loop impedance: $Z_p = 100\Omega$;
- Capacitors $C1 = C2 = C3 = C4 = 4700uF$;

A new topology of a five-level semiconductor converter was synthesized and a vector pulse-width modulation algorithm to control this converter was proposed. The experimental results confirmed the possibility of forming a common-mode voltage having a character of a constant signal and, consequently, eliminating a common-mode leakage current. This in turn gives reasons to believe that the implementation of autonomous power generation systems using the proposed type of the semiconductor converter will improve the functional and operational characteristics of PVPGS, such as electrical safety and reliability.

5. Conclusions

The structure of the PVPGS generation system which includes a multilevel semiconductor converter proposed by the authors, as well as the control algorithm was tested. This is the main contribution of the authors. A vector-based PWM strategy to be used in this type of multi-level semiconductor converters was also developed, which allows the formation of the common-mode voltage having the character of a constant signal. In addition, a fundamental possibility of eliminating the transformer from the structure of the generating system while maintaining the quality of the output current and voltage was demonstrated. Experimental research aimed at verifying these results was also carried out.

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Conflicts of Interest: The authors declare no conflict of interest.

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