Article

DC-link Current Harmonic Mitigation via Phase-shifting of Carrier Waves in Paralleled Inverter Systems

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Abstract: DC-connected parallel inverter systems are gaining popularity in industrial applications. However, such parallel systems generate excess current ripple (harmonics) at the DC-link due to harmonic interactions between the inverters in addition to the harmonics from the PWM switching. These DC-link harmonics cause the failure of fragile components such as DC-link capacitors. This paper proposes an interleaving scheme to minimize the current harmonics induced in the DC-link of such a system. The results show that when the carrier waves of the two inverters are phase-shifted by 90 angle, the maximum high-frequency harmonic ripple cancellation occurs, which reduces the overall RMS value of the DC-capacitor current.The outcome of this proposed solution is a cost-effective DC-harmonics mitigating strategy for the industrial designers to practically configuring multi-inverter systems, even when most of the drives are not operating at rated power levels. Experimental and simulation results presented in this paper verify the effectiveness of the proposed carrier-based phase-shifting scheme for two different configurations of common DC connected multi-converter systems.

Keywords: DC-link current; harmonic mitigation; voltage source inverters; multi-converter systems; carrier wave interleaving scheme; DC-grid; phase-shifting; capacitor current ripple; unipolar sinusoidal pulse width modulation

1. Introduction

To improve the power delivering capacity and reliability of power electronic converters, many researchers have directed towards the parallel connection of these converter units. Indeed, parallel connection of converters have received increased attention in the past few years, due to several reasons; increased reliability through reduced number of conversion stages, modularity, ease of maintenance through the operation of identical units, scalable designs, and reduced size of the overall system [1].More significantly, such systems enable the integration of renewable energy sources and storage with the bulk electric grid[2]. Analytical and experimental verification of a scenario where multiple generators are connected in parallel and an interleaving scheme reduced the harmonics at the common point of connection is discussed in [3]. Also, it explains how the parallel connection of multiple lower power units is used as a solution to design high power converters with better flexibility and higher reliability. However, one drawback of this kind of parallel-connected systems [2–4] is that, due to the common AC point of connection, integration of renewable resources becomes difficult. Additionally, in the multi-converter systems explained in [1],[5–7] each inverter has its own individual rectifier system and shared the common DC-link, an example of which is shown in Figure 1a. Hence the total number of rectifiers needed in the whole system increases, eventually increasing the overall size and reducing reliability.

Even though in the industrial applications DC-connected parallel inverter systems are gaining popularity, such parallel systems generate excess current ripple (harmonics) at the DC-link due to the harmonic interactions between the inverters in addition to the harmonics from the pulse width modulation switching. This harmonic interaction at the

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DC-link causes the failure of fragile components such as DC-link capacitors [1,4]. This is of significant importance as the current ripple causes a decrease in the capacitor lifetime due to an increase in the internal temperature. Also, the power loss of the capacitor, which is a function of the current harmonic spectrum and its Equivalent Series Resistance (ESR) increases as the capacitor current increases [8]. Several studies show that 30% of the total failure root causes in the power electronic systems are due to capacitors failures [9], and hence they are considered as the most fragile components in a power electronic system [9–12]. In order to extend the lifetime of the DC-link capacitor, two possible solutions are considered. One practical solution in the market is to use higher capacitance and higher rated current capacitor at the DC-link, but the total volume, weight, and cost will significantly increase. Another way is to actively reduce the current stresses of the DC-link capacitor. This method is considered in this paper for a parallel-connected inverter system, which is more cost efficient and convenient to use due to no hardware change is needed. Because in a parallel system the DC-link current is generated by a summation of the current harmonics from the connected converter, the phase-shifted switching cycles lead to variations of the current ripple [5]. Thus, using an interleaving (i.e. phase-shifting) of the PWM carrier waves of inverters at an optimal angle is a possible solution to effectively reduce the total DC-current ripple at the DC-link.

A plethora of research has been conducted on interleaving the carrier waves of the parallel-connected PWM inverters to reduce the DC-link current harmonics [1–5], [7,13]. Lowering the DC-link harmonics reduces the power losses within the capacitor [14]. In a parallel-connected system, the phase-shifted switching cycles of the carrier waves can effectively reduce the current ripple as a result [7], the size and weight of passive components such as the DC-link capacitors, and EMI-filters can be reduced. A detailed study of a harmonic reduction technique using synchronized phase-shifted PWM voltage source inverter (VSI) units having individual DC-source has been provided in [1]. Alternately, [5] presents the effect of optimal phase-shift angle in reducing DC-current ripples under unequal DC-link voltage scenarios in two parallel three-phase grid-connected voltage-source inverters (VSIs) are presented. The effect of the size of the DC-link components and the grid configuration in three-phase multi-drive systems, similar to the topology shown in Figure 1a, on the resonant frequencies have been studied in [6]. In [7], analytical modeling of paralleled and interleaved 3-level neutral point clamped inverters using space vector modulation is discussed. It explains how interleaving helps to reduce both AC and DC-side harmonics and reduces the EMI harmonics in parallel-connected inverter systems.

As mentioned above, the existing methods for multi-converter systems, to the best of the authors' knowledge, have the following two limitations : Firstly, most of them considered common AC-grid connection for the parallel inverters, which limits the integrating with the DC-grid system. Secondly, there is no DC-link current harmonic elimination method proposed for multiple drive systems with a common DC-link in any of the pieces of literature so far. To address research gaps, this work presents a carrier phase-shifting strategy for two different configurations of common DC-connected multi-converter systems. The two key contributions of this paper are:

1. A family of common DC-link structure is proposed, where one topology is a multi-converter system with an individual DC-bank is shown in Figure 1b, and another topology is a multi-converter system with a common DC-bank is shown in Figure 1c. Both these proposed topologies have a centralized rectifier, which provides the flexibility for plug-and-play of the number of inverters connected to DC-grid in parallel-connected systems. Notably, this kind of operation allows the easy integration of DC sources at the common DC link in a system, compared to the conventional parallel-connected system having a common AC point of connection illustrated in Figure 1a. Also, using the centralized rectifier reduces the number of converters being used in a parallel-connected system. Thus, reducing the overall size and increasing reliability as shown in Figures 1b–1c compared to the conventional system shown in Figure 1a.

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2. A modulation method for mitigation of DC-link capacitor current harmonics in parallel connected inverters system is proposed via phase-shifting of the carrier waves. The optimally phase-shifted switching cycles lead to variations of the output current ripples, which when summed together at common DC results in the minimization of ripples at DC-link current. Thereby, the switching frequency harmonics reduce, which reduces the overall DC-capacitor RMS current. Hence reducing the overall stress (electro-thermal stress, and hot-spot temperature) at the DC-link, leading to an improved lifetime of the DC-link capacitor.

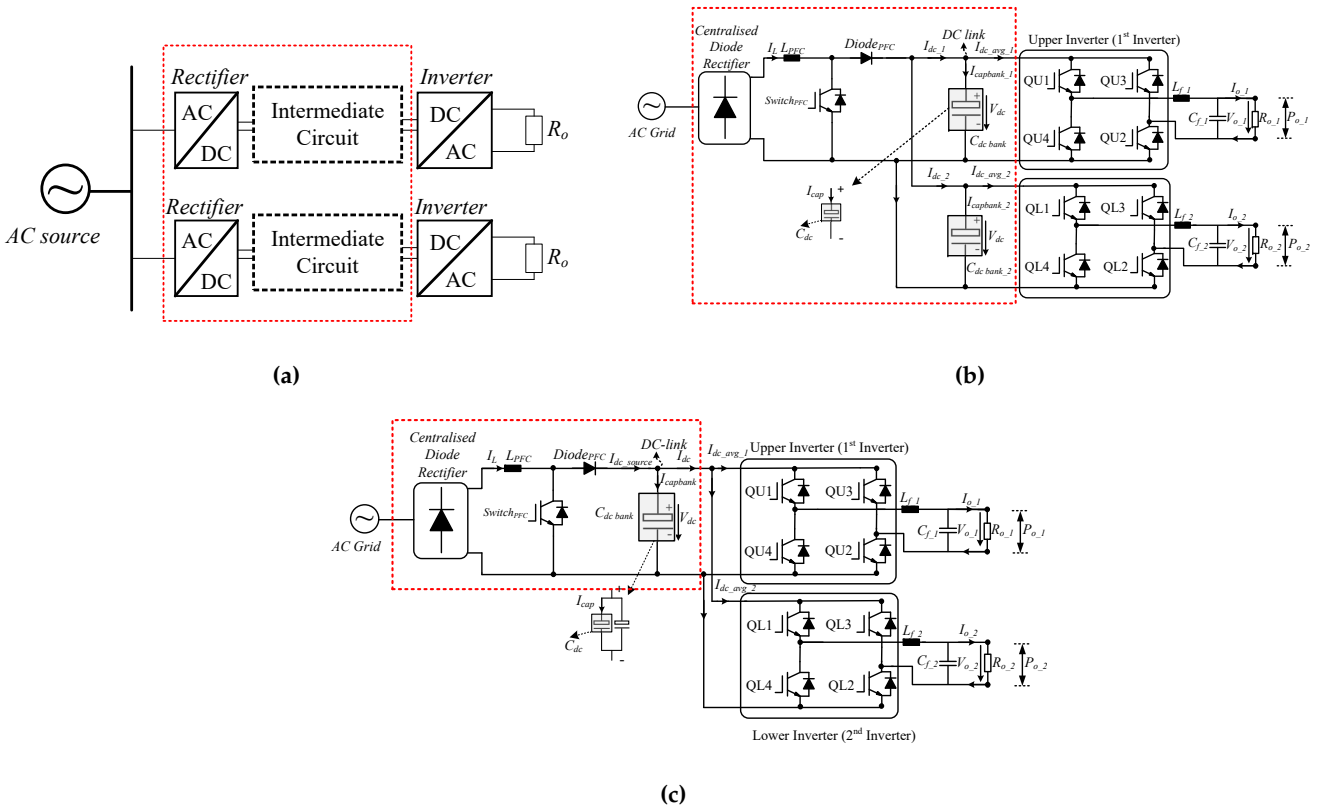

Figure 1. Block diagram of: (**a**) the conventional parallel-connected system, (**b**) a multi-converter system with individual DC-bank having a centralized rectifier, (**c**) a multi-converter system with common DC-bank having a centralized rectifier

This paper is structured as follows. The overall system description is presented in Section 2. Section 3 discusses the harmonic analysis of the capacitor current based on the conventional system, and Section 4 explains the proposed system. The lifetime estimation is discussed in Section 5. The effectiveness of the developed analysis is demonstrated by the results and discussions in Section 6. Finally, conclusions are drawn in Section 7.

2. Proposed System Description

In this study, a diode rectifier with boost power factor corrector (PFC), and DC-filter (consisting of a DC-choke and a large electrolytic DC-link capacitor) is implemented due to its simplicity, cost-effectiveness, and reliability advantages [6]. Aluminium electrolytic capacitors (El-caps) are used as DC-link capacitors, due to their advantage of providing a high capacitance per unit volume at low costs compared to other types of capacitors [15]. The boost PFC employed improves the power factor, as well as facilitates power supply hold-up, which ensures that the system can maintain the DC voltage until the backup power supply is connected, in case of a power supply disruption [16,17].

The proposed topologies in this paper, shown in Figure 2 (hereby referred to as the multi-converter system with individual DC-bank), and Figure 3 (hereby referred to as the

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multi-converter system with common DC-bank) have a centralized rectifier and a common DC point to connect the parallel inverters. More importantly, a DC-link current harmonics mitigation strategy is introduced via phase-shifting of the inverter carrier waves in these two topologies. Using a centralized rectifier eliminates the need for each inverter to have its rectifier as shown in Figure 1a. For the proposed multi-converter system with individual DC-bank, each of the parallel-connected inverters has its individual capacitor bank to limit the DC-link voltage fluctuation. This kind of connection provides more flexibility to the industrial designers to plug and play with the number of inverters connected to DC-grid in parallel-connected systems. On the other hand, the proposed multi-converter system with a common DC-bank has a common capacitor bank consisting of individual capacitors, which connected in parallel to ensure the equal distribution of the ripple current (I_{cap}) flowing through the the DC-link capacitor bank ($C_{DC-bank}$). The total ripple current flowing through ($C_{DC-bank}$) is denoted by ($I_{capbank}$), and through a single capacitor is (I_{cap}).

The four switches Q_{x1}, Q_{x2},Q_{x3},Q_{x4} of the VSI units shown in both Figures 2–3 are controlled using the unipolar sinusoidal PWM (SPWM) technique, explained in detail in [18,19]. The specifications of the inverter system and output filter (designed according to [19]) are given in Table 1 and Table 2. Both the topologies (in Figures 2–3) have the same parameters and loading conditions. The rated output voltage of 230 V (RMS value) for each inverter unit is maintained by its own specific Proportional-Resonant (PR) controller, which is designed according to [20,21]. The control algorithm for the inverter is shown in Figure 4a, and for the boost, PFC is shown in Figure 4b. The parameters for the controllers have the same value as both VSI units are synchronized and controlled using unipolar SPWM to get the same $V_{o-rated}$. The parameters for boost PFC are shown in Table 3, designed according to [22,23]. The data for the DC-link capacitor is from the datasheet [24] and shown in Table 4.

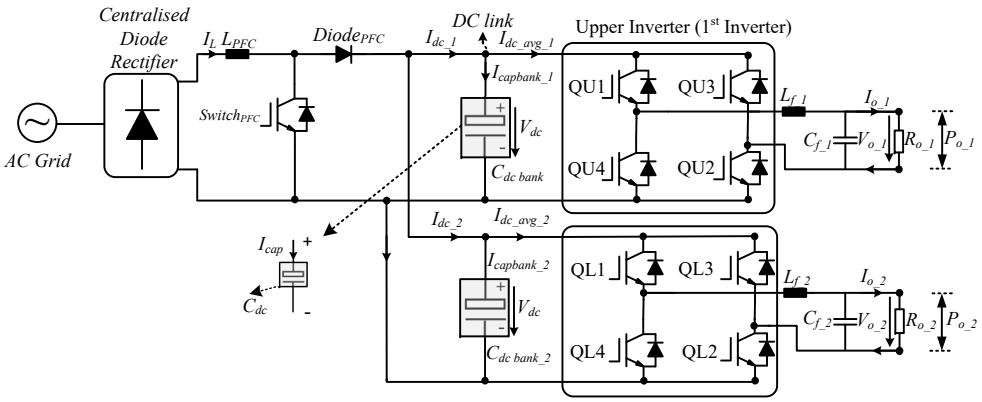

Figure 2. Block diagram of the multi-converter system with individual DC-bank.

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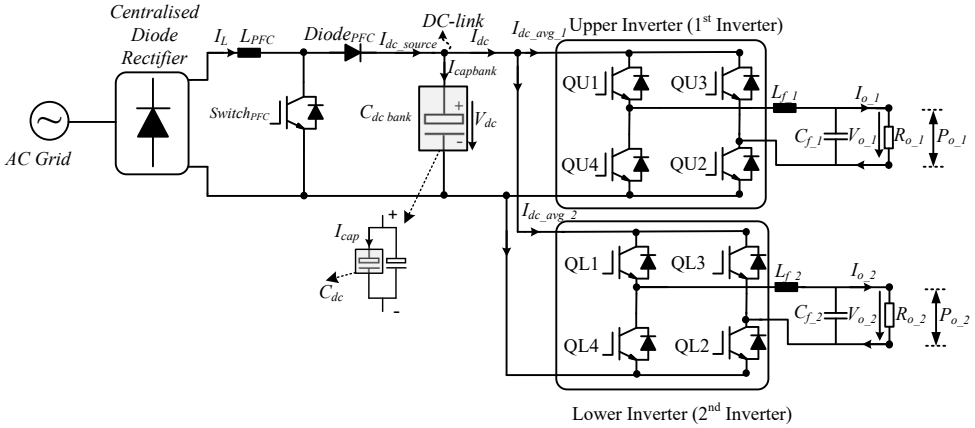

Figure 3. Block diagram of the multi-converter system with common DC-bank.

Table 1. Specifications of the output load.

Parameter	Symbol	Value
Rated power (kW)	P_o	2.5
Load (Ω)	R_L	20
Rated RMS load voltage (V)	$V_{sine-ref}$	230
Load frequency (Hz)	f_o	50
Rated DC-link voltage (V)	V_{dc-ref}	400
Switching frequency (kHz)	f_{sw}	20
Modulation amplitude index	M_A	0.8

Table 2. Specifications of the inverter output filter.

Parameter	Symbol	Value
Inductor filter ripple current limit	I_{f_ripple}	20%
Inductor (H)	L_f	2×10^{-3}
Filter cutoff frequency (kHz)	f_{cutoff} ($f_{cutoff}<f_{sw}/10$)	2
Filter capacitor (F)	C_f	6×10^{-6}

Table 3. Specifications of the boost PFC.

Parameter	Symbol	Value
Power rating (kW)	P_{PFC}	2.5
RMS AC−input voltage (V)	V_S	230
RMS AC−input current (A)	I_S	10.58
PFC Switching frequency (kHz)	f_{PFC}	20
PFC inductor current ripple	I_{PFC_ripple}	30%
PFC inductor current maximum (A)	I_{PFC}	16
PFC inductor minimum (H)	L_{PFC}	3×10^{-3}
Ripple output peak to peak (p−p) voltage (V)	V_{PFC_p-p}	20
Hold-up time (s)	$t_{hold}(=1/f_o)$	2×10^{-3}
PFC capacitor minimum (F)	C_{PFC}	3.3×10^{-3}

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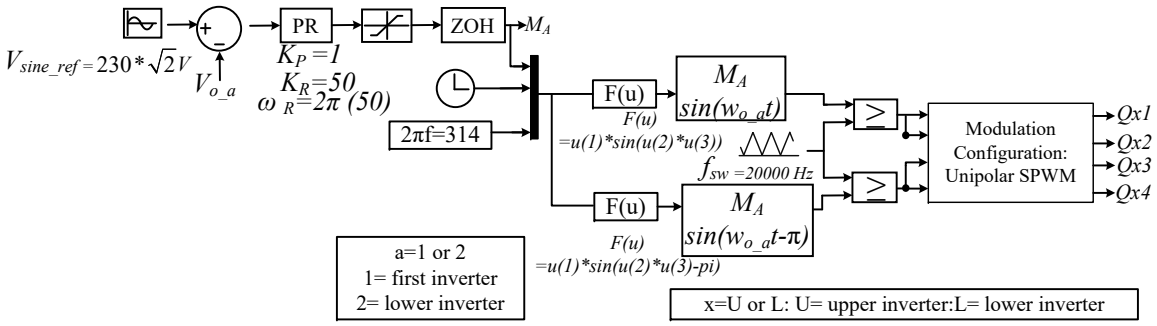
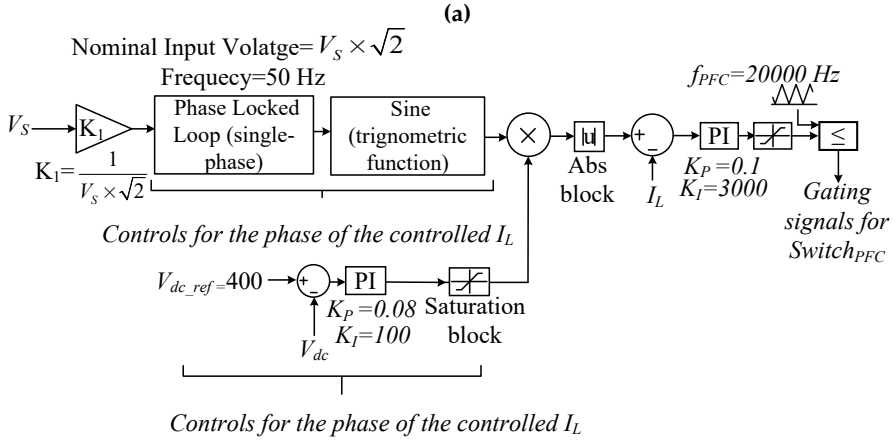
Table 4. Specifications of the DC-capacitor (KEMET−AlS8(1)(2)392NF500).

Parameter	Symbol	Value
Single capacitance (μF)	C_{dc}	3900
Equivalent series resistance $(m\Omega)$	ESR	61 (100Hz), 46(10kHz)
Thermal resistance (°C/W)	R_{th}	3.8
Rated lifetime (hours)	L_o	9000 (at T_{rated} & I_{rated})
Rated upper category temperature(°C)	T_{rated}	105
Rated ripple current (A)	I_{rated}	12.2(100Hz), 19.0(10kHz)
Rated voltage (V)	V_{rated}	500
Operating temperature (°C)	T_a	45



(a)



(b)

Figure 4. Control algorithm: (**a**) inverter, (**b**) boost PFC−where nominal input voltage of the phase lock loop is given as $V_S \times \sqrt{2}$. (K_P−Proportional parameter, K_I−Integral parameter, K_R−Resonant coefficient, ω_R−Resonant frequency, $K_1 = 1/(V_S \times \sqrt{2})$)

3. Conventional method without any phase-shift

In this section, the DC-current harmonics generated by the PWM switching of each of the parallel-connected inverters are analyzed. Let us take the system with two parallel inverters shown in Figure 3 for analysis. For simplicity, it is assumed that both inverters have the same loading conditions, hence, draw the same output current. Conventionally, the two output current ripples and carrier waves (Triangle Wave 1 for upper inverter, and Triangle Wave 2 for lower inverter) appear as seen in Figure 5. These output current ripples sum up to produce higher ripples in the DC-current. These ripples (harmonics) degrades the efficiency of the whole system as well as decreases the lifetime of the DC-link capacitors [3]. As the number of inverters increases, more DC-current ripples would be generated

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by a summation of the current harmonics from the connected converters. To solve the aforementioned issue, it is important to reduce the DC-current harmonics to improve the reliability and lifetime of the DC-link capacitors at optimized cost.

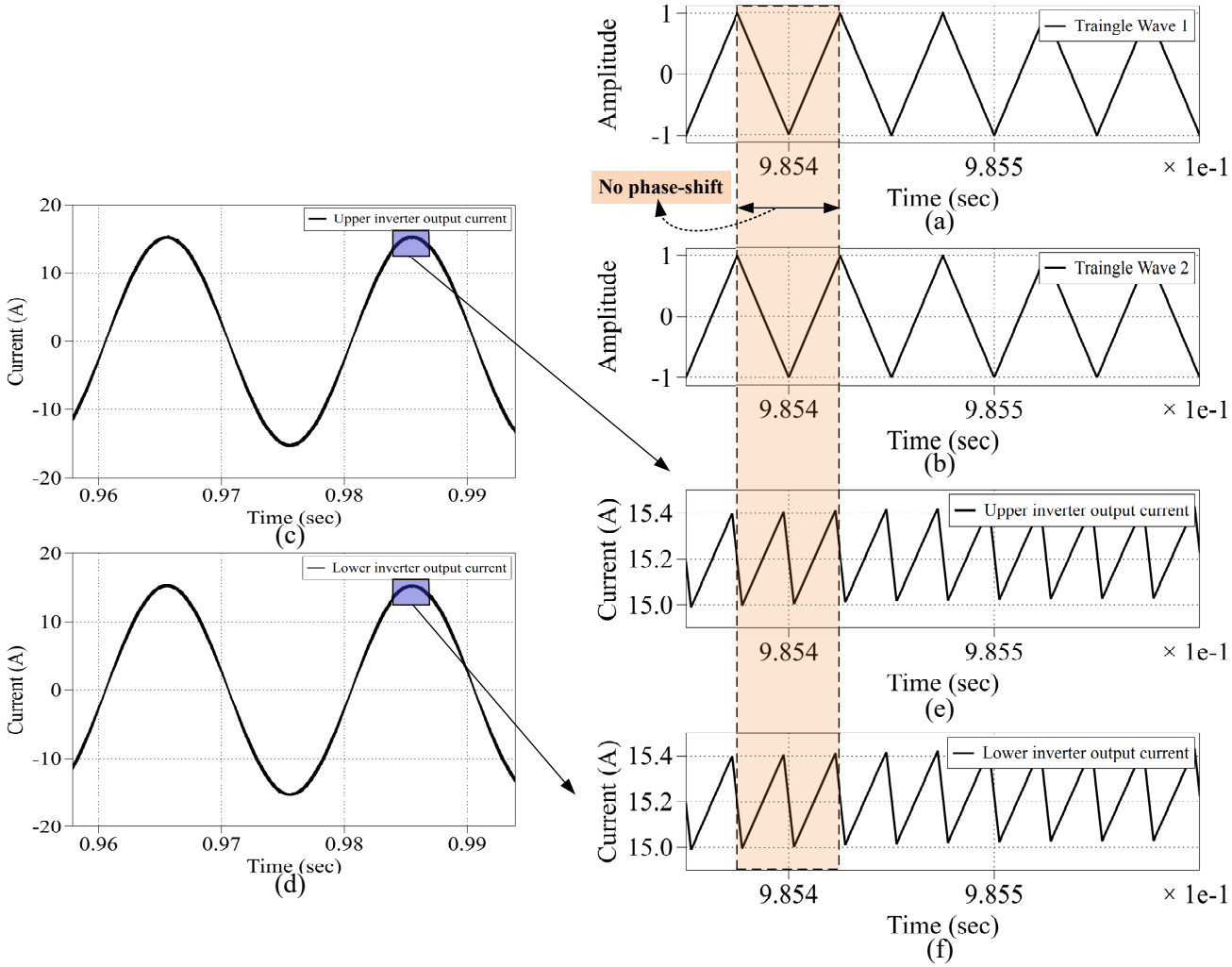

Figure 5. Parallel-connected system waves using the conventional method : (**a**) upper inverter carrier wave, (**b**) lower inverter carrier wave, (**c**) upper inverter output current wave, (**d**) lower inverter output current wave, (**e**) output current ripples of upper inverter, and (**f**) output current ripples of the lower inverter.

4. Proposed method with an optimal carrier phase-shift

For the multi-converter systems shown in Figures 2–3, one of the effective methods to reduce the DC-current ripple is interleaving the carrier signals of the parallel converters. To apply the proposed DC-link harmonic mitigation method, it is necessary to first find the optimal phase-shift angle ($\theta_{fsw\_optimal}$) for the carrier signal which provides maximum capacitor current ripple cancellation (i.e. at the main switching frequency harmonic component which appears at $f_{sw_harmonic} = 40$kHz). The optimally phase-shifted switching cycles lead to variations of the output current ripples, which when summed together results in the minimization of ripples at DC-link current. This is analytically explained as per the Equations (1)–(9) provided below for inverters having unipolar PWM [25]. In this paper, the phase shift is applied to the lower inverter carrier signal. Hence the phase angle of the upper inverter carrier signal, $\theta_{fsw1} = 0°$, whereas phase angle of lower inverter carrier signal θ_{fsw2}=$\theta_{fsw\_optimal}$.

$$V_{o\_1} = M_A V_{dc} \sin(\omega_{o1} t + \theta_{o1}) + \frac{4V_{dc}}{\pi} \sum_{m=2,4,6\ldots}^{\infty} \sum_{n=\pm1,\pm3,\pm5\ldots}^{\pm\infty} \frac{J_n(mM_A\pi/2)}{m} cos(\frac{m\pi}{2}) \sin(n(\omega_{o1} t + \theta_{o1}) + m(\omega_{c1} t + \theta_{fsw1})) \quad (1)$$

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$$I_{o\_1} = I_{o\_peak\_1}\sin(\omega_{o1}t + \theta_{o1}) \tag{2}$$

$$I_{dc\_1} = I_{o\_1} \times \underbrace{(\frac{V_{o\_1}}{V_{dc}})}_{SwitchingFunction} \tag{3}$$

$$I_{capbank\_1} = I_{dc\_1} - I_{dc\_avg\_1} \tag{4}$$

$$V_{o\_2} = M_A V_{dc}\sin(\omega_{o2}t + \theta_{o2}) + \frac{4V_{dc}}{\pi}\sum_{m=2,4,6\ldots}^{\infty}\sum_{n=\pm1,\pm3,\pm5\ldots}^{\pm\infty}\frac{J_n(mM_A\pi/2)}{m}cos(\frac{m\pi}{2})\sin(n(\omega_{o2}t+\theta_{o2}) + m(\omega_{c2}t + \theta_{fsw2})) \tag{5}$$

$$I_{o\_2} = I_{o\_peak\_2}\sin(\omega_{o2}t + \theta_{o2}) \tag{6}$$

$$I_{dc\_2} = I_{o\_2} \times \underbrace{(\frac{V_{o\_2}}{V_{dc}})}_{SwitchingFunction} \tag{7}$$

$$I_{capbank\_2} = I_{dc\_2} - I_{dc\_avg\_2} \tag{8}$$

$$I_{capbank\_2} = I_{capbank\_1} + I_{capbank\_2} \tag{9}$$

In the above equations, $V_{o\_1}, V_{o\_2}, I_{o\_1}, I_{o\_2}$, present upper and lower inverter output voltages and output currents. The peak value of output currents of upper and lower inverters is $I_{o\_peak\_1}, I_{o\_peak_2}$. The DC-current source and its average value of upper and lower inverter are represented by $I_{dc\_1}, I_{dc\_2}, I_{dc\_avg\_1}, I_{dc\_avg\_2}$. The capacitor bank current for upper and lower inverter are denoted by $I_{capbank\_1}, I_{capbank\_2}$. Finally, the fundamental frequency and switching frequency of upper inverter are symbolised by ω_{o1}, ω_{c1}, and that of lower inverter is designated by ω_{o2}, ω_{c2}. Equations (1)–(4) describe the upper inverter, while Equations (5)–(8) is for the lower inverter. Equation (3) and Equation (7) are derived based of the power balance equation of the inverter, which states that the input power on the DC-side ($P_{dc} = V_{dc} \times I_{dc}$) of the converter relates to the output apparent power on the AC-side($P_{ac} = V_o \times I_o$).

The method used in this paper is as follows: firstly, various phase-shift angles are applied for carrier signal of the lower inverter (θ_{fsw_2}), and the multi-converter system with individual DC bank (shown in Figure 2) is simulated using PLECS, under the rated operating conditions mentioned in Table 1. Then the harmonic spectrum (Figure 6b) and the ripples in time domain waveform (Figure 7b) of the total capacitor current is studied to find the phase-shift angle at which maximum high-frequency harmonic ripple cancellation occurs, which produces the minimum the overall RMS value of the DC-capacitor current. This will be the optimal $\theta_{fsw\_optimal}$. The same method is applied to the multi-converter system with a common DC-bank shown in Figure 3 to obtain its optimal carrier phase-shift angle.

The switching frequency harmonic component $f_{sw\_harmonic} = 40kHz$ is shown for various phase-shift angles (θ_{fsw_2}) applied to the carrier frequency of lower inverter for the multi-converter system with common DC-bank in Figure 6a and the multi-converter system with individual DC-bank in Figure 6b. At $\theta_{fsw\_2} = 0°$(violet colour bar), there is no phase-shift applied and this case scenario is taken system using the conventional method. Among the various phase-shift angles analyzed, it can be seen that the harmonic ripple ($f_{sw\_harmonic} = 40kHz$) is minimum when $\theta_{fsw\_2} = 90°$, denoted by the red color bar in Figure 6a, and green color in Figure 6b. Thereby, it can be observed from Figure 6 that both the topologies (shown in Figures 2–3) have minimum main switching frequency harmonic component ($f_{sw\_harmonic} = 40kHz$) and maximum DC-capacitor current ripple cancellation at 90°. Furthermore, at 90° carrier phase-shift angle, there is maximum ripple cancellation in the DC-capacitor bank current as illustrated in Figure 7. It can be understood that the capacitor current ripple is almost half the value (red dotted line) when compared to the scenario where there is no phase-shift applied (violet line) in both the multi-converter

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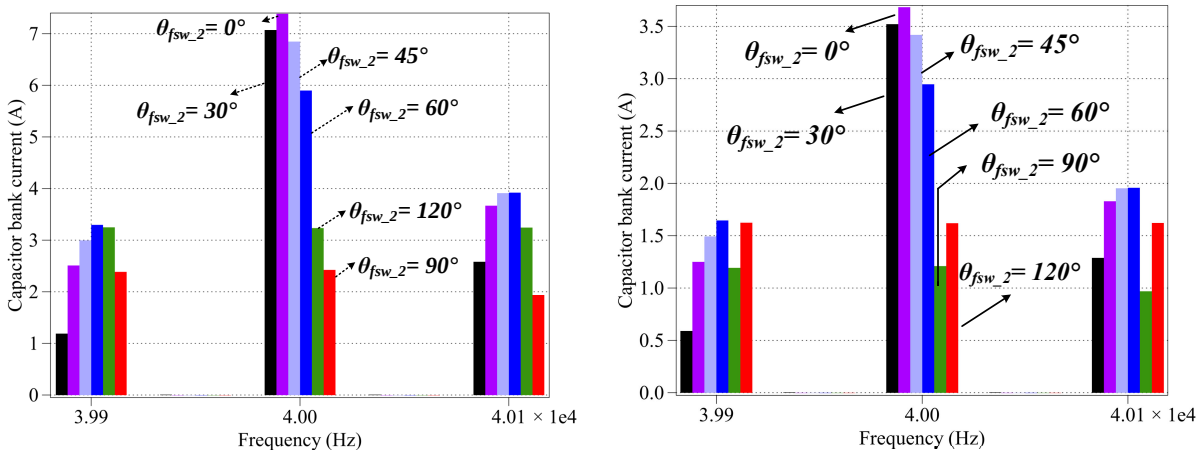
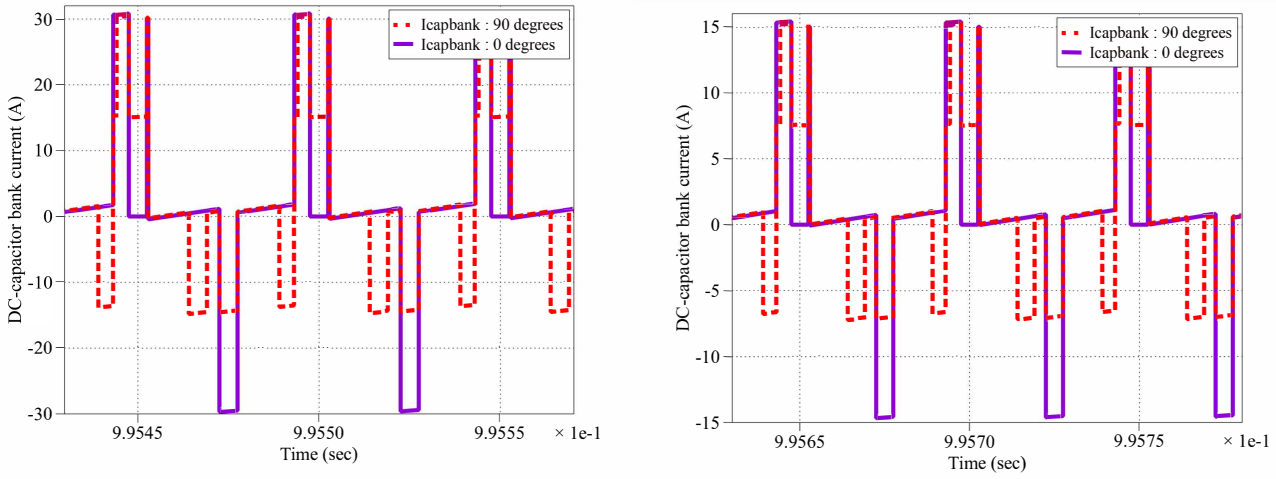
system with individual DC-bank and common DC-bank. Accordingly, from Figures 6–7, it can be concluded that the optimal phase angle is found to be when the two carrier signals for two inverters are phase-shifted by 90°.



(a) (b)

Figure 6. The $f_{sw\_harmonic} = 40kHz$ harmonic spectrum of capacitor bank current for various θ_{fsw_2} for the multi-converter system with: (**a**) common DC-bank, and (**b**) individual DC-bank – both at rated operating conditions.



(a) (b)

Figure 7. DC-capacitor bank current ripple reduction at $\theta_{fsw\_2} = 0°$ (violet line), and $\theta_{fsw\_2} = 90°$ (red dotted lines) for: (**a**) the multi-converter system with common DC-bank, and (**b**) the multi-converter system with individual DC-bank.

The optimally phase-shifted switching cycles lead to variations of the output current ripples, which when summed together results in the minimization of ripples at DC-link current as shown in Figure 8e. Reduction of the DC-capacitor current ripples means that the switching frequency harmonics reduces (since a unipolar SPWM is used, for $f_{sw} = 20kHz$, the main switching frequency harmonic component appears at $f_{sw\_harmonic} = 40kHz$). Consequently, the overall DC-capacitor RMS current decreases, thus reducing the overall stress (electro-thermal stress, and hot-spot temperature) at the DC-link. Hence, the proposed scheme is shown in Figure 8 (in red line) helps to reduce harmonics, and thereby the total harmonic distortion (THD) in the DC-capacitor current. Without any phase-shift, the THD =5.8% for the capacitor current, and after applying the proposed optimal phase-shifting, the THD reduces to 2.7%, calculated as per [26].

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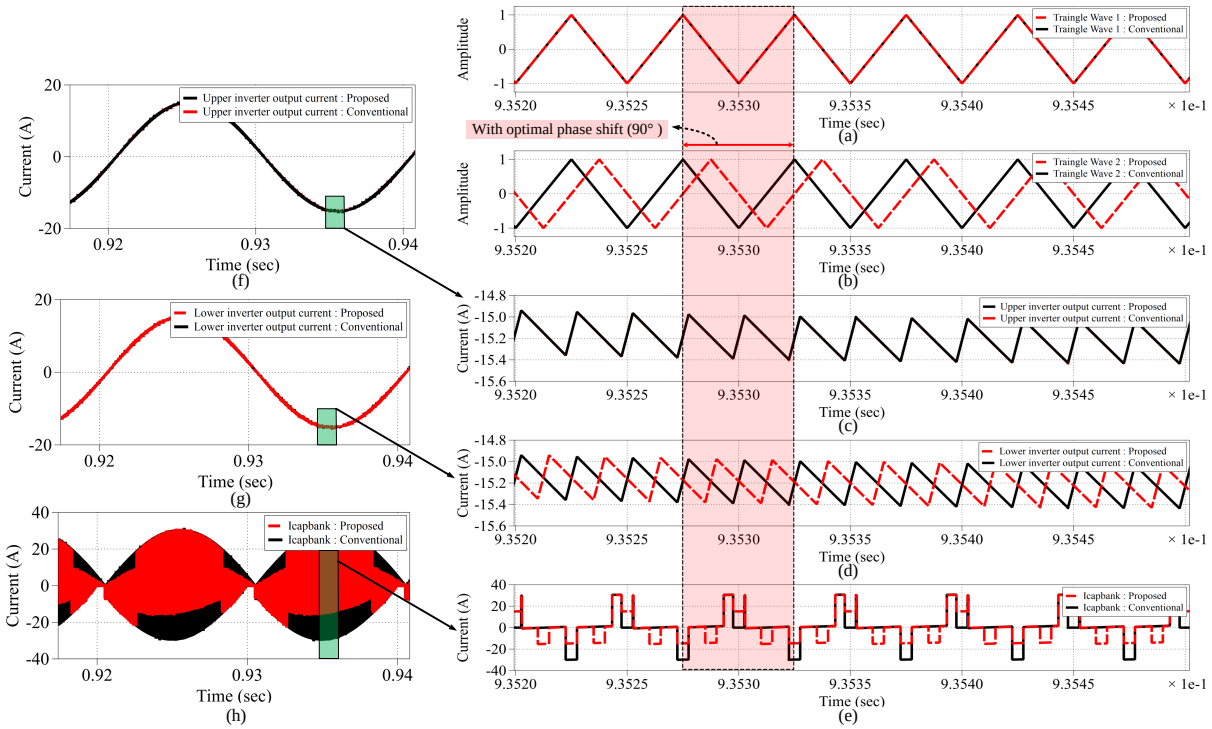

Figure 8. Red lines (proposed method with optimal phase-shift) and black lines (without any phase-shift): (**a**) upper inverter carrier wave, (**b**) lower inverter carrier wave, output current ripple of: (**c**) upper inverter, and (**d**) lower inverter, (**e**) total DC-capacitor current ripple, the time-domain waveform of output current from the: (**f**) upper inverter and (**g**) lower inverter, (**h**) total DC-capacitor current waveform.

5. Lifetime Estimation of DC-link Capacitor

Reducing the harmonics ripples in the DC-capacitor current helps to improve the lifetime L_x of the DC-capacitor as the overall electrical and thermal stress in the capacitor significantly decreases [15]. The lifetime prediction model used in this paper is shown in Equation (10) and explained in detail (including the equivalent circuit model of capacitor) in [26].

$$L_x = L_o \times \underbrace{(\frac{V}{V_{rated}})^{-p}}_{K_V} \times \underbrace{2^{\frac{(T_{rated}-T_h)}{10}}}_{K_T} \tag{10}$$

L_o is the rated lifetime of the capacitor at rated voltage V_{rated} , and rated upper category temperature T_{rated} (given in Table 4). K_T is the temperature factor, and K_V is the voltage ripple factor. V is the actual operating voltage. The value of the exponent p is between 3-5 for El-caps [15]. The hot-spot temperature T_h of the DC-capacitor, estimated by Equation (11) depends upon the operating temperature and P_{loss} the power loss of the capacitor (which is a function of ripple current and ESR). Considering the heat dissipation from the diode bridge, DC-link filter, and inverter, the operating temperature T_a is defined as $40 - 60^{\circ}C$ instead of the room temperature [14]. P_{loss} can be estimated by Equation (12).

$$T_h = T_a + (P_{loss} \times R_{th}) \tag{11}$$

$$P_{loss} = \sum_{i=1}^{n} (I_{rms(f_i)})^2 \times ESR(f_i) \tag{12}$$

where $I_{rms(f_i)}$ is the RMS value of harmonic ripple current at frequency f_i, obtained from the harmonic spectrum of capacitor current. $ESR(f_i)$ is the ESR of at the i^{th} frequency f_i.

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R_{th} is the thermal resistance of the capacitor between the hot spot and ambient. The rated values for the chosen capacitor (KEMET AlS8(1)(2)392NF500) in this paper are given in Table 4.

6. Results and Discussion

In this section, the effectiveness of the proposed harmonic mitigation for both the multi-converter system with common DC-bank and the multi-converter system with individual DC-bank is analyzed through experimental and simulation results.

As shown in Figures 2–3, the multi-converter system with a common DC-bank differs from the multi-converter system with individual DC-bank mainly in terms of the DC-link capacitor bank configuration. In the common DC-bank topology (shown in Figure 3), the current harmonics from both inverters flow through the common capacitor bank, consisting of two parallel capacitors. This means that the harmonics from all the parallel-connected inverters flow into this common capacitor bank. Hence, there is a constrain to have a large DC-link capacitor to absorb the harmonics at DC-link, when numerous inverters are connected in parallel in the multi-converter system with a common DC-bank. Alternately, in the multi-converter system with individual DC-bank, each inverter has its own DC-bus, meaning that harmonics from each inverter are absorbed by its own individual DC-capacitor bus. This topology has the advantage that a greater number of inverters can be connected to a common DC-bus without the need to increase the bulkiness of the DC-bank. Therefore, due to the aforementioned reasons, when a greater number of inverters needed to be connected in parallel to the DC grid with a centralized rectifier, the multi-converter system with individual DC-bank (Figure 2) is preferred.

6.1. Experimental verification (with scaled-down parameters)

In order to validate the proposed optimal carrier phase-shift angle for the topologies, referring to Figures 2–3, a downscale experimental platform is built, where resistors are used as the loads as shown in Figure 9. The scaled-down main circuit parameters are listed in Table 5. Compared to the simulation result, the operating conditions are scaled down to enable lab-scale experimentation. For both the inverters, the operating conditions are kept the same throughout the experiment, as explained in Table 6. Both the SEMIKRON power stacks are connected to a common DC-bus, and the PWM signals for each of these are controlled by the PLECS-RT box 2. Since RT-box PWM signals have only 5V, LM393 comparators are used to shift this voltage level to 15V (the minimum requirement for gate drivers to operate). A constant DC-voltage source of 50V is supplied at the common DC-point for both the power stacks by the DC-power supplier.

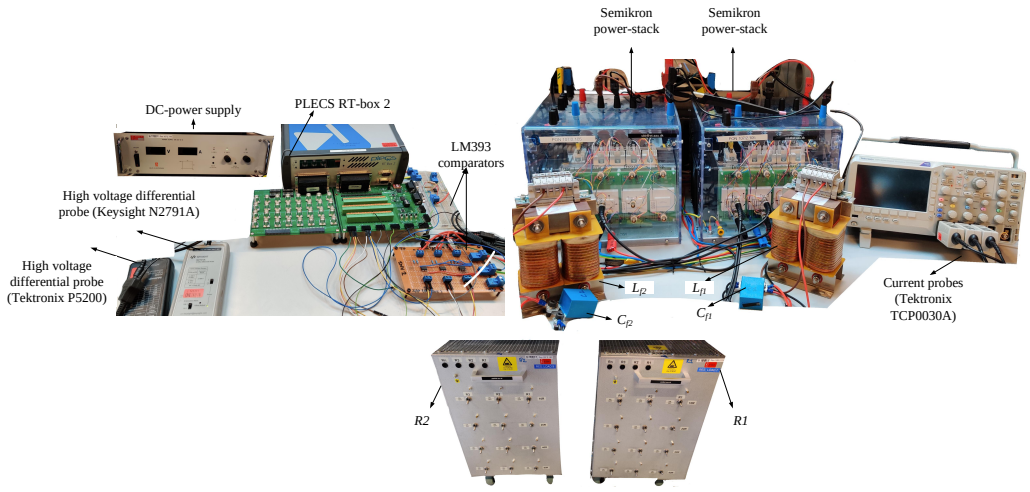

Figure 9. Experimental prototype of the multi-converter system.

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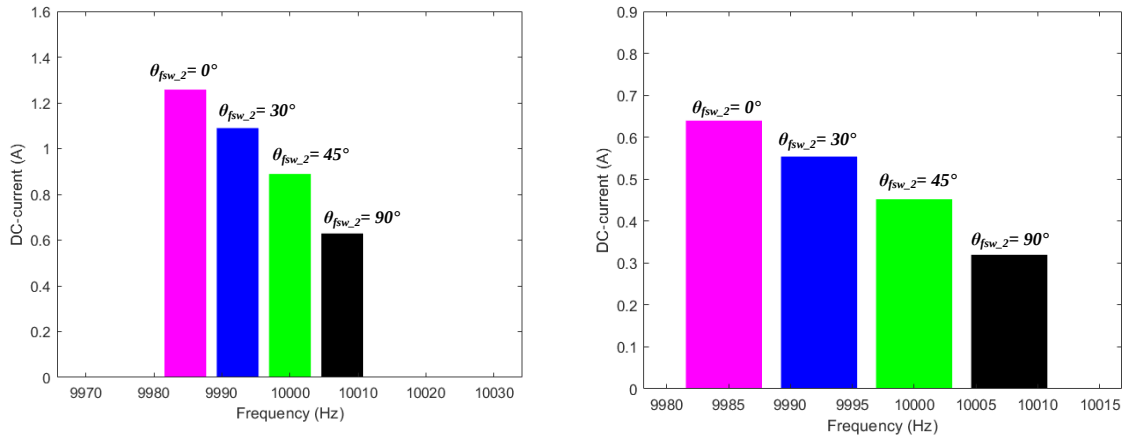
Table 5. Experimental system specifications

Module	Part Number/ Parameter	Symbol
SEMITEACH IGBT module stack	SEMIKRON 08753450	-
AC-filter inductors	4mH, 20A rated current	L_{f1},L_{f2}
AC-filter capacitors	$1\mu F$, 1600 V, 19.1 A @ 40°C	C_{f1},C_{f2}
Voltage comparators	LM393	-
PLECS controller box	RT-box 2	-
Resistor Banks	10Ω-80Ω	R_1,R_2

Table 6. Operating conditions (scaled - down) for the experimental analysis

Parameter	Symbol	Value
Rated power of each inverter (W)	P_o	50
Load (Ω)	R_L	20
Rated RMS load voltage (V)	$V_{sine-ref}$	40
Load frequency (Hz)	f_o	50
Rated DC-link voltage (V)	V_{dc-ref}	50
Switching frequency (kHz)	f_{sw}	5
Modulation amplitude index	M_A	0.8

One of the ways to validate the effectiveness of the proposed harmonic mitigation strategy is to observe the switching frequency harmonics (i.e. at 10kHz) for various carrier phase-shift angles in the I_{dc} for the multi-converter system with common DC-bank, and I_{dc_1} for the multi-converter system with individual DC-bank. It is difficult to obtain these two wave-forms directly. Due to the presence of a large DC-link capacitor in the power stack, only low harmonics of I_{dc} and I_{dc_1} can be measured, as all higher harmonics are absorbed by DC-capacitor. So, the CSV data for I_{dc} and the capacitor current $I_{capbank}$ was obtained from the oscilloscope measurements for the multi-converter system with a common DC-bank, and the harmonic spectrum was obtained in MATLAB. Similarly, for the multi-converter system with individual DC-bank, the CSV data for I_{dc_1} and the capacitor current $I_{capbank\_1}$ was obtained from the oscilloscope measurements, and the harmonic spectrum was obtained in MATLAB. The obtained results are shown in Figures 10a–10b, respectively. It shows that the switching frequency harmonics (at 10kHz) is minimum when carrier phase-shift of $\theta_{fsw\_2} = 90°$, is applied for the proposed two multi-converter systems, making it the optimal carrier phase-shift angle. These results are hence, in agreement with the proposed DC-link harmonic mitigation method explained in Section. 4.



(a) **(b)**

Figure 10. Experimental data plotted in MATLAB showing the $f_{sw\_harmonic} = 10kHz$ harmonic spectrum of DC-link current for various θ_{fsw_2} for the multi-converter system with: (**a**) common DC-bank, (**b**) individual DC-bank – both under scaled down operating conditions, given in Table 6.

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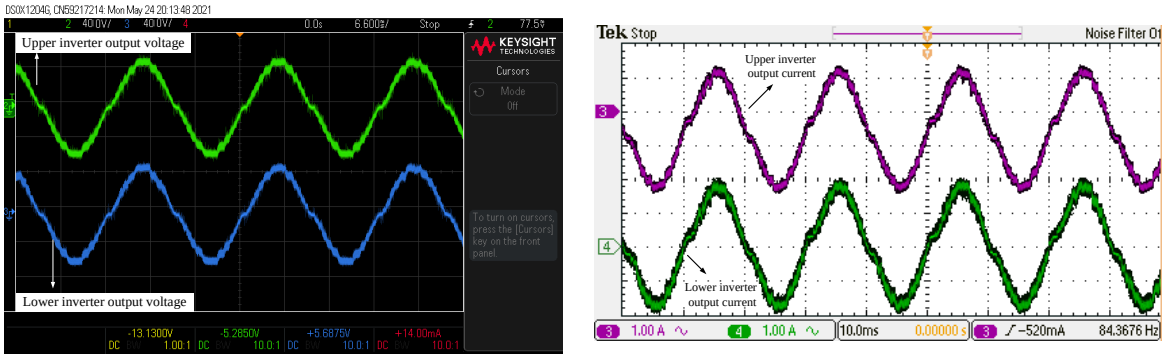
The output voltage and current waveforms at $\theta_{fsw\_2} = 0°$, and $\theta_{fsw\_2} = 90°$, for the multi-converter system with a common DC-bank captured in the oscilloscopes, are shown in Figure 11. Since the output voltage and current waveforms are not affected by the phase-shift in carrier waves, they overlap each other at $\theta_{fsw\_2} = 0°$, and $\theta_{fsw\_2} = 90°$.

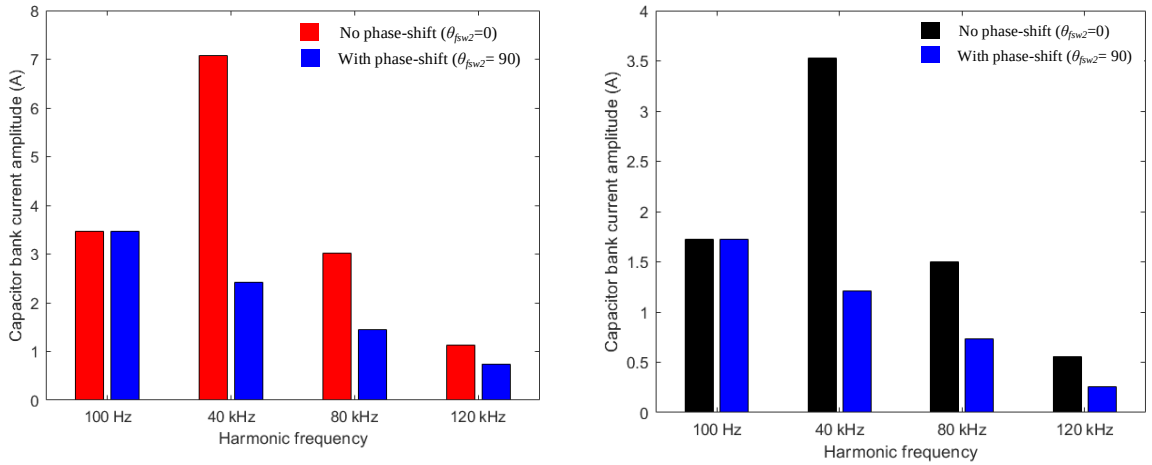


(a) **(b)**

Figure 11. Measured waveforms of the multi-converter system with a common DC-bank (**a**) output voltages (**b**) output currents- two inverter units interleaved at $\theta_{fsw\_2} = 0°$, and $\theta_{fsw\_2} = 90°$, using parameters Table 6.

6.2. DC-harmonic analysis -using optimal phase-shift angle for the carrier signal

To illustrate the DC-link harmonic mitigation method, the optimal phase-shift angle for carrier signal (i.e. $\theta_{fsw\_optimal} = 90°$) is applied to both the topologies shown in Figures 2–3. Each of the two inverters (of two topologies) is simulated (in PLECS) under rated output power of 2.5 kW and has the same the rated operating conditions given in Table 1. The effect of applying interleaving to the carrier signals of the parallel-connected inverters is illustrated in Figure 12.



(a) **(b)**

Figure 12. Effect of the optimal shift in the DC-capacitor bank current harmonics for: (**a**) the multi-converter system with common DC-bank, (**b**) the multi-converter system with individual DC-bank.

It can be seen that adopting the proposed method helps to reduce the dominant switching harmonic components ($f_{sw\_harmonic} = 40kHz, 80kHz, 120kHz$) in the DC-capacitor bank current, and overall RMS capacitor bank current. As a result, the electro-thermal stress for each capacitor reduces thereby increasing its life expectancy calculated using Equations (10)–(12), as shown in Table 7. From the industry point of view, it is important

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to have a lower DC-capacitor bank current as a lesser number capacitor is now needed, which helps to lower the cost of the overall system.

Table 7. Operating conditions (scaled - down) for the experimental analysis

Topology	$P_{loss}(Watts)$ $\theta_{fsw\_2} = 0^\circ$	$L_x(hours)$ $\theta_{fsw\_2} = 0^\circ$	$P_{loss}(Watts)$ $\theta_{fsw\_2} = 90^\circ$	$L_x(hours)$ $\theta_{fsw\_2} = 90^\circ$
The multi-converter system with common DC-bank	1.27	1.35×10^5	0.41	1.70×10^5
The multi-converter system with individual DC-bank	0.33	1.73×10^5	0.12	1.85×10^5

However, it is necessary to take into consideration the fact that from a practical application standpoint, it is almost impossible to achieve the loading of two drives according to operating at rated conditions [27]. So, to further demonstrate the effectiveness of the proposed method under such scenarios, for the topologies shown in Figures 2–3, the output load of the lower inverter is varied between 0W to 2500W (rated power), while the upper inverter is at a rated output power of 2500W. In each case, the first ($f_{sw\_harmonic} = 40kHz$) and second switching frequency harmonic component ($f_{sw\_harmonic} = 80kHz$) is observed when $\theta_{fsw\_2} = 0^\circ$ (conventional method), and $\theta_{fsw\_2} = 90^\circ$(proposed method) as shown in Figure 13.

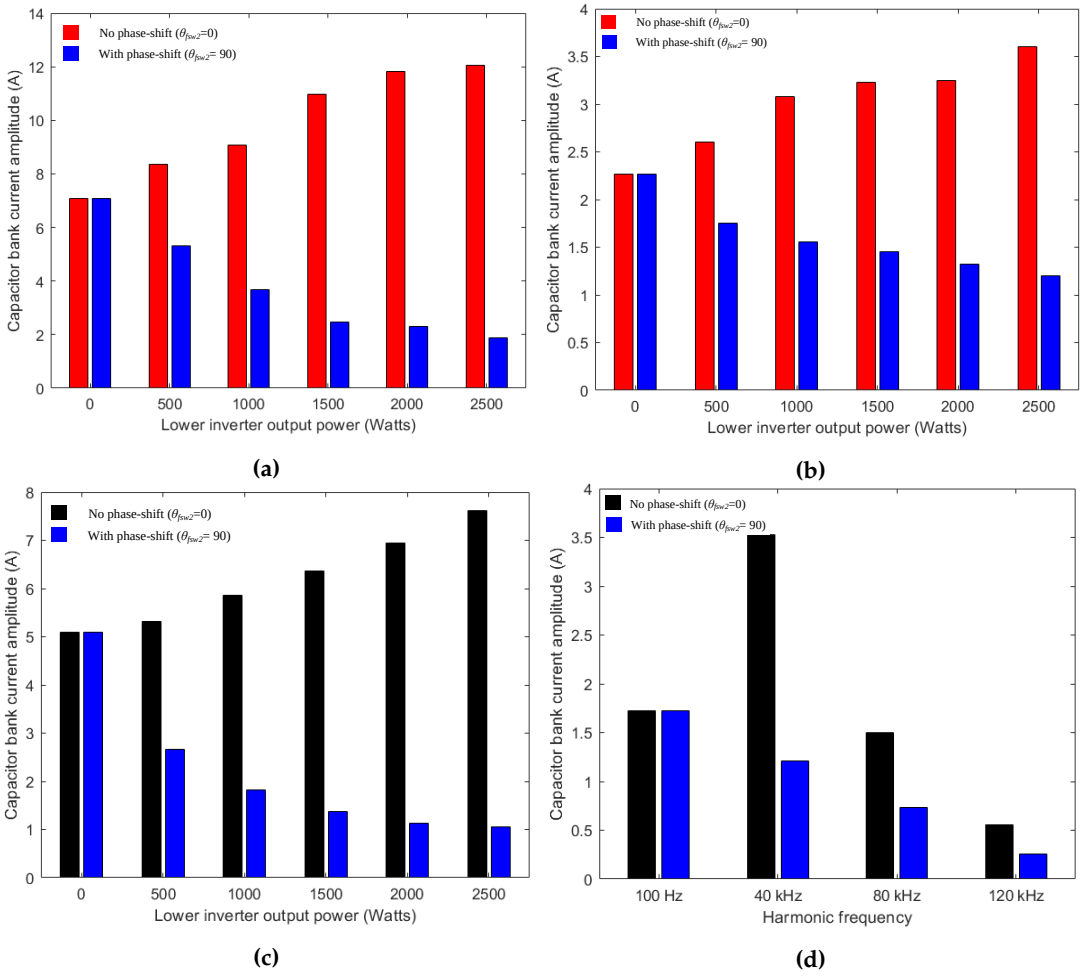

Figure 13. Effect of optimal shift in the DC-capacitor bank current for varying lower inverter loading in: the multi-converter system with common DC-bank for (**a**) $f_{sw\_harmonic} = 40kHz$, (**a**) $f_{sw\_harmonic} = 80kHz$, and in the multi-converter system with individual DC-bank for (**c**) $f_{sw\_harmonic} = 40kHz$, (**d**) $f_{sw\_harmonic} = 80kHz$.

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It is demonstrated in by the above Figures 13a–13d that as the output power of lower inverter (P_{o2}) varies from 500 W to 2500 W, the first and switching frequency harmonic component amplitude reduces, due to the impact of intervening of the carrier waves. The only time when there is no harmonic ripple cancellation is when P_{o2} =0W, the scenario where the lower inverter is not operating, due to which there is no interleaving (phase-shifting) occurring. Alternately, the maximum ripple cancellation (or in other words the minimum amplitude of switching frequency harmonic components) is achieved when each of the two inverters has the same output power, (i.e. case when P_{o2} = 2500 W in Figures 13a–13d. This is because, at the same output loading scenarios, the DC-ripples will be equal (due to the same output power) and opposite (due to $\theta_{fsw\_2} = 90^{\circ}$). Remarkably, even in cases where the inverters do not have the same output power (P_{o2} is between 500W and 2000 W), the DC-current harmonic (ripple) reductions occur. This result is of particular importance in industrial applications where parallel-connected inverters do not run at the same rated power. Applying the proposed method will help to reduce the harmonic content at DC-link, thereby reducing the requirement to use a large number of DC-link capacitors (saves cost).

Among the two topologies, the multi-converter system with individual DC-bank is more preferred due to the flexibility it gives the industrial designers to play with the number of inverters being connected to the centralized rectifier, and also the better lifetime of its DC-link capacitors (Table 7). Notably, one of the advantages of having a centralized rectifier is that, in the event of power failure, it is easy to connect a backup battery at the common DC link connecting the parallel inverter systems. Finally, in the future, it is also possible to integrate renewable energy resources without much difficulty at the common DC link in these kinds of systems.

7. Conclusions

In this paper, a carrier-based phase-shifting scheme is presented to minimize the DC-link current harmonics in the two proposed configurations of common DC-connected multi-converter systems having a centralized rectifier. Using a centralized rectifier is more compact, and reliable due to the reduction of conversion stages in the power system. Analyzed results showed that the maximum high-frequency harmonic ripple cancellation in the DC-capacitor bank current is when the carrier waves of the paralleled-inverters are phase-shifted by 90° angle (optimal phase angle). This helps to reduce the overall DC-capacitor bank current by almost 50%, thereby improving the lifetime of DC-link capacitors due to lesser power loss within the DC-link capacitor. Thereby, the cost of the overall system will be lower as a lesser number of capacitors are needed in the DC-link. Remarkably, even in cases where the inverters do not have the same output power, the DC-current harmonic (ripple) reduction occurs at the optimal phase angle. The outcome of this paper is a simple and effective solution for industrial designers to practically configuring multi-inverter systems with reduced DC-link current harmonics, even when most of the drives are not operating at rated power levels.

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