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Article

Basic modifications of "floating" differential stages based on complementary field-effect transistors with a control p-n junction

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Abstract: The circuitry of the summarized "floating" differential stages (FDS) based on complementary field-effect transistors with a control p-n junction (CJFET), intended for use in low-noise analog microcircuits, for example, operational amplifiers. The results of modeling the flow characteristics of one of the CJFET FDSs in the LTSpice XVII environment at low temperatures (down to -197 ^{0}C) and exposure to a neutron flux in the range of 1e13 ÷ 1e15 n / cm^2 are presented.

Keywords: Analog microcircuit, differential stage, complementary field-effect transistors with control p-n junction, low temperatures, neutron flux

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1. Introduction

One of the promising circuit solutions that have been used in low-noise Op-amps are "floating" differential stages [1], which have low sensitivity characteristics to changes in supply voltages and input common-mode signals. The FDS circuitry of this class has received further development in recent years in works [2-9].

The use of complementary JFETs, which are mastered in the framework of a number of modern technological processes [10,11], provides a low noise level and increased resistance of analog microcircuits to the effects of penetrating radiation. For many problems of analog circuitry, floating FDSs are promising not only on silicon JFETs, but also on JFETs based on SiC, GaN, GaAs transistors [12].

The purpose and novelty of this article is to consider the main properties of the new topologies JFet FDS [1-9], which are studied on the models of JFET transistors of corporation "Integral" (Minsk) and corporation "SPE" Pulsar "(Moscow).

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2. Basic CJFET circuits for floating differential stages.

According to a number of publications [3-9,15-20], to date, more than 10 variants for constructing differential cascades of this FDS class have been developed.

The classic "floating" DS circuit in Fig. 2.1, as a system in the case, is implemented on two JFET microcircuits LSJ698 and LSK489 [1], which contain pairs of transistors with p-channel (LSJ698) and n-channel (LSK489). At the same time, a sufficiently stable static mode is provided over a wide temperature range.

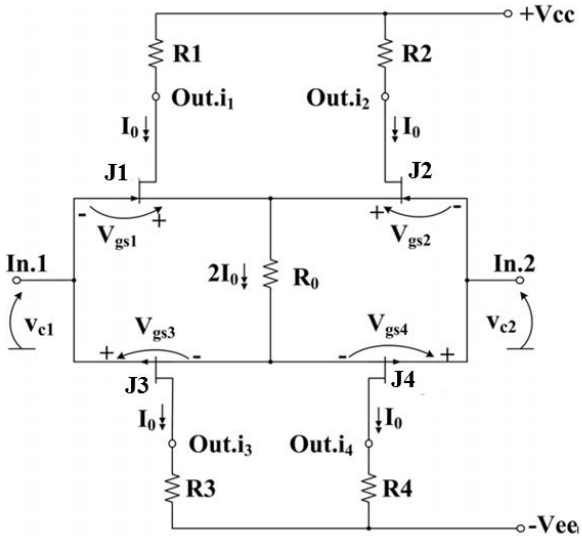

Figure 2.1-Classical scheme of "floating" input DS on JFET chips LSJ689 [21] and LSK489 [22]

CJFET DS in Fig.2.2 [3] provides increased attenuation coefficients common-mode rejection ratio (Kcm) and suppression of noise on the power buses (Ksn).

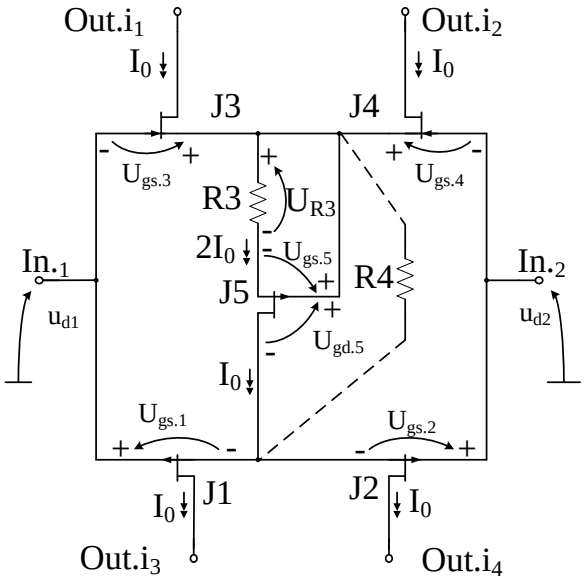

Figure 2.2 - "Floating" DC with increased Kcm and Ksn

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Figure 2.3 shows a CJFET multichannel DS class AB [7], which converts the input differential voltage into paraphase output currents in a wide range of input signals. This circuit is recommended for use in operational amplifiers with an increased maximum output voltage rise rate.

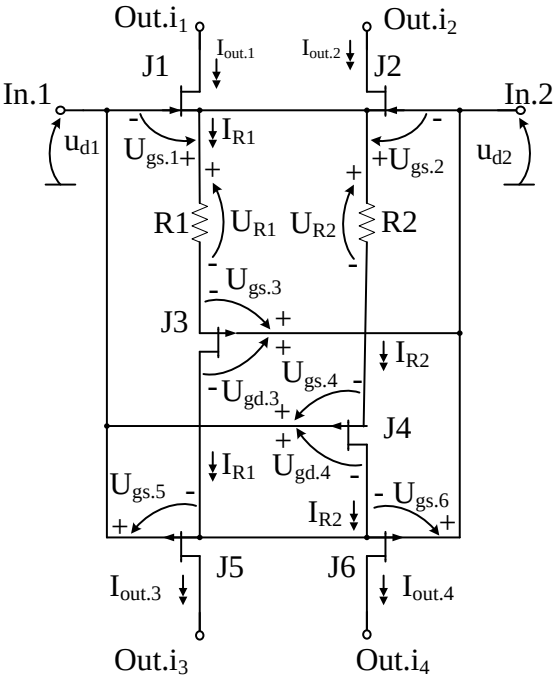

Figure 2.3 - CJFET multi-channel DS class AB

The DS circuit in Fig.2.4 [6,8,9] provides for wide-range adjustment of the voltage limiting the pass-through characteristic, which is important for constructing high-speed Op-amps. In addition, the DS in Fig. 2.4 in comparison with the DS in Fig. 2.2 has a doubled input capacitance.

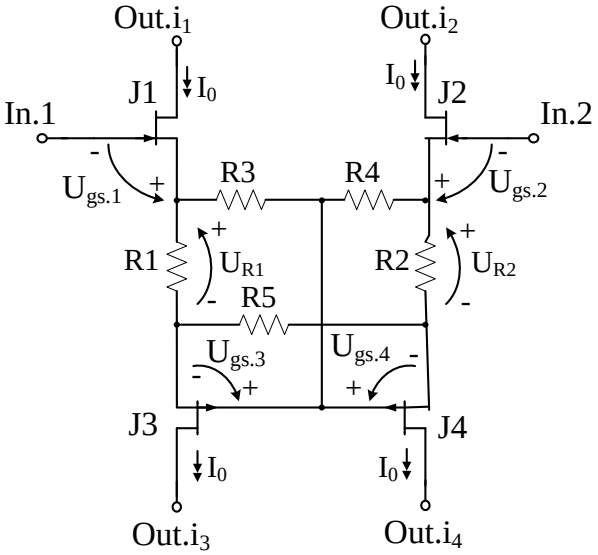

Figure 2.4 - CJFET DS with reduced input capacitance

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Figure 2.5 shows the DS [4] on CJFET transistors with a control pn- junction, which provides higher values of Kcm and Ksn, incl. at negative temperatures (down to -197 ^{0}C) and providing the conversion of the input common mode voltage of the DS u_c into the currents of the DS outputs (Out.1, Out.2, Out.3, Out.4) in the range Vin = ± 1 V.

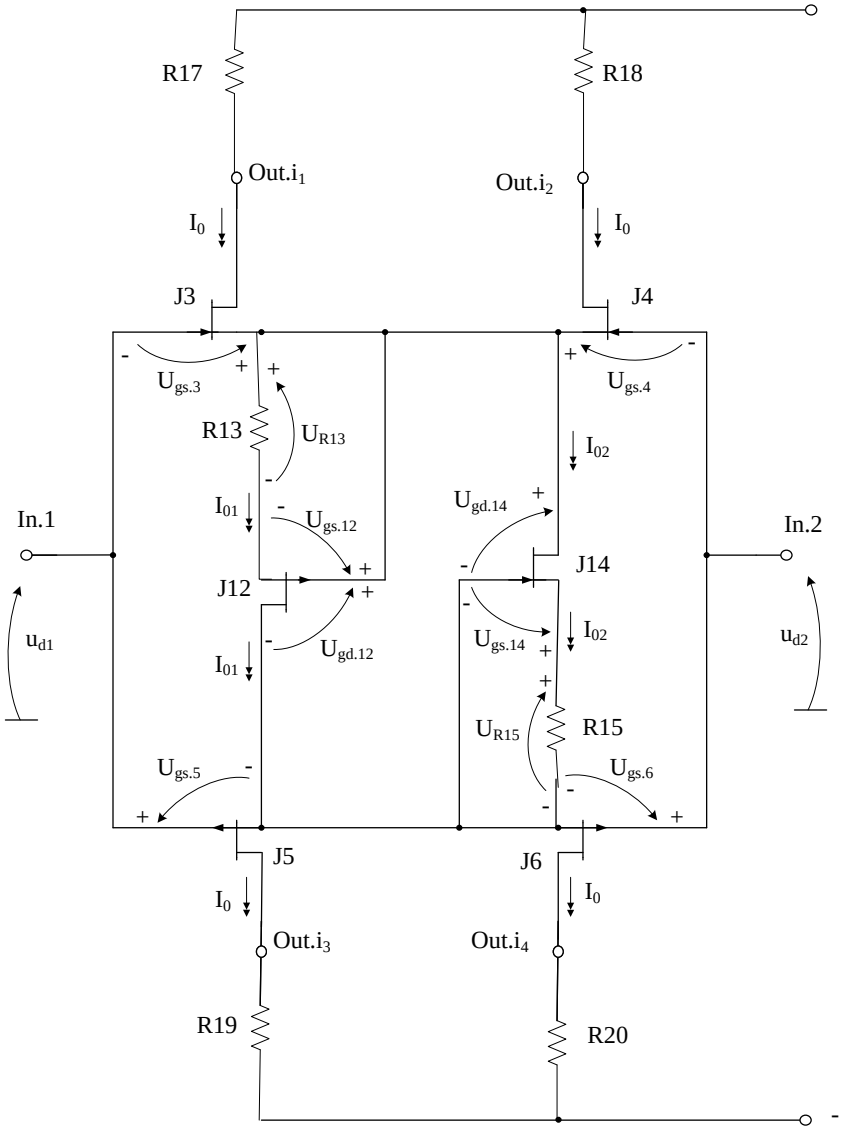

Figure 2.5 - DS [4] on complementary JFET field-effect transistors with increased attenuation of the input common mode signal

In Fig.2.6 DS [4] with increased stability of the static mode is presented, which provides, due to the rational choice of the numerical values R19, R20, insignificant changes in the currents in the resistor R20 over a wide temperature range. This allows you to stabilize the steepness of the DS and provide temperature stable values of its main static and dynamic parameters.

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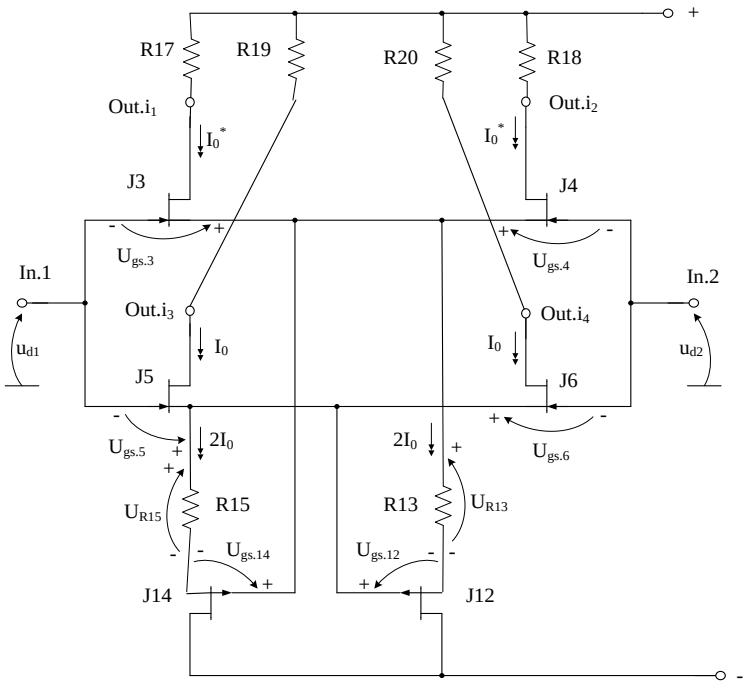

Figure 2.6-DS with increased stability of static modes [4]

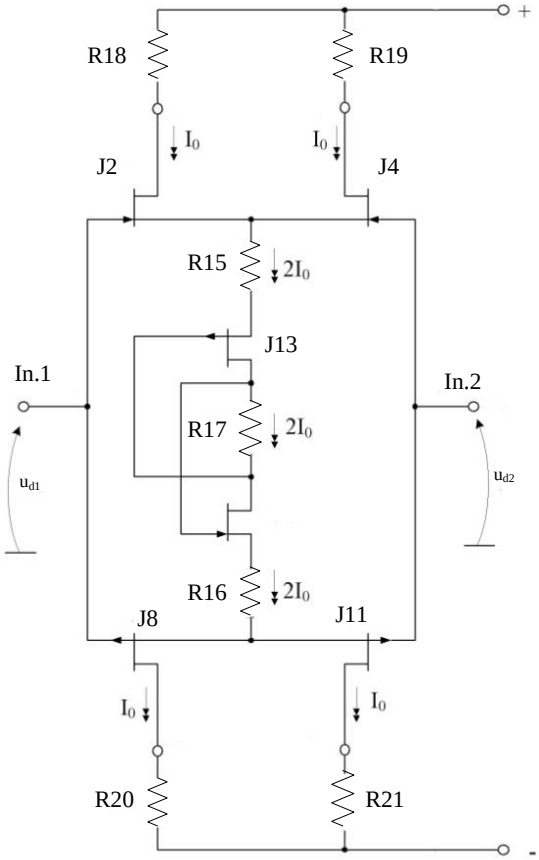

Figure 2.7-DS on complementary field-effect transistors with increased static mode stability [17]

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In Fig.2.7 The DS [17] is presented, in which the static mode for the source currents of the field-effect transistors J2 and J4, as well as J8 and J11, is set by a static mode stabilization circuit integrated into a single functional node, including as a whole the input J2, J4, J8, J11 and additional field – effect transistors J13, J14 with a control pn - junction. This makes it possible to do without classical reference current sources and solve the problem of establishing the static mode of the remote control in an unconventional way.

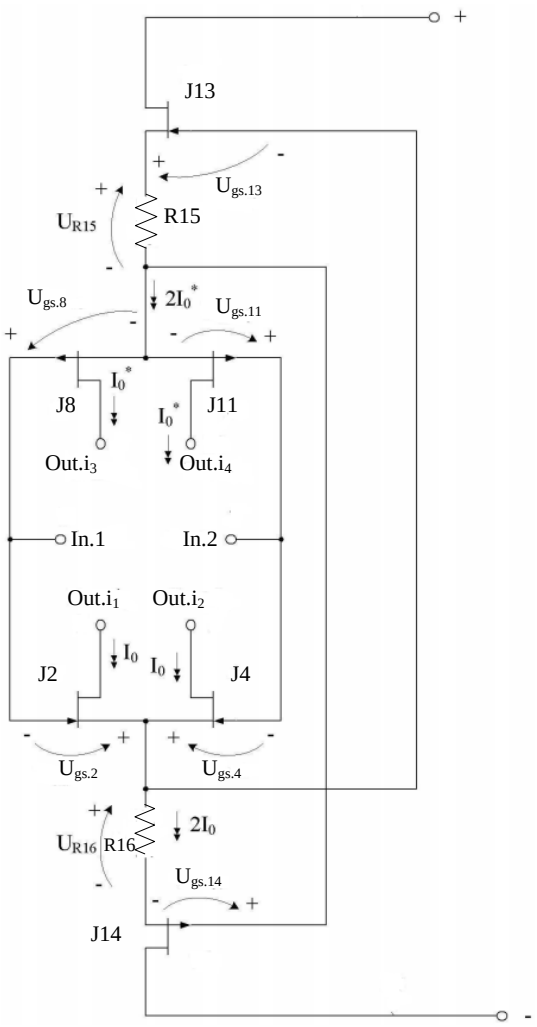

Figure 2.8-Input DS [18] on complementary field-effect transistors for operation at low temperatures

In Fig.2.8 The DS [18] is presented, in which the static mode for the source currents J2, J4, J8 and J11 of the input field-effect transistors, as well as the input field-effect transistors, is set by the DS static mode stabilization circuit integrated into a single functional node, which includes as a whole J2, J4, J8, J11 input field-effect transistors, as well as J13 and J14 additional field-effect transistors with a control pn - junction. Thus, the static DC mode in Fig.2.8 [18] practically does not depend on the value of the input common-mode signal $u_c=u_{c1}=u_{c2}$ and changes in the

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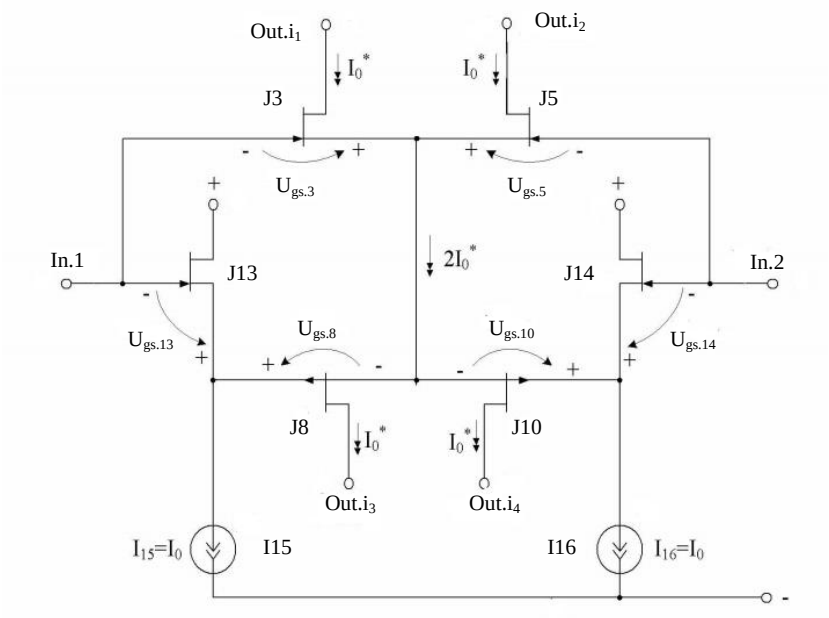
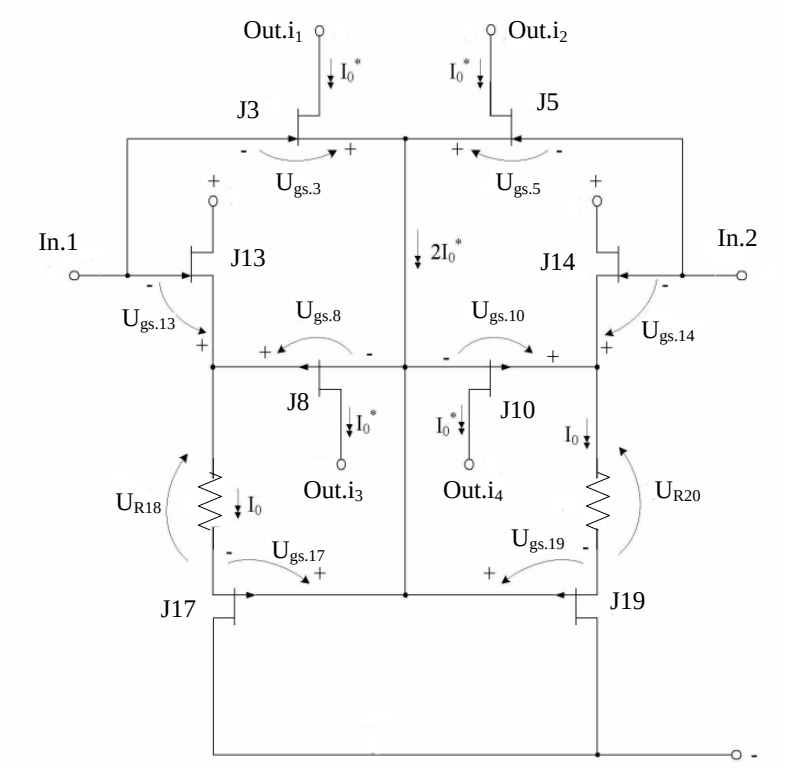
bus voltages of power sources. This allows you to exclude the DC from the scheme in Fig.2.8 traditional reference current sources that negatively affect its many parameters.



(a)



(b)

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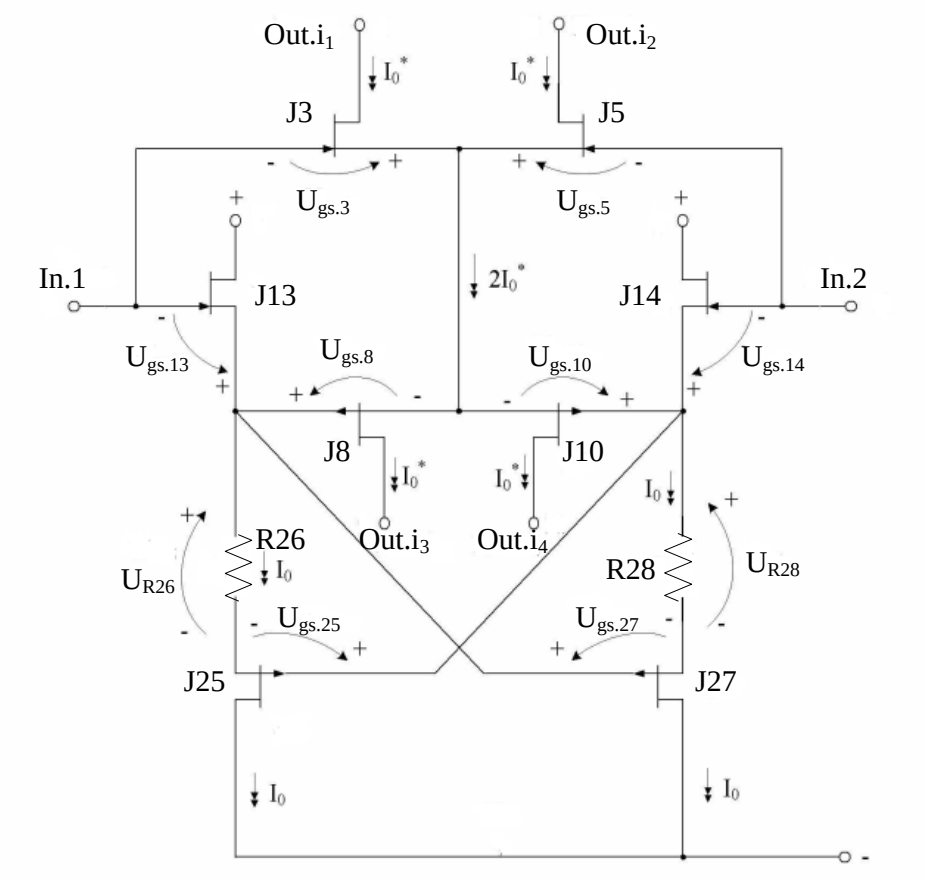

(c)

Figure 2.9-Modified DS class AB [19] on complementary field-effect transistors with a control pn – junction

In Fig.2.9 (a) shows a DS [19] operating in the class "AB" mode, when its maximum output currents exceed the static value I_0 by 5÷7 times. Large voltage limitations of the DS flow characteristic allow you to create a circuit based on Fig.2.9 (a) High-speed CJFet operational amplifiers. Figure 2.9 (b) and Figure 2.9 (c) show special cases of DC construction in Figure 2.9 (a), in which auxiliary field-effect transistors J17, J19, J21, J23, J25, J27 are introduced, which improve other parameters of the basic circuit in Fig. 2.9 (a) - the attenuation coefficient of the input common mode signals, the suppression coefficient of interference on the power buses.

In Fig.2.10 DS is presented on complementary field-effect transistors with a control pn - junction of class AB with a variable voltage limiting the pass characteristic [20]. To set the set value of the DS limit voltage, see Fig.2.10 additional resistors R19 and R20 are introduced. The change in the resistance of these resistors significantly affects both the maximum output currents of the DS and the voltage limiting its flow characteristics. This effect is realized both at room and cryogenic temperatures.

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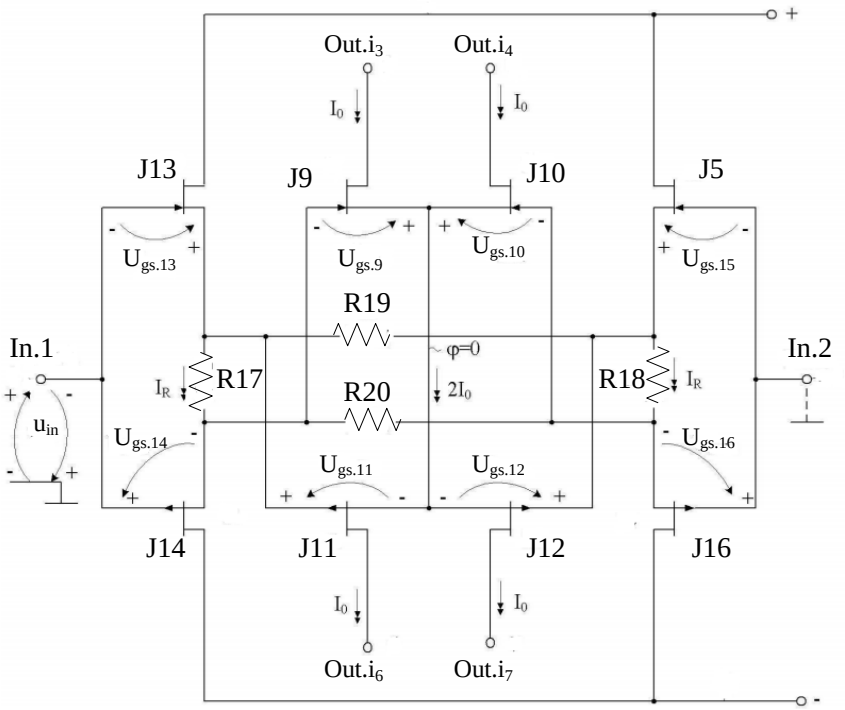

Fig. 2. 10-DS on complementary field-effect transistors with a class AB control pn junction with a variable voltage of the pass-through characteristic limitation [20]

3. Study of FS CJFet differential cascades with reduced input capacitance

In contrast to the well-known "floating" FS [1], the input capacitances of the gate-drain transistors J1, J2 are reduced by half in the scheme of Fig. 3.1 [16]. The current outputs of the circuit in Fig. 5 are matched with the positive (Out. i_1, Out.i_2) and negative (Out. i_3, Out.i_4) buses of the power supply. They can be connected to intermediate "bent" cascodes [1] for further amplification and conversion of signals, for example, into an Op-amp.

In the proposed FS in Fig.5, the static currents of the field-effect transistors J1, J2 are determined by the following equations:

$$I_{s1} = \frac{U_{gs.3}}{R_1} = I_{R1} = I_R, \quad (1)$$

$$I_{s2} = \frac{U_{gs.4}}{R_2} = I_{R2} = I_R, \quad (2)$$

$$I_{d.3} = I_{s3} = I_R = I_{d4} = I_{s.4}, \quad (3)$$

$$2I_R = I_{R1} + I_{R2}, \quad (4)$$

where I_{si} is the source current of the i-th field-effect transistor;

$U_{gs.\,3}$, $U_{gs.\,4}$ – the gate-source voltage of the corresponding input field-effect transistors J3, J4 at the operating point at a source current equal to I_R.

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Thus, by selecting the resistances of the resistors R1, R2 with the known drain-gate characteristics of JFET, the specified static current mode of all FS field-effect transistors is provided.

A distinctive feature of FS Fig. 3.1 is that its static mode does not depend on the value of the input common mode signal and changes in supply voltages.

If a positive input voltage of the is applied to input 1 relative to input 2, this causes an increase in the current through the input field-effect transistors J1, J4 and a decrease in the drain current of the field-effect transistors J2, J3.

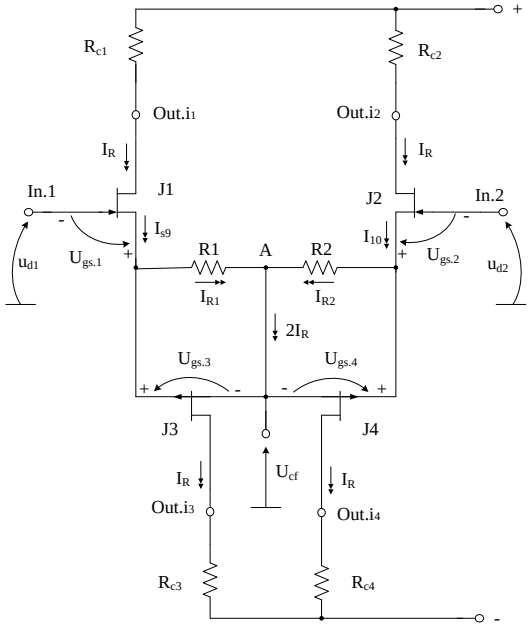

Figure 3.1 Circuit of a "floating" DC with a reduced input capacitance [16]

Figure 3.2, Figure 3.3 show other FS modifications that extend the properties of the basic circuit in Figure 3.1.

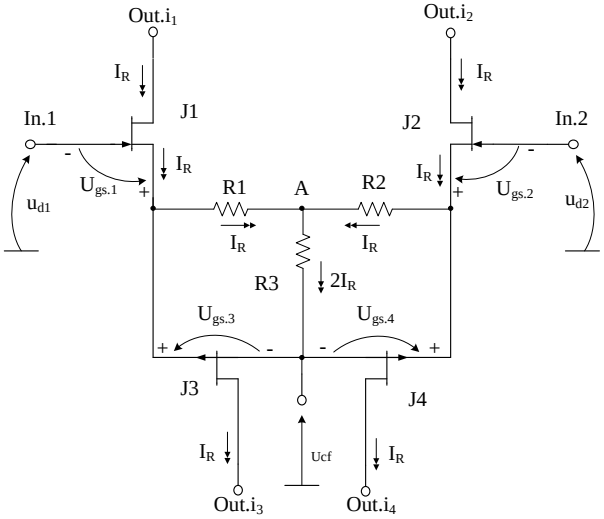

Figure 3.2 First modification of CJFET FS

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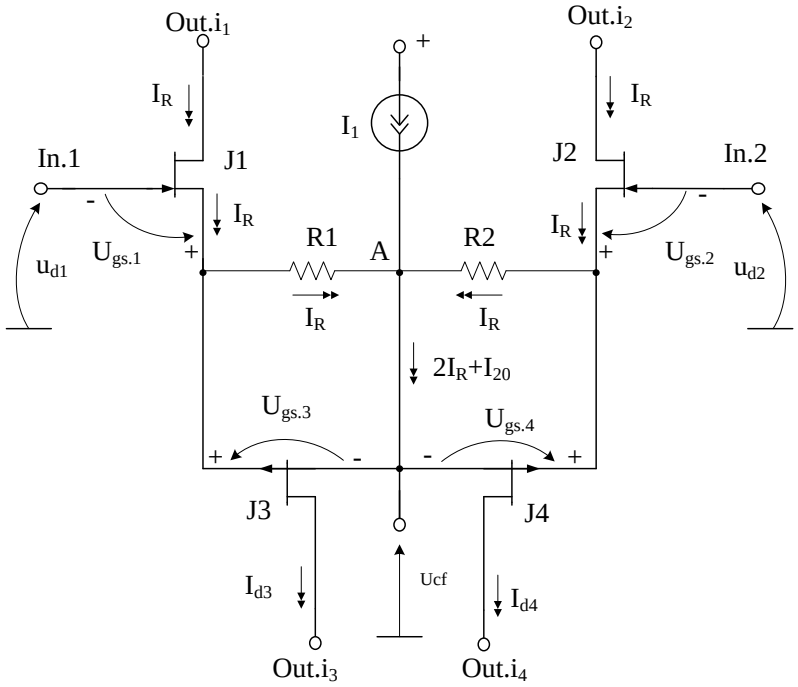

Figure 3.3 The second modification of the proposed in [16] FS

The FS circuit in Figure 3.4 has 4 current outputs (Out. i_1, Out. i_2, Out.i_5, Out.i_6) aligned with the positive bus of the power supply, as well as an increased steepness of converting the FC input voltage into the output currents of Out. i_5, Out. i_6.

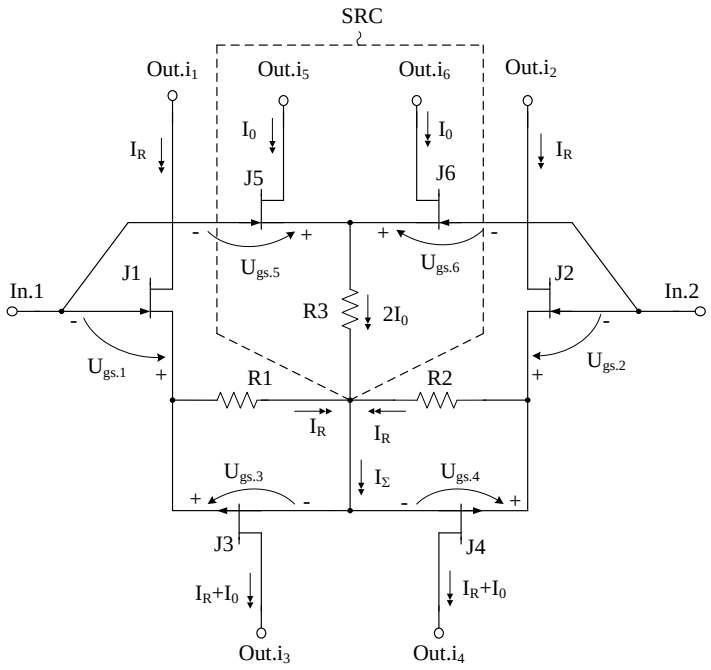

Figure 3.4 The third modification of the proposed in [16] FS

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In the FS circuit in Figure 3.5, the set values of the drain currents of the input field-effect transistors J3, J4 are also set by the resistor R3.

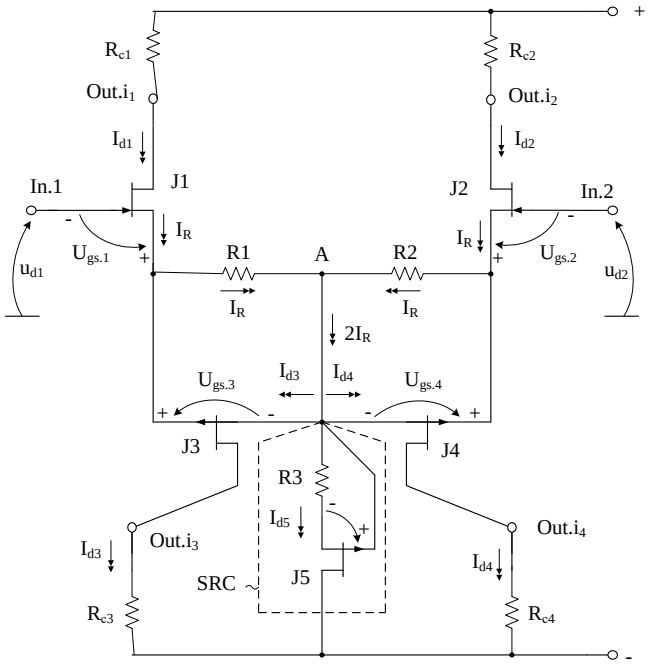

Figure 3.5 The fourth modification of the proposed in [16] FS

The peculiarity of the FS circuit in Fig. 3.6 is that here it has increased output resistances for all current outputs. This is achieved through the use of staged composite transistors and allows you to obtain higher values of the maximum voltage gain in the Op-amp on the basis of the circuit Fig. 3.6.

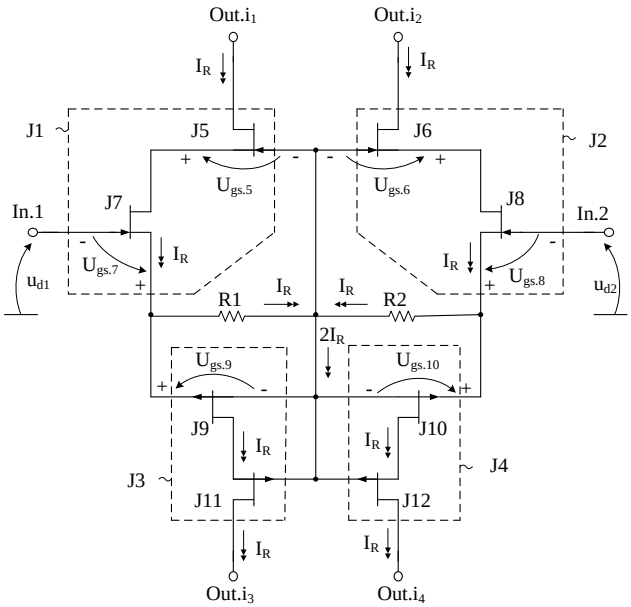

Figure 3.6-Diagram of the proposed FS with increased output resistances in [16]

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Figure 3.7 shows the pass-through characteristics of CJFet FS Figure 3.1 in the LTspice environment on JFET transistor models of Integral SPE (Minsk), at t=27°C, R1=R2=1k and measuring the input voltage in the range V= -1.5÷1.5 V.

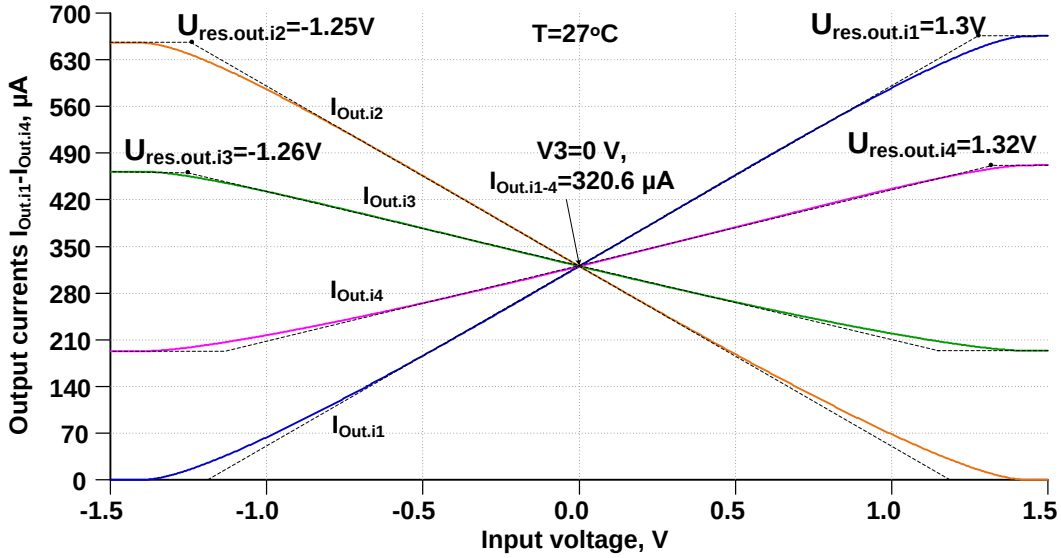

Figure 3.7 CJFet FS flow characteristics Figure 3.1 at t=27°C

The flow characteristics of CJFet FS Fig. 3.1 at negative temperatures "t= -197°C", R1=R2=1 k and measuring the input voltage in the range V= -1.5÷1.5 V are shown in Fig. 3. 8.

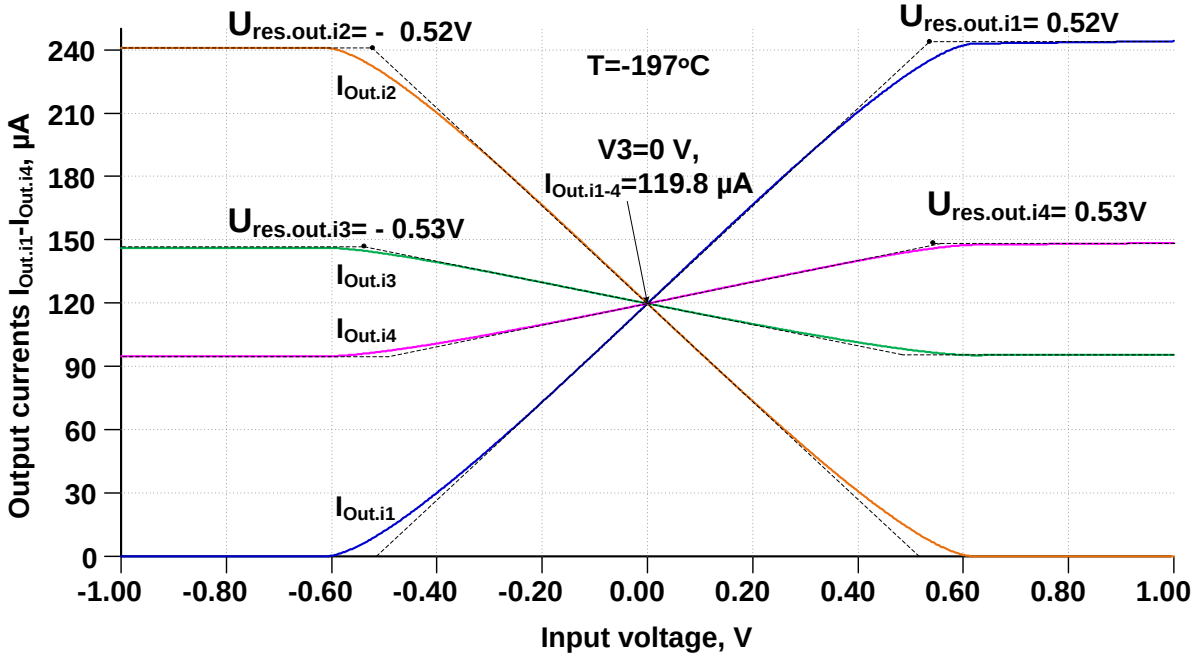

Figure 3.8 CJFet FS flow characteristics at t=-197°C

The simulation results (Fig. 3.7, Fig. 3.8) show that on the basis of the FS proposed in [16], it is possible to implement a wide range of pass characteristics with different numerical values of the limiting voltage U_l for the first and second, as well

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as the third and fourth current outputs. This allows you to purposefully select the numerical values of the U_l when designing differential and multidifferential operational amplifiers with a given speed in the large signal mode. Thus, the maximum rate of rise of the output voltage of the Op-amp with the classical architecture [13] is determined by the formula $SR=2nf_1U_l$, where f_1 is the frequency of the unit gain of the corrected Op-amp; U_l is the voltage limiting the pass characteristic of the input stage.

Figure 3.9 shows the dependence of the output currents of CJFet FS in Figure 3.1 on the neutron flux in the range Fn=1e13÷1e15 n / cm^2 at resistances R1=R2=1 k. At the same time, well-known models with JFet were used [14].

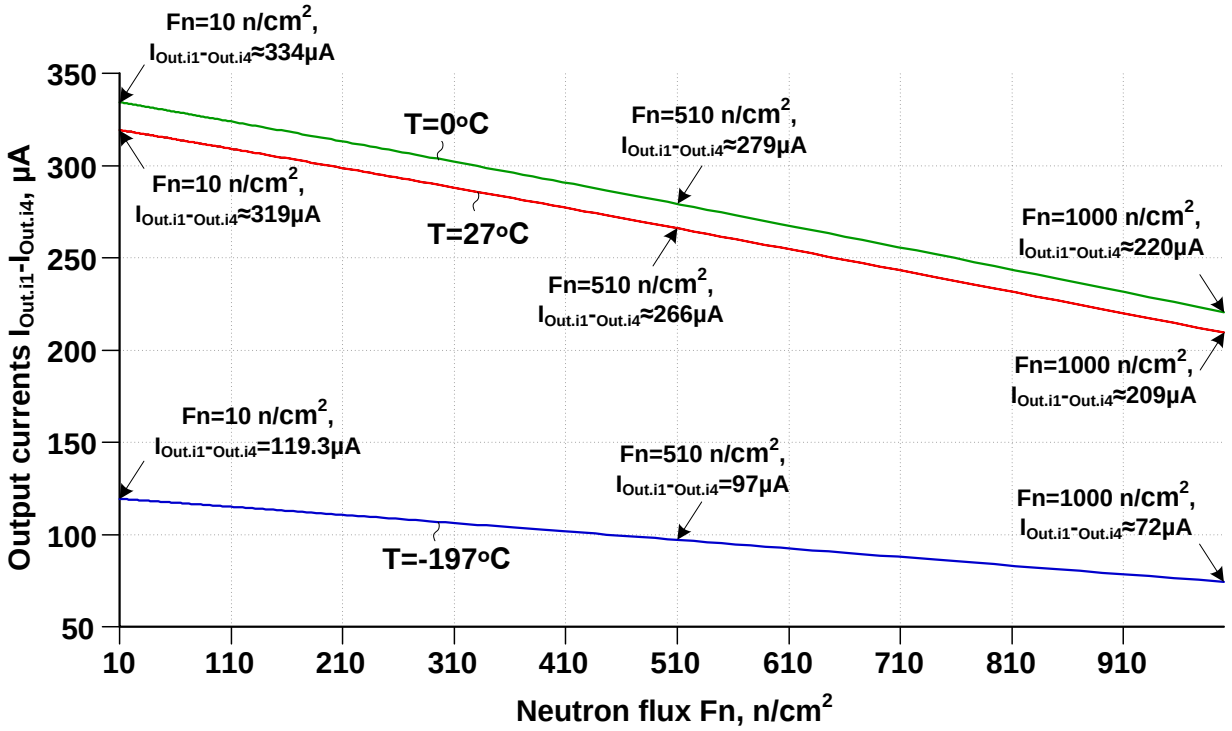

Figure 3.9 Dependence of the output currents of CJFet FS Fig. 3.7 and Fig. 3.8 on the neutron flux in the range Fn=1e13÷1e15 n / cm^2

Conclusion

The circuit design of "floating" CJFET differential stages is generalized, which is recommended for the design of analog chips with a low noise level and relatively high resistance to radiation and low temperatures. At the same time, CJFET of various microelectronic companies can be used, including CJFet of of corporation "Integral" (Minsk) and corporation "SPE" Pulsar "(Moscow).

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