 doi:10.20944/preprints202011.0447.v1

Article

Optimal IP Current Controller Design Based on Small Signal Stability for THD Reduction of High-Power Density PFC Boost Converter

Ahmed H. Okilly[1], Jeihoon Baek[1,*]

[1] Electrical & Electronics and Communication Engineering Department, Koreatech University, Cheonan-si 31253, Korea; ahmed21490@koreatech.ac.kr

* Correspondence: jhbaek@koreatech.ac.kr; Tel.: +82-41-560-1258

Abstract: This paper presents an optimal design for the inner current control loop of the continuous current conduction mode (CCM) power factor correction (PFC) stage, which it can be used as the front stage of the two stages alternating current-direct current (AC-DC) telecom power supply. Conventional single-phase CCM-PFC boost converter usually implemented with using of the proportional-integral (PI) controllers in both of the voltage and current control loops, to regulate the output DC voltage to the specified value, moreover to maintains the input current follows the input voltage which offers converter with high power factor (P.F) and low current total harmonic distortion (THD). However, due to the slow dynamic response of the PI controller at the zero-crossing point of the input supply current, input current can't fully follow the input voltage which leads to high THD. Digitally controlled PFC converter with an optimal design of the inner current control loop using doubly control loops IP controller to reduce the THD and to offer input current with unity P.F was performed in this paper. Furthermore, for the economic design of the digitally control PFC converter, two isolated AC and DC voltage sensors are proposed and designed for the interfacing with the microcontroller unit (MCU). PSIM software was used to test the converter performance with using the proposed designed current controllers and isolated voltage sensors. High power density digitally controlled telecom PFC stage with P.F of about 99.93%, full load efficiency of about 98.70% and THD less 5.50% is achieved in this work.

Keywords: CCM-PFC; small signal model; IP controller; zero-crossing point; total harmonic distortion (THD); power factor (P.F); isolated voltage sensors.

1. Introduction

Conventional AC–DC rectifiers which consists of the bridge rectifier and smoothing capacitors can be used to supply the telecom power applications, but circuit performance and fixed control parameters in such these rectifiers leads to high THD, high-power losses and reduced the conversion efficiency especially in the high-power density applications. So, the high-power factor and efficiency requirements in telecom applications limit the use of such conventional rectifiers [1]. Currently; to offer high power density efficient power supplies, the active controlled AC-DC converters with high power density based on the boost converter technique have been widely used to regulate the P.F, reducing THD, reducing the circuit power losses and increase the conversion efficiency [2,3].

The AC-DC power supply with two stages as illustrated in Figure 1 is the optimal configuration to get high values of the input P.F and power conversion efficiency. Two stages active AC–DC telecom power supply, consisting of the active power factor correction (PFC) stage, to offer input current with high power factor (P.F) and the DC–DC output converter stage, which used to regulate the bus voltage of the PFC converter stage usually (320-410) V to the distribution load level (45-63) V for the telecom applications [4].

 doi:10.20944/preprints202011.0447.v1

based on the power applications, there are more types of PFC converters which widely used, such as the Conventional PFC boost converter [5-7], the bridgeless PFC boost converter [8, 9], and the interleaved PFC boost converter [10, 11]. For telecom applications, conventional PFC boost converter is the mostly used circuit because its good performance with economic, simplest and less requirements of the power and control circuits design [1, 12], the target of this paper is to improve the performance of the telecom power supply conventional PFC stage by optimized the control technique of the boost converter controllers in order to offer converter with unity power factor by reducing the THD of the input supply current.

PFC boost converter controlling circuit can be implemented using the digital or analog techniques, controlling circuit using analog integrated circuits (IC) offers economic design of the converter, otherwise it is having some disadvantages as compared with the digital micro-controller unit (MCU) such as slow response, low operating temperature and fixed control parameters. Digital MCU offers high speed response, flexible adjustment and programming of the control techniques [13], despite all of that, the price of the measurement sensors required for the interface between the converter power circuit and DSP MCU are very expensive as compared with sensors for interfacing with the analog control IC.

Conventional PFC boost converter consisting of power and control circuits, where the power circuit contains the bridge rectifier, energy storage inductor, single switch or multiple switches connected in parallel (to increase the converter current rating), fast switching diode as well as the output bulk capacitor. The PFC boost converter control circuit usually implements with two control loops, the inner current control loop to control the inductor current which making the input current follows the input voltage and maintain the circuit power factor (P.F) at higher values, and the outer voltage loop which maintain the output voltage value as the specified load value, usually these control loops implemented using PI controllers.

For the output voltage control loop, PI controller is enough to regulate the output voltage to the specified value [14], but for the inductor current control loop, the slow response of the PI current controller at the current zero-crossing point causes distortion of the inductor current which leads to increasing the THD of the supply current [15]. Increasing of the THD in the converter circuits, causes higher power losses in all circuit components, further, it can lead to high current stresses and failures of the system insulation and protection [16]. Power quality and performance requirements required to maintain the THD value at the standard values such as IEEE 519-20142 [17], and IEC 61000-3-2 [18], which suggests that in order to improve the circuit P.F, reducing the current stresses and reducing the power losses in the system different parts, THD should be kept at the lowest value with the given standard requirements [17, 18].

Reducing of the current THD in the digitally controlled PFC boost converters can be done by using different techniques such as, the passive harmonic filters connecting in parallel with the input side, this technique can be used to reduce the THD in case of the low switching frequency PFC converters, however in case of the high frequency PFC converters where the EMI filters connecting in the input side of the converters, reliability of the passive filters to decrease the THD is very low due to the difficulty of the tuning of the filter's resonance frequency with the presence of the EMI filters [19]. Digital current filters such as finite response impulse (FIR), and infinite impulse response (IIR) filters can be optimally designed and used to moderate the feedback digital current signals for the inner current control loops to reduce the current error and hence reducing the current distortion,

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

using of the adaptive FIR filter to reduce the THD of the CCM-bridgeless PFC converter was proposed in [20].

Another widely used technique to reduce the THD in PFC converters is the variable on-time (VOT) switching control technique by optimized the duty cycle of the PFC converter to decrease zero crossing distortion (ZCD) period [20-23], VOT switching control technique is reliable to reduce the THD in PFC converter but with complex mathematical analysis of the converter operation around the zero-crossing point in order to optimize the exact dead time around the zero-crossing point for exact on-time switching prediction [24].

This paper presents the small signal stability modeling of the conventional PFC boost converter proposed, and based on the signal stability model, an optimal integral-proportional (IP) current controller consists of double loop control strategy, where the integral gain feed forward to return the inductor current back to the reference set point, and the proportional gain implemented in the feedback path to increase the controller response. IP controller usually used in the control circuits of the DC-DC converters and the DC motor drive systems [25-27], as compared with the PI controller, the IP controller have less overshoot and fast dynamic response [28]. So, IP current controller with fast dynamic response has been designed to let the inductor current track the reference current, removing the total distortion occurred around the zero-crossing point and increase the power factor. The Two different current techniques based on the conventional PI controller and the proposed IP controller have been presented in this paper and the comparative analysis based on the system stability and the controller reliability to reduce the zero-crossing current distortion was performed. Furthermore, For the economic design of the digitally controlled PFC converter, the isolated voltage sensors with low price components for interfacing with the MCU analog digital converter (ADC) has been proposed, and completely designed.

The following sections in this paper are organized as follow, section 2 explain briefly the problem of high THD in the current zero-crossing point of PFC converters and the impact of this problem on the circuit P.F. Section 3 describes the operation principle and the complete design of the PFC boost converter employed in this work. Section 4 presents the design technique of the proposed controlling circuits for the CCM-PFC converter based on the small signal stability modeling. Section 5 introduces the proposed AC and DC isolated voltage sensors for the economic and reliable operation of the digitally controlled PFC converters. Section 6 is the simulation of the complete designed converter with different control techniques. Section 7 is the conclusion and the future work.

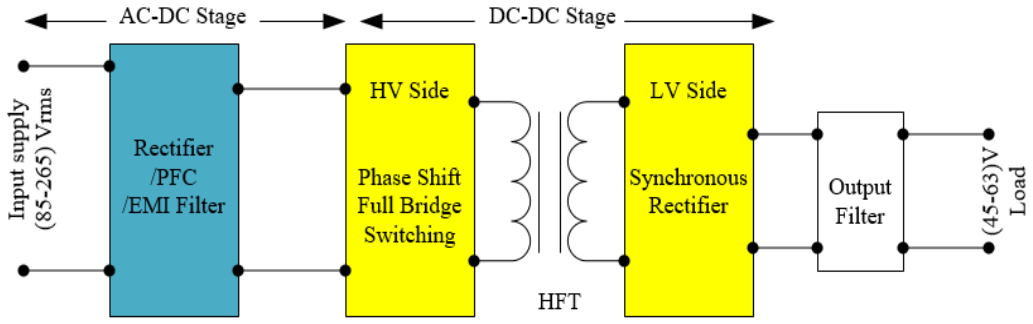

Figure 1. Block diagram of the two stages AC-DC telecom power supply.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

2. PFC Converter Total Harmonic Distortion (THD) and Power Factor (P.F)

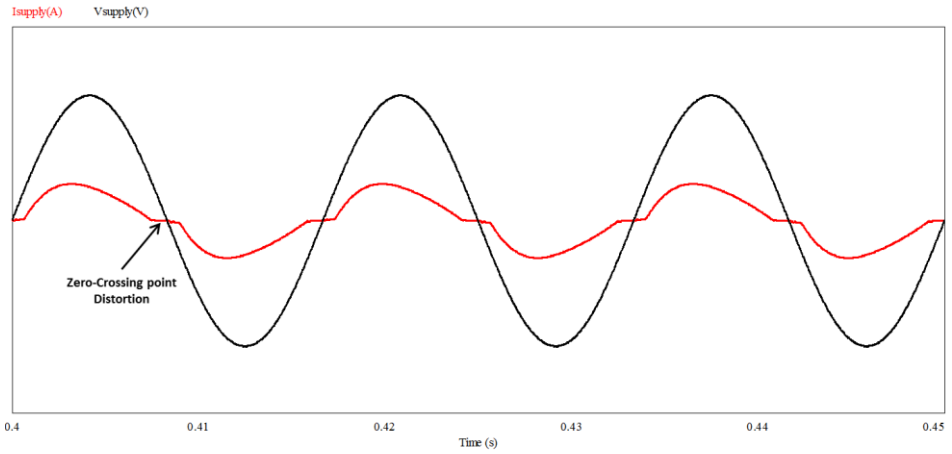

Figure 2. Supply voltage-current waveforms for PFC-boost converter with conventional PI current controller.

In power system, THD value should be keep as low as possible, lower THD offer higher power factor, higher efficiency and lower current stress in power system components due to less peak currents. Usually, THD value should follow the standard specifications such as IEC61000-3-2 or IEEE 519-20142 for different classes of equipment.

Ignoring the effect of current distortion, the input P.F of the PFC converter can be expressed as (1).

$$P.F = \cos(\theta_{vs} - \theta_{is}) \tag{1}$$

where θ_{vs} is the voltage angle and θ_{is} is current angle for the input supply.

Equation (1) is not the fully definition of the converter P.F and usually this mathematical expression called as displacement factor (d.F). Power factor calculation using (1) can be applied only if the supply voltage and current waveforms are completely sinusoidal.

In most of power electronic circuits including the PFC boost converters, operation techniques and rapidly changes between on and off states of such these converters acts as nonlinear loads which can change the nature of the current so it's no longer to be sinusoidal waveform. Figure 2 shows the supply current and voltages of the PFC boost converter, which shows the current distortion when the boost converter switch changes rapidly from on to off states, this point usually called zero crossing point. The conventional control techniques using PI controllers can't fully remove the current distortion of the input current in the zero-crossing point due to the slow dynamic response of the current controller in this point [15], where the inductor current can't track the reference current when the supply current changes rapidly from the positive to negative value.

Root mean square value of the input current (I_{s_rms}) for the PFC converter can be expressed as (2).

$$I_{s\_rms} = \sqrt{I_{dc}^2 + \sum_{n=1}^{\infty} I_{n\_rms}} \tag{2}$$

where I_{dc} is the average current component, n represents the harmonic order, and when n=1, I_{1_rms} is the fundamental component of the supply input current. With ideal voltage source which offer voltage only at the fundamental frequency ($V_{s\_rms}=V_{1\_rms}$), the converter input average power (P_{avg}) can be calculated as (3).

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

$$P_{avg} = V_{1\_rms} \times I_{1\_rms} \times D.F \tag{3}$$

Apparent power (S) which represents the supply active and reactive power components still include all of the current harmonics and can be expressed as (4).

$$S = V_{s\,rms} \times I_{s\,rms} = V_{1\_rms} \times \sqrt{I_{dc}^2 + \sum_{n=1}^{\infty} I_{n\_rms}} \tag{4}$$

From (3) and (4), the fully definition of PFC converter power factor with taken in account the current distortion can be expressed as (5).

$$P.F = \frac{I_{1\_rms}}{\sqrt{I_{dc}^2 + \sum_{n=1}^{\infty} I_{n\_rms}}} \times d.F = D.F \times d.F \tag{5}$$

where D.F represents the current distortion factor and equal to $\frac{I_{1\_rms}}{I_{s\_rms}}$.

The THD value as relating to the current distortion factor can be expressed as (6).

$$D.F = \sqrt{\frac{1}{1 + THD^2}} \tag{6}$$

So, the power factor (P.F) is the product of two factors called displacement factor (d.F) and distortion factor (D.F) as given in (5). The displacement factor (d.F) depends on the phase shift between the voltage and current of the input supply which is usually very low for the AC-DC power converters (less than 5 degree). And the distortion factor (D.F) which is depends on the total harmonic distortion of the current waveform.

For clear explanation of the relation between the P.F and THD in the PFC boost converters, for 5-degree phase shift between supply voltage and current, to get P.F more than 99% as required by almost of the telecom power applications, THD must be less than 11.20 %.

3. Telecom AC-DC PFC Boost Converter operation principle and Design

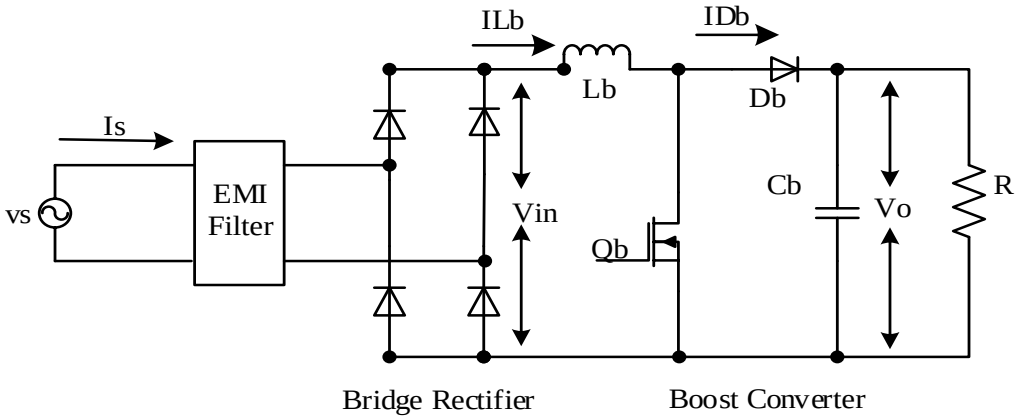

Figure 3. Schematic diagram of the conventional AC-DC PFC boost converter.

Figure 3. shows the schematic circuit of the PFC boost converter which usually consists of the electro-magnetic interface (EMI) filter connected to the AC input power source, bridge rectifier and

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

the boost converter unit which represents the main part of the PFC boost converter. The boost converter employed in this article works in current continuous conduction mode (CCM), this topology is the conventional and the most used topology in the most of the telecom applications due to it is simplest design, reliability at higher power applications and economic price as compared with the other PFC topologies [1, 12]. Boost converter unit consists of three main parts, the storage energy part which represents by inductor (L_b), the switching elements represents by high voltage switch (Q_b), high-speed switching diode (D_b), and the output filtering capacitor C_b.

The following section presents the operation principle and the design of the main components of the single-phase CCM- boost converter.

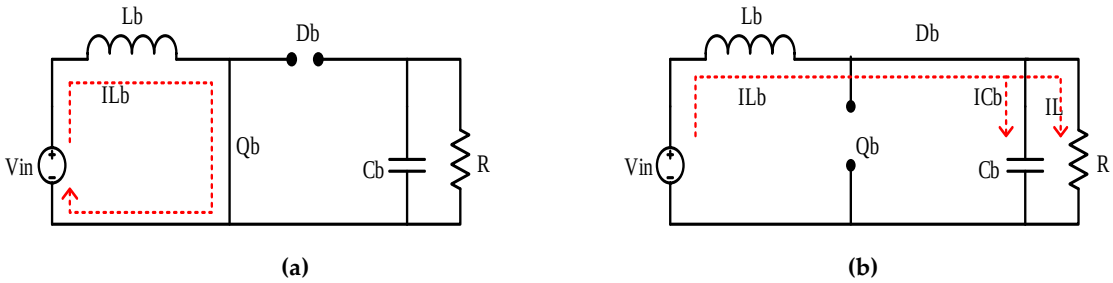

Figure 4. CCM-boost converter operation modes. (a) Switch Q_b closed, (b) Switch Q_b opened.

Figure 4 depicts the schematic circuits of the different operation modes for the CCM-boost converter. When the switch (Q_b) is closed as shown in Figure 4.a, the current will flow through the energy storage element (L_b) in the direction marked in the red dotted line, at this moment the energy will be storage in the inductor generating magnetic field, and when Q_b is opened, as shown in Figure 4.b, the current circuit impedance will be increased leads to the current reducing, and the magnetic field previously created, will be reduced to maintain the current towards the load as marked also in the red dotted line. Thus, the polarity of the inductor voltage will be reversed, which make two sources in series causing a higher voltage to charge the capacitor (C_b) through the high-speed switching diode (D_b).

The three parts of the boost converter should be optimally designed in order to maintain the circuit specified ripple currents, reduce the voltage stress in the switching elements during the converter operation and to maintain the output voltage with the specified ripple value required by the telecom applications.

PFC boost converter inductor (L_b) is designed based on the specified circuit ripple current (%Ripple) and the corresponding input and output voltage conditions [29]. PFC control circuits is usually designed to offer good performance with wide range of the input AC voltage (85-265) V, with using these specifications of the design, L_b value can be calculated as (7).

$$L_b = \frac{1}{\%Ripple} \times \frac{1}{\eta} \times \frac{v_{s\,min}^2}{P_o}\left(1 - \frac{\sqrt{2}\, v_{s\,min}}{V_o}\right)\frac{1}{Fsw} \tag{7}$$

Also, the inductor maximum current ($I_{Lb\,Max}$) is determined based on the specified maximum current ripple[29] as expressed in (8).

$$I_{Lb\,Max} = \frac{\sqrt{2}\, P_O}{v_{s\,min}} \times \left(1 + \frac{\%Ripple}{2}\right) \tag{8}$$

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

where $V_{s\,min}$ is the minimum supply voltage in root mean square (RMS) value, V_o is the rated output DC voltage, η is the converter designed efficiency, P_o is the output rated power and F_{sw} is the switching frequency.

The output filter capacitor, usually called as the output bulk capacitor is designed to meet the specified output voltage ripple at the supply frequency requirements using (9).

$$C_o \geq \frac{P_o}{2 * \pi * F * V_{rpp} * V_o} \tag{9}$$

where F is the input supply frequency, V_{rpp} is the output voltage ripple peak to peak value.

also, the Bulk output capacitor should be designed to offer the minimum voltage hold up with the specified time (t_{hold}) as expressed in (10).

$$C_o \geq \frac{2 * P_o * t_{hold}}{V_o^2 - V_{o\,min}^2} \tag{10}$$

The capacitor value is selected to have the larger value among the two equations.

Another important issue at the choosing of the output bulk capacitor, the capacitor series equivalent resistance (ESR) should be very low, which it is effects in circuit efficiency and the output voltage regulations. Also, higher ESR causes more ripple, influencing stability of the control loops [25]. Table 1 shows the designed specification and results for the 2500 W PFC boost converter employed in this work.

Table 1. Telecom CCM-PFC converter design specifications and components value.

Parameter	Specification	Unit
AC Input voltage (V_s)	220 (85-265)	V rms
AC Input frequency (F)	60 (47-63)	Hz
DC output voltage (V_o)	400 (320-410)	V
Rated power (P_{out})	2500	W
Switching frequency (F_{sw})	100	kHz
Input ripple current (%Ripple)	10%	at full load
output ripple voltage (V_{rpp})	20	$V_{\_peak\ to\ peak}$
Hold up time (t_{hold})	6	ms
Output capacitor (C_o)	1120	uF
Boost converter inductor (L_b)	470	uH

4. Design of the proposed PFC boost Converter Control systems

A block diagram of the complete schematic circuit of the telecom CCM-PFC converter including the digitally controlled technique is shown in Figure 5. CCM-PFC control circuit include two control loops implemented inside the DSP MCU as implemented in Figure 6, the outer voltage control loop and the inner current control loop.

The outer loop is used for regulating the output voltage (V_o) of the PFC converter to the reference value and also to generate the voltage error signal which is modified with the input sinusoidal voltage (V_{in}) to generate the reference current (I_{ref}) value for the inner control loop as depicted in the control blocks in Figure 6. The inner loop is used to make the inductor current (I_{Lb}) track the refence current (I_{ref}), inductor current is the DC value of the input supply current, so that any distortion in the inductor current will affect in the sinusoidal shape of the input supply current.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

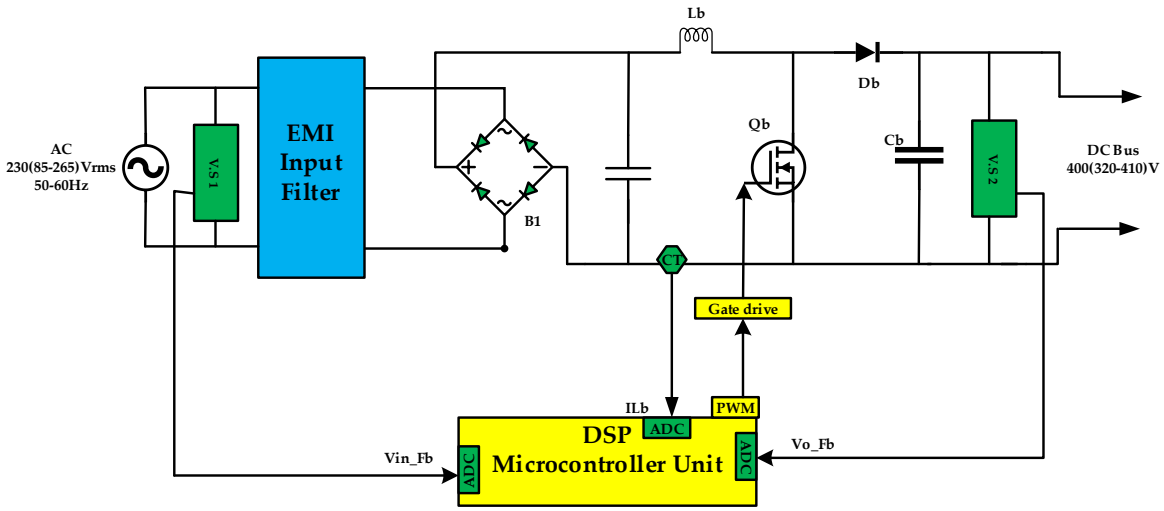

Figure 5. AC-DC telecom PFC boost converter with digitally controlled technique.

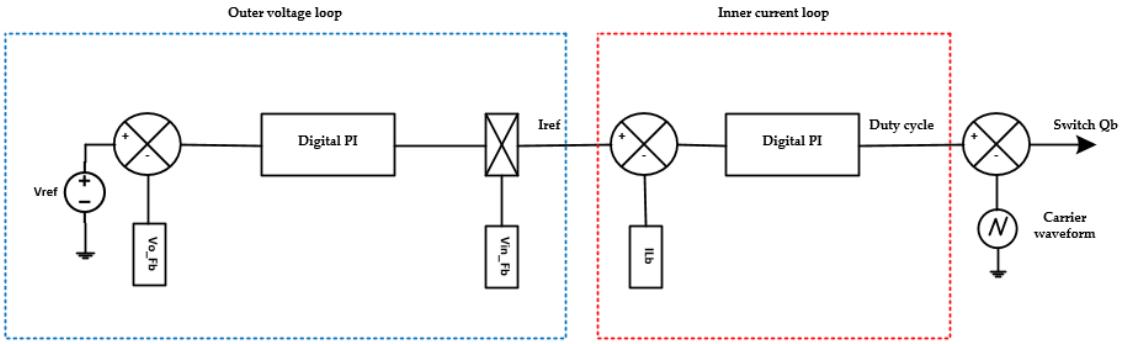

Figure 6. Implementation technique of the controlling circuit inside the DSP.

Usually the PI controller is enough to regulate the output voltage to the reference limit with good performance and fast response [14], so in the conventional and the proposed control circuits, the same PI controller has been used in the voltage control loop.

4.1 PFC Boost Converter Average Small Signal Modelling

For the PFC boost converter shown in Figure 3, the inductor voltage (V_{Lb}) can be expressed as (11).

$$V_{Lb} = L_b \frac{dI_{Lb}}{dt} = V_{in} - V_o(1 - D) \tag{11}$$

The output capacitor current (I_{Cb}) can be expressed as (12).

$$I_{Cb} = C_b \frac{dV_o}{dt} = -\frac{V_o}{R} + I_L(1 - D) \tag{12}$$

where D refers to the converter duty cycle, V_o is the output bus voltage (V_o=V_{bus}), and R is the load resistance in ohm.

Assume all variables $(\mathbf{I_{Lb}, V_{in}, V_o \text{ and } D})$ at the steady state values in the selected operational point$(\mathbf{i_{Lb}, v_{in}, v_o \text{ and } d})$ and small signal AC variation $(\mathbf{i^*_{Lb}, v^*_{in}, v^*_o \text{ and } d^*})$ where:

$$I_{Lb} = i_{Lb} + i^*_{Lb}\ ;\ V_{in} = v_{in} + v^*_{in}\ ;\ V_o = v_o + v^*_o\ ;\ D = d + d^* \tag{13}$$

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

The PFC boost converter control circuit shown in Figure 6 should modify the duty cycle (D) based on the small signal AC variation to control the output voltage (V_o) and the inductor current (I_{Lb}).

Substituting from (13) in (11) and (12).

$$L_b \frac{d(i_{Lb}+i^*_{Lb})}{dt} = (v_{in} + v^*_{in}) - (v_o + v^*_o)\,(1 - d - d^*) \tag{14}$$

$$C_b \frac{d(v_o + v^*_o)}{dt} = -\frac{(v_o + v^*_o)}{R} + I_{load}(1 - d - d^*) \tag{15}$$

Equations (14) and (15) can be re-written again as given in (16) and (17) with neglecting the term $\mathbf{v^*_o d^*}$ which it is the result of the product of two AC small signals.

$$L_b \frac{d(i^*_{Lb})}{dt} = (v^*_{in}) - (v^*_o)\,(1 - d) + v_o\,.\,d^* \tag{16}$$

$$C_b \frac{d(v^*_o)}{dt} = -\frac{v^*_o}{R} + I_{Lb}\,.\,d^* + (i^*_{Lb})(1 - d) \tag{17}$$

Using the Laplace transform to get the small signal model, and arranging the model in state space matrixes form as given in (18).

$$\begin{bmatrix} sL_b & 1-d \\ 1-d & -sC_b - \frac{1}{R} \end{bmatrix} \begin{bmatrix} i^*_{Lb}(s) \\ v^*_o(s) \end{bmatrix} = \begin{bmatrix} v_o \\ i_{Lb} \end{bmatrix} . d^*(s) + \begin{bmatrix} 1 \\ 0 \end{bmatrix} . v^*_{in}(s) \tag{18}$$

With using of the derived model of the PFC boost converter and selecting the appropriate system stability criterions which enhance the system stability and power quality improvement, the two control loops of the PFC boost converter can be designed as discuss in the following subsections.

4.2 Design of the Outer Voltage Loop

The design of the outer voltage control loop starts with obtaining the transfer function (T.F) of the outer voltage circuit by using the small signal stability modeling of the boost converter which describe the operation of the converter in the steady state operation point. For the boost converter shown in Figure 3.

$$\frac{V_o}{V_{in}} = \frac{1}{1 - D} \tag{19}$$

$$1 - D = \frac{|v_s|\sin(\omega t)}{V_o} \tag{20}$$

Boost converter inductor current ($\mathbf{I_{Lb}}$) and diode current ($\mathbf{I_{Db}}$) can be expressed as (21) and (22) respectively.

$$I_{Lb} = |i_{Lb}|\sin(\omega t) \tag{21}$$

$$I_{Db} = I_{Lb}.(1 - D) \tag{22}$$

Substituting from (19, 20 and 21) in (22), the boost converter diode current ($\mathbf{I_{Db}}$) complete equation can be written as (23).

$$I_{Db} = |i_{Lb}|\sin(\omega t).\frac{|v_s|\sin(\omega t)}{V_o} = \frac{|i_{Lb}||v_s|\sin^2(\omega t)}{V_o} = \frac{1}{2}\,\frac{|i_{Lb}||v_s|}{V_o} - \frac{1}{2}\,\frac{|i_{Lb}||v_s|}{V_o}\cos(2\omega t) \tag{23}$$

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

where the term $\frac{1}{2}\frac{|i_{Lb}||v_s|}{V_o}$ is refers to the DC component and the term $\frac{1}{2}\frac{|i_{Lb}||v_s|}{V_o}\cos(2\omega t)$ is refers to the AC component of the diode current.

Applying the averaged small signal perturbation to (23) gives the expression in (24).

$$i^*_{Db} = \frac{1}{2}\frac{|v_s| \, . \, i^*_{Lb}}{V_o} + \frac{v^*_o \, . \, I_{Db}}{V_o} \tag{24}$$

Diode current is the sum of two components, load current ($\mathbf{I_{load}}$) and the output capacitor current ($\mathbf{I_{Cb}}$), which it can expressed as (25).

$$I_{Db} = I_{load} + I_{Cb} \; = I_{cb} + \frac{V_o}{R} \tag{25}$$

Applying the averaged small signal perturbation to (25) with the resistive load case give expression in (26).

$$i^*_{Db} = v^*_o C_b s + \frac{v^*_o \, . \, I_{Db}}{V_o} \tag{26}$$

With Comparing between the right-hand side parts of (24) and (26):

$$\frac{1}{2}\frac{|v_s| \, . \, i^*_{Lb}}{V_o} = v^*_o C_b s \tag{27}$$

So, the open loop T.F of the outer voltage system is given as (28).

$$G_v(s) = \frac{v^*_o(s)}{i^*_{Lb}(s)} = \frac{|v_s|}{2 \, V_o \, C_b s} \tag{28}$$

Figure 7 shows the control blocks for the outer voltage control loop of the PFC boost converter using the PI controller.

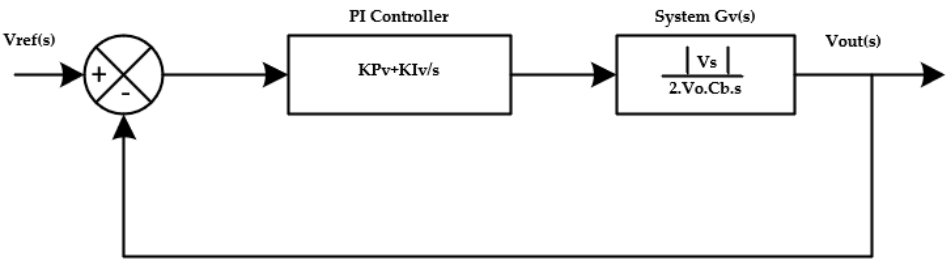

Figure 7. Block diagram of the outer voltage control loop using the PI controller.

PI controller system can be described using the following T.F.

$$G_{PIv}(s) = K_{Pv} + \frac{K_{Iv}}{s} \tag{29}$$

where K_{Pv} is the proportional gain, K_{Iv} is the integral gain of the PI controller?

The closed loop T.F of the outer voltage control loop system ($G_{CLV}(s)$) can be obtained as (30).

$$G_{CLv}(s) = \frac{G_v(s) \, . \, G_{PIv}(s)}{1 + G_v(s) \, . \, G_{PIv}(s)} \tag{30}$$

by substituting from (28) and (29) in (30) gives the closed loop T.F of the outer voltage control loop as expressed in (31).

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

$$G_{CLv}(s) = \frac{\frac{|v_s|}{2\,V_o\,C_b}.(K_{Pv}\,s + K_{Iv})}{s^2 + \frac{|v_s|\,K_{Pv}}{2\,V_o\,C_b}s + \frac{|v_s|\,.K_{Iv}}{2\,V_o\,C_b}} \quad (31)$$

So, the PI controller gains K_{Pv}, K_{Iv} can be designed using (31) and the standard form of the second order system T.F, by selecting the optimal stability criteria for the control system bandwidth and undamped natural frequency. Usually the bandwidth of the outer voltage loop must be very small to eliminate the harmonic of the DC-bus voltage reflected by the AC input voltage at 60 Hz [8].

In this work, the closed loop bandwidth of the outer voltage loop is assumed to be about W_n=85 rad/sec, the undamped natural frequency is about ξ=0.707, and for the reliable operation of the controller with the wide loading range, the PI controller parameters are sets to work with the minimum value of the load voltage V_o=320 V with the rated input supply voltage V_s=220 V_{rms}.

with using these values, the closed loop T.F of the outer voltage control loop finally can be expressed as (32).

$$G_{CLv}(s) = \frac{276.23\,K_{Pv}\,s + 276.23K_{Iv}}{s^2 + 276.23\,K_{Pv}\,s + 276.23K_{Iv}} \quad (32)$$

Figure 8 shows the bode plot of the closed loop T.F of the outer voltage control loop, which shows that the controller offer unity gain for frequencies less than 27.8 Hz, this voltage control system working as a low pass filter helps to remove the 60 Hz voltage ripple.

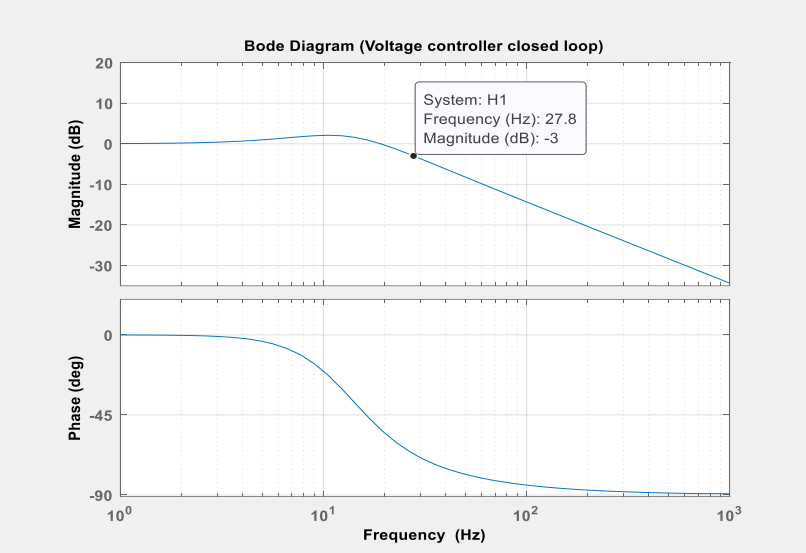

Figure 8. Bode plot of the closed loop outer voltage control system.

And the optimal PI controller T.F designed for the outer voltage control loop can be expressed as (33).

$$G_{PIv}(s) = 0.435 + \frac{26.55}{s} \quad (33)$$

In order to check the stability of the designed control voltage loop, root locus of the closed loop T.F was plotted as shown in Figure 9, which shows that the closed loop eigenvalues were located in the negative side of the pole zero plane, so the closed loop voltage system is inherently stable.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

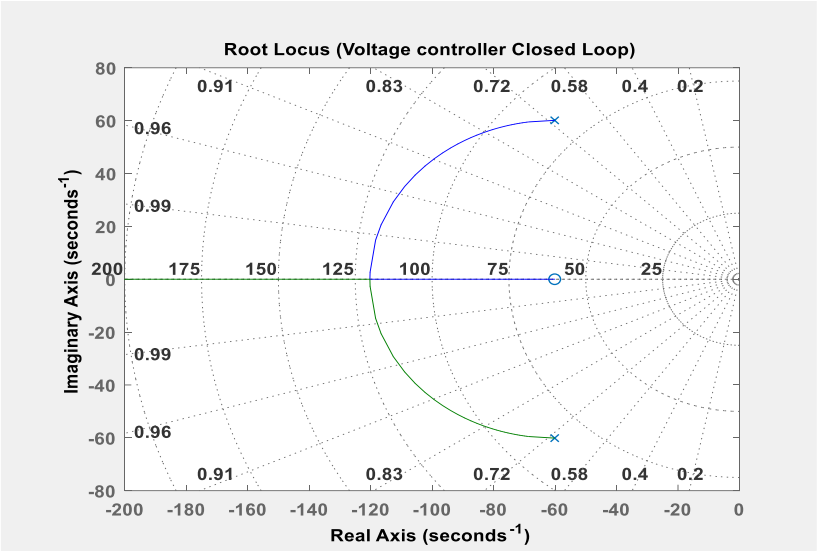

Figure 9. Root locus of the closed loop T.F of the outer voltage control system.

4.3 Design of the Inner Current Control Loop

Design procedure of the inner current control loop have been performed by the same way of the voltage controlling design and with an appropriate stability criterion for the inner current control loop. The inner current-control loop must have enough bandwidth higher than outer voltage loop bandwidth so that it be fast enough to track the current changes (to let the inductor current track the reference current), nevertheless, the current control loop bandwidth must be less than switching frequency (F_{sw}) to reject the noise at the switching frequency.

Using the small signal model of the boost converter obtained in (18), the open loop T.F of the inductor current control system $G_i(s)$ can be expressed as (34).

$$G_i(s) = \frac{i^*_{Lb}(s)}{d^*(s)} = \frac{2V_o}{R(1-D)^2} \cdot \frac{1 + \frac{sRC_b}{2}}{1 + \frac{sL_b}{R(1-D)^2} + \frac{s^2L_bC_b}{(1-D)^2}} \tag{34}$$

After rearranging (34) , the open loop T.F of the inductor current system can be written as (35).

$$G_i(s) = \frac{\left(\frac{V_o}{L_bC_bR}\right).(sRC_b + 2)}{s^2 + \frac{1}{C_bR}s + \frac{1}{L_bC_b}(1-D)^2} \tag{35}$$

From (35) it is observed that the stability of the inductor current system is depending on the converter duty cycle (D), in this work the PFC boost converter has been designed to obtain a constant output voltage with a wide range of the input voltage (85-265 Vac), based on these operating conditions, minimum duty cycle of the converter is considered about 0.40 and maximum duty cycle of about 0.95.

Before starting the design of the controller for the inner current control loop, the inductor current system stability checked with using Root locus stability plotted as shown in Figure 10 for the minimum and maximum converter duty cycle. Which shows that at D_{min}=0.40, the open loop roots $r_{1,2}$ = -6.97± 826.82i, and at D_{max}=0.95, $r_{1,2}$ = -6.97+68.55i. Also, with the different duty cycle from 0.4 to 0.95 the real part of the roots is usually negative and at constant value about (-6.97) and only the imaginary parts are changing with the different values of the converter duty cycle in which that the current system of the CCM-PFC converter is absolute stable in open loop with the operating range of the converter duty cycle (D).

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

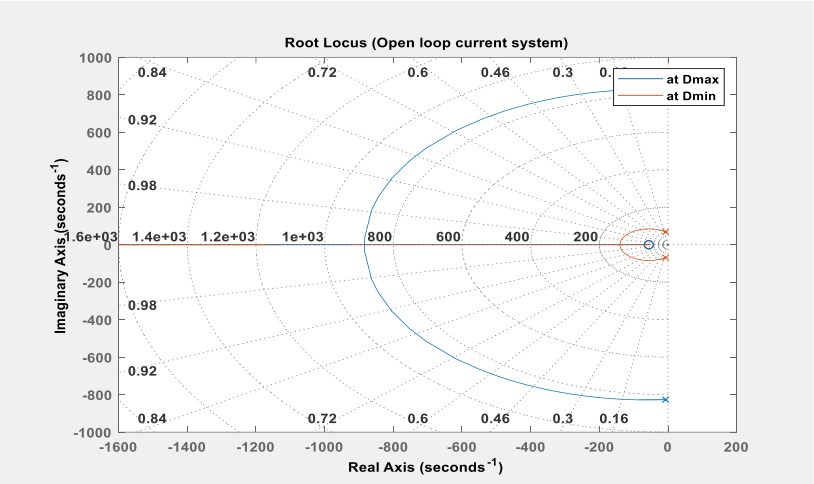

Figure 10. Root locus plot of the open loop current system with different duty cycle.

Figure 11 shows the bode plot of the Open loop of the inductor current system. Which it can notice that, the peak resonance frequency is proportionally with the duty cycle value, also the converter high bandwidth available with high duty cycle of the converter.

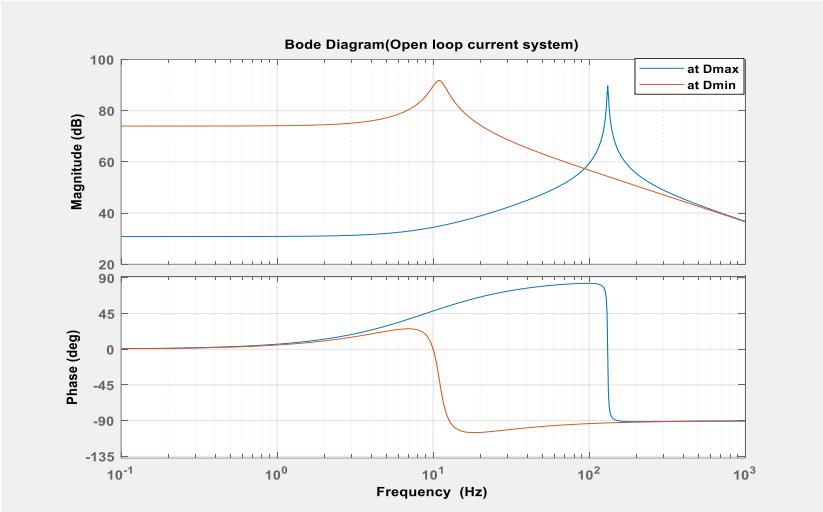

Figure 11. Bode plot of the open loop current system with different duty cycle.

Figure 12 depicted the block diagram of the inner current control loop with using the PI controller, the T.F of the closed loop current control loop can be expressed as (36).

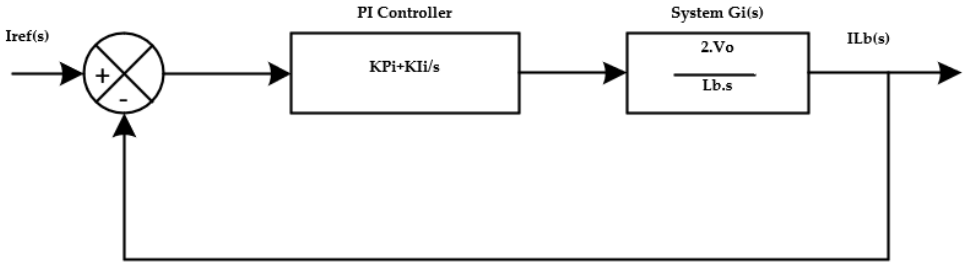

Figure 12. Block diagram of the inner current control system with PI controller.

$$G_{CLI}(s) = \frac{I_{Lb}(s)}{I_{ref}(s)} = \frac{G_i(s) \,.\, G_{PIi}(s)}{1 + G_i(s) \,.\, G_{PIi}(s)} \tag{36}$$

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

The T.F of the PI current controller ($G_{PIi}(s)$) can be expressed as (37).

$$G_{PIi}(s) = K_{Pi} + \frac{K_{Ii}}{s} \tag{37}$$

where K_{Pi}, K_{Ii} are the proportional and integral gains for the PI current controller respectively.

Since the converter switching frequency is selected about F_{sw}=100 kHz in this work, so for high frequency analysis, the capacitor can be shorted, and the open loop T.F of the inductor current system in (35) can be simplify as expressed in (38).

$$G_i(s) = \frac{2\,V_o}{sL_b} \tag{38}$$

Substituting from (37) and (38) in (36), the closed loop T.F for the inner current control system can be derived as (39).

$$G_{CLI}(s) = \frac{2\,V_o\,K_{Pi}\,s + 2\,V_o K_{Ii}}{s^2 L_b + 2\,V_o\,K_{Pi}\,s + 2\,V_o K_{Ii}} \tag{39}$$

with using of the same converter operating conditions of the voltage and power which used in the voltage loop controller design and with high bandwidth of about 5000 rad/sec for the inner current control loop, the closed loop T.F of the inner current control loop can be expressed as (40).

$$G_{CLI}(s) = \frac{(1.36 * 10^6)\,K_{Pi}s + (1.36 * 10^6)K_{Ii}}{s^2 + (1.36 * 10^6)K_{Pi}\,s + (1.36 * 10^6)K_{Ii}} \tag{40}$$

Figure 13 shows the Bode plot of the closed loop T.F of the current control loop, which shows that the controller offer unity gain for frequencies less than 1610 Hz, this current control system working also as a low pass filter helps to remove the switching frequency noise.

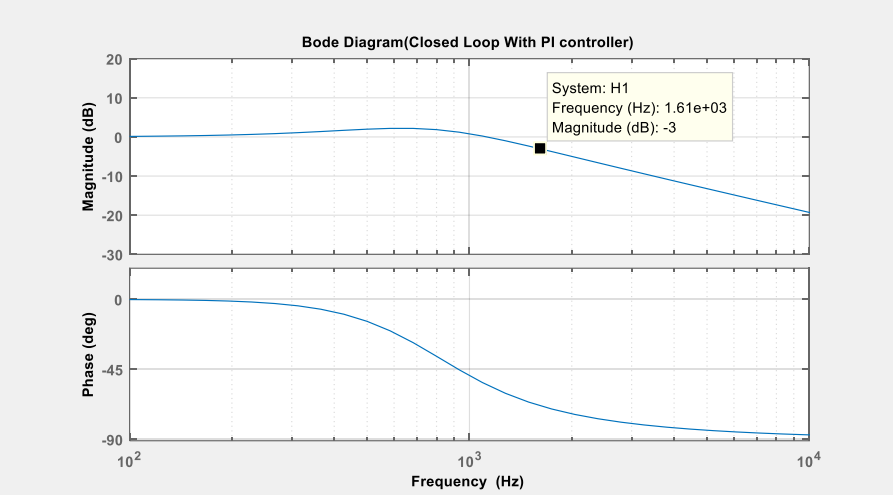

Figure 11. Bode plot of the current controller closed loop T.F with PI controller.

And the optimal PI controller transfer function designed for the inner voltage control loop can be expressed as (41).

$$G_{PIv}(s) = 0.005 + \frac{18.40}{s} \tag{41}$$

Figure 14 shows that the eigenvalues of the closed loop current controller were located at the negative side of the pole zero plane, which ensures that the current control system has absolute stability.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

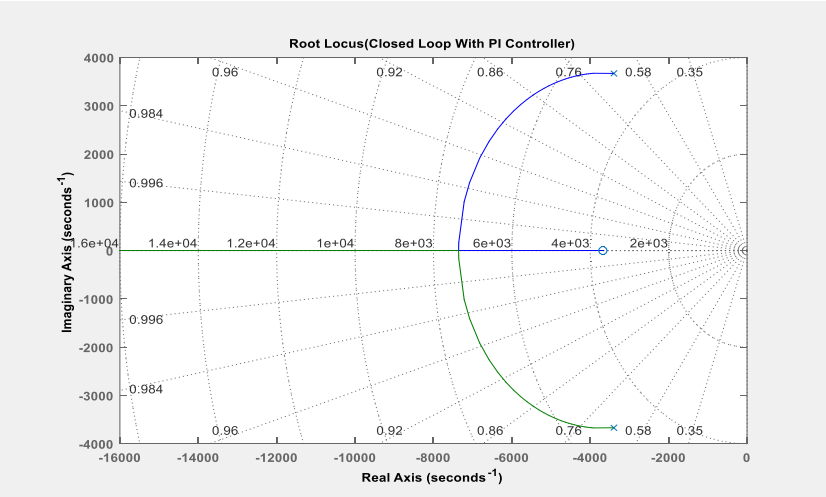

Figure 14. Root locus of the closed loop T.F of the inner current control loop.

The IP controller characterized with high dynamic response, less overshoot as compared with the PI controller. So, an optimal IP controller has been proposed and designed in this section to replace the PI in the inner current control loop in order to eliminate the current distortion around the zero-crossing point.

Figure 15 depicted the block diagram of the inner current control system with using the IP controller consisting of two control loops instead of one in case of the PI controller, where the integral gain feed in forward and the proportional gain feed backward.

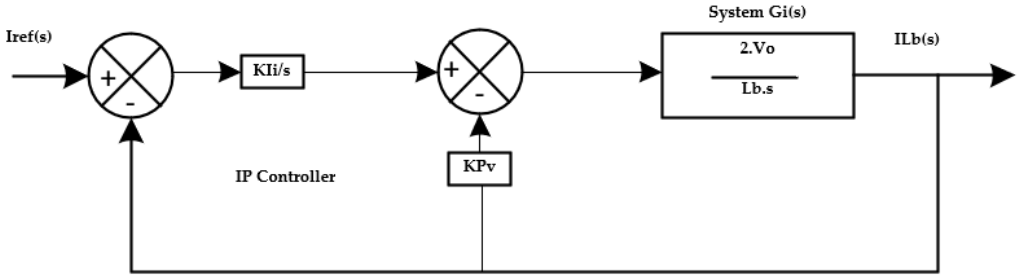

Figure 15. Block diagram of the inner current control system with the proposed IP controller.

From the block diagram in Figure 8, equation (42) can be derived.

$$I_{Lb} = \left[(I_{ref} - I_{Lb})\frac{K_{Ii}}{s} - I_{Lb}K_{Pi}\right]\left[\frac{2\,V_o}{L_b\,s}\right] \tag{42}$$

After rearranging (42).

$$I_{Lb}\left[\frac{2\,V_o}{L_b\,s}\left(\frac{K_{Ii}}{s} + K_{Pi}\right) + 1\right] = I_{ref}\left(\frac{2\,V_o\,K_{Ii}}{L_b\,s^2}\right) \tag{43}$$

The closed loop T.F of the inner current control loop using the IP controller can be expressed as (44).

$$G_{CLI}(s) = \frac{I_{Lb}(s)}{I_{ref}(s)} = \frac{\frac{2\,V_o\,K_{Ii}}{L_b\,s^2}}{\frac{2\,V_o}{L_b\,s}\left(\frac{K_{Ii}}{s} + K_{Pi}\right) + 1} = \frac{2\,V_o K_{Ii}}{s^2 L_b + 2\,V_o\,K_{Pi}\,s + 2\,V_o K_{Ii}} \tag{44}$$

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

The problem of the slow response of the inductor current to track the reference current can be solved by using the IP controller in the inner current control loop. Since, this controller structure provide two control loops for the current control system not only one as in case of the PI controller, which provide reliable and exact tracking of the inductor current to the reference current. Also, as shown in (44) there is no zero in the T.F using of the IP controller as compared with the T.F in (39) with the PI controller, which also provides system response with less overshoot.

To perform the comparative study between the PI and IP controllers based on the reliability to reduce the current distortion around the zero-crossing point, IP controller parameters were designed with the same operating condition and system stability criteria which used in the design of the PI controller. Therefore, the closed loop T.F of the inner current control loop with using the IP controller can be expressed as (45).

$$G_{CLI}(s) = \frac{(1.36 * 10^6)K_{Ii}}{s^2 + (1.36 * 10^6)K_{Pi}\, s + (1.36 * 10^6)K_{Ii}} \tag{45}$$

Figure 16 shows the Bode plot of the closed loop T.F of the current control loop with the IP controller, which shows that the controller offers unity gain for frequencies less than 823 Hz, this current control system with the IP controller also works as a low pass filter which helps to remove the switching frequency noise. Also, eigenvalues of the PI and IP controller are the same which shows that the closed loop T.F of the current controller with the IP controller is also stable as in case of the PI controller.

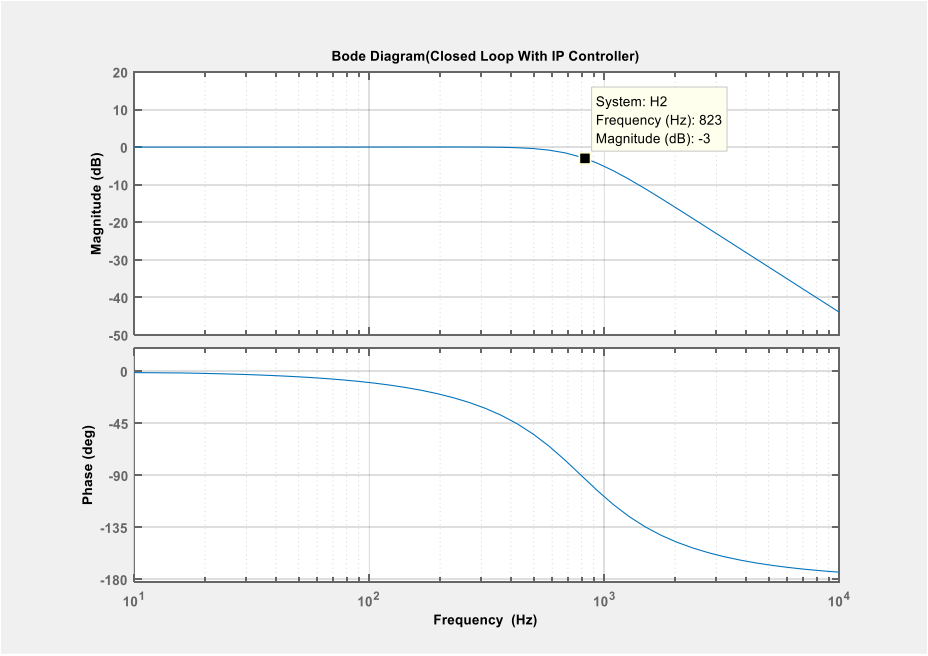

Figure 16. Bode plot of the current controller closed loop T.F with proposed IP controller.

Figure 17 shows the bode plot of the closed loop T.F using the PI and IP controllers, which can notice that the overshoot using the PI controller was eliminated in case of the IP controller, also Figure 18 shows the step response with using the both controllers, overshoot of the current controller due to input step response was reduced from 21.7% with PI controller to 5.40% with using the proposed IP controller.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

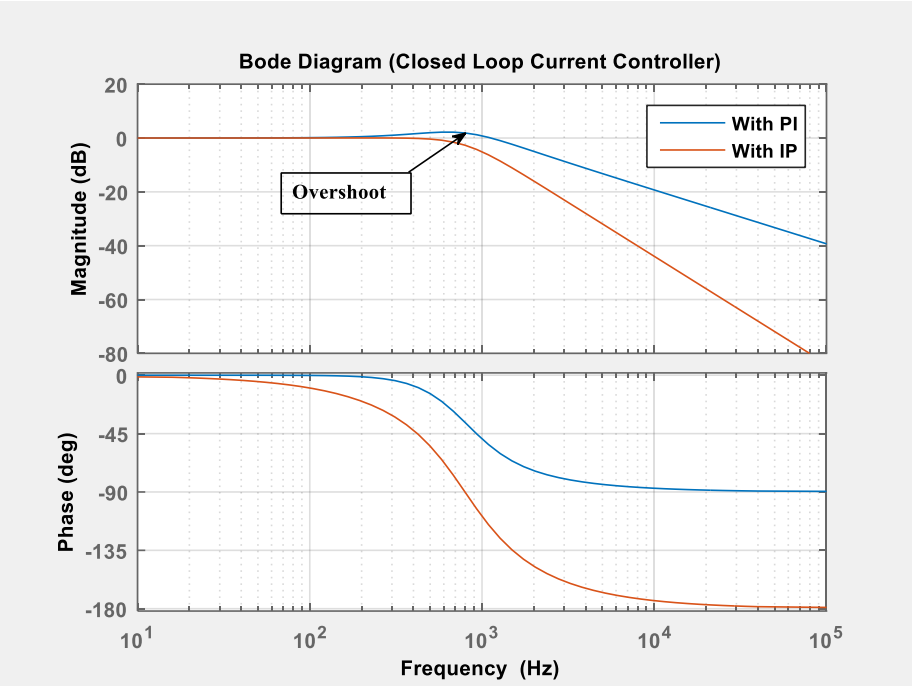

Figure 17. Block diagram of the inner current control loop with different controllers.

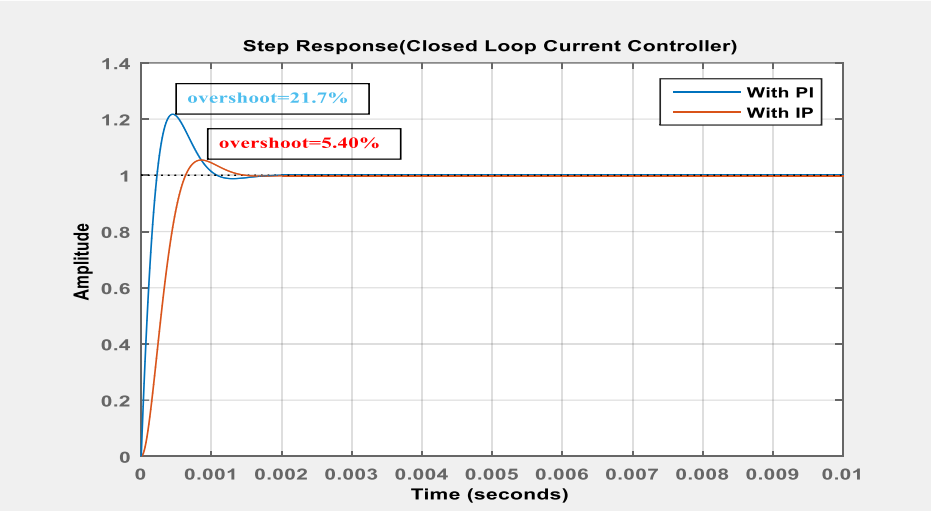

Figure 18. Step response of the inner current control loop with different controllers.

5. Design and Implementation of the Isolated voltage Sensors

As mentioned before in the introduction part, one of the disadvantages of the digitally controlled PFC converter is that the voltage and current sensors which required for the interfacing with the MCU is very expensive, in this section for economic and reliable operation of the designed digitally controlled PFC converter, two voltage sensors for sensing the AC input and the DC output voltage of the PFC converter were proposed to interface with the DSP TMS320F28335 from Texas instruments.

Figure 19 shows the schematic circuit of the proposed isolated DC voltage sensor, For the DSP TMS320F28335 [31], the input voltage range to analog digital converter (ADC) range is 0 to 3 V DC voltage. So, the voltage sensors should be designed to convert the measured DC output voltage of the PFC converter to be in the available input range of the ADC of the DSP MCU.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

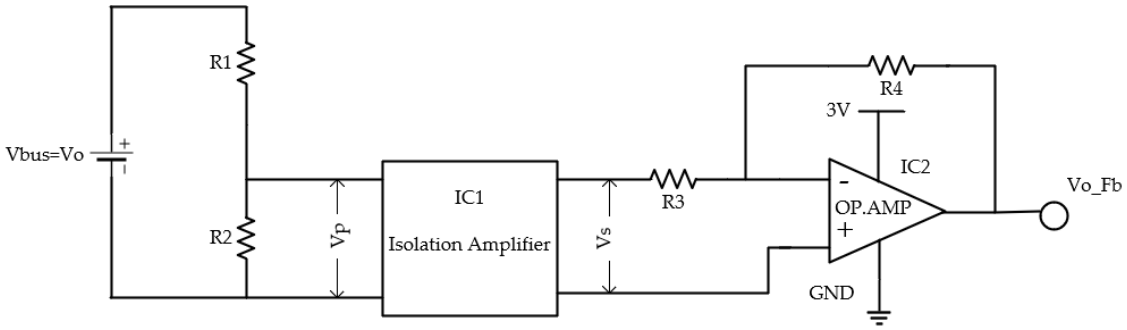

Figure 19. Block diagram of the proposed isolated DC voltage sensor (V.S 2).

The proposed voltage sensor consists of two stages, the first stage is implemented using the voltage dividers R_1, R_2 and the isolation amplifier (IC_1) to offer isolation between the high voltage power circuit and the low voltage control circuit. The second stage is the operational amplifier (IC_2) circuit which used to adjust the sensor voltage to the required value based on its operation mode.

From the gain of the chosen isolation amplifier (IC_1) in the first stage, the value of resistors R_1 and R_2 can be designed as (45).

$$V_{bus\_Max} = V_{p\_Max} \cdot \frac{R_2}{R_1 + R_2} \tag{45}$$

where V_{p_Max} is the maximum primary voltage of the isolation amplifier and can be easily known from the datasheet of the chosen isolation amplifier (IC1), and then by choose the value of R_1, the value of R_2 can be easily calculated from (45). AMC1311 isolation amplifier from TI with primary voltage range about 2 V and unity voltage gain was used in the designed sensor which provides galvanic isolation up to 7 kV, low offset error, very low nonlinearity less than 0.03% with cheap price (about 3 $) which provide high reliability and economic design of the Isolated voltage sensing [32].

Operational amplifier should be chosen to offer wide bandwidth and low slew rate time and low noise. OPA320 operational amplifier from TI was used in this work with wide bandwidth more than 20 MHz and low slew rate time to the output voltage about 10V/us with cheap price (about 2.5 $) [33] and the expected total price of the proposed sensor will be not more than 10 $, this price is very cheap as compared with the other sensor types such as LV25-P sensor with price about 80 $ which used for the voltage sensing in reference[8].

The operational amplifier implemented in proposed sensor works in the inverting mode, so the closed loop voltage gain (β) can be expressed as (47).

$$\beta = \left| \frac{V_{o\_Fb}}{V_{s\_Max}} \right| = \frac{R_4}{R_3} \tag{47}$$

where V_{s_Max} is the maximum secondary voltage of the isolation amplifier and can be calculated using (48).

$$V_{s\_Max} = V_{p\_Max} \cdot \alpha \tag{48}$$

where α is the isolation amplifier voltage gain.

with choose of R_3 value, the value of the resistance R_4 can be easily calculated from (47).

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

Figure 20 shows the input output voltage curves for the designed isolated voltage sensor, which shows that for the input voltage of 400 V DC, the output voltage level is limited from 0 to 3 V with very small slew rate time about 25 us.

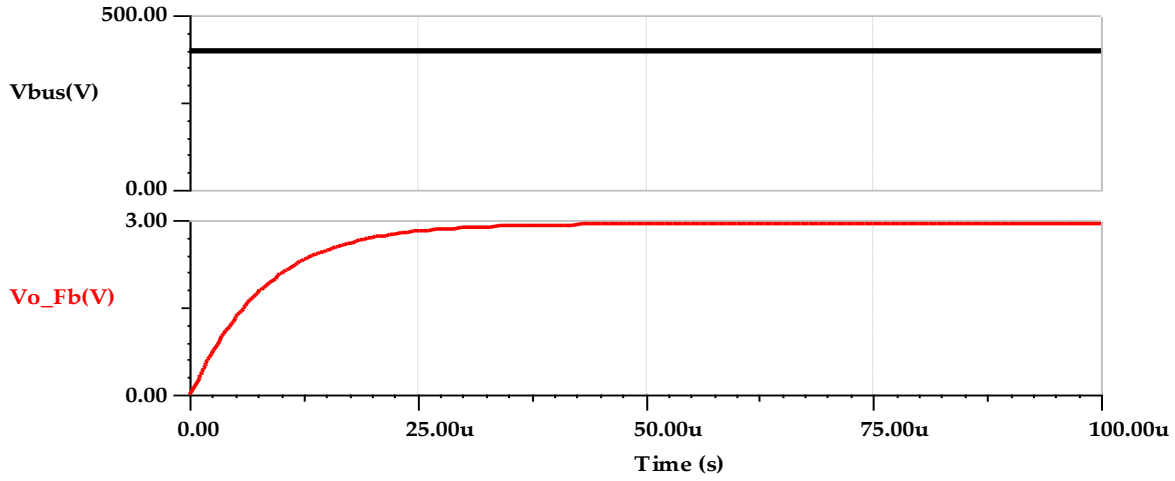

Figure 20. Isolated DC voltage sensor voltage curves with input voltage of 400 VDC.

Figure 21 shows the schematic circuit of the proposed isolated AC voltage sensor. By the same steps of the DC voltage sensor design, the AC isolated voltage sensor has been designed and the offset voltage (V_{offset}) was used to remove the negative voltage part from the sensed voltage to be in the range of the DSP MCU input specification (0 to 3) V as shown in the waveform of the input – output waveforms in Figure 22.

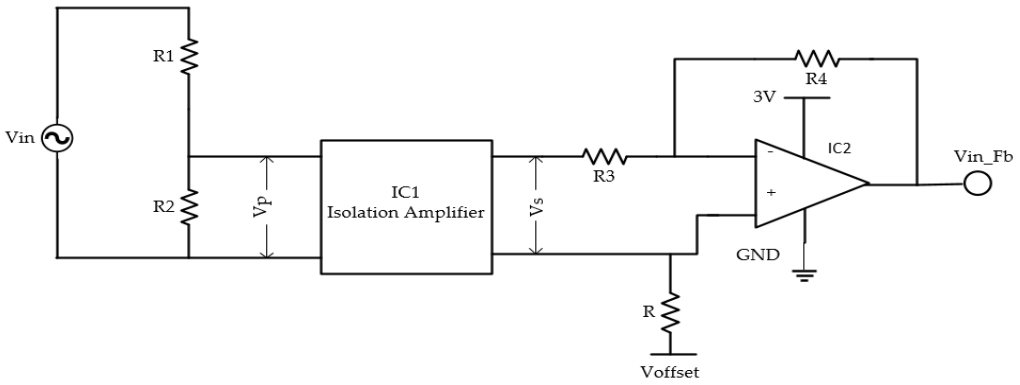

Figure 21. Block diagram of the proposed isolated AC voltage sensor (V.S 1).

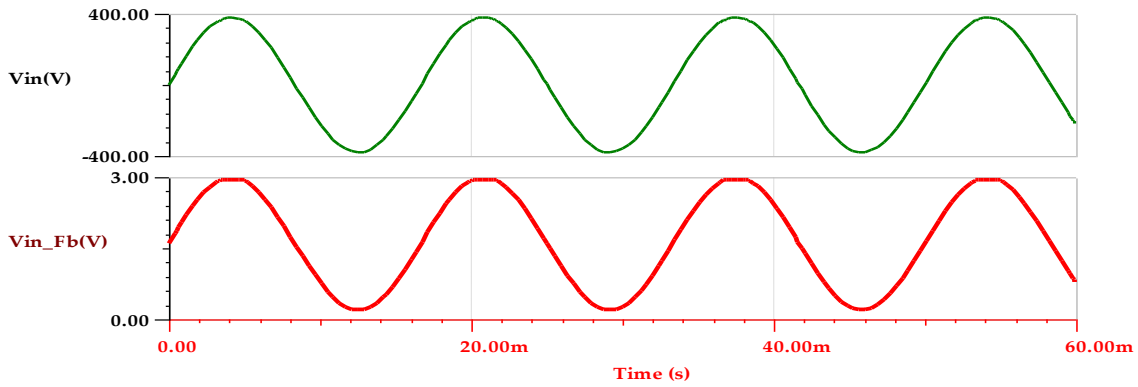

Figure 22. Isolated AC voltage sensor voltage curves with input voltage of 220 Vrms.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

6. Simulation Results and Discussion

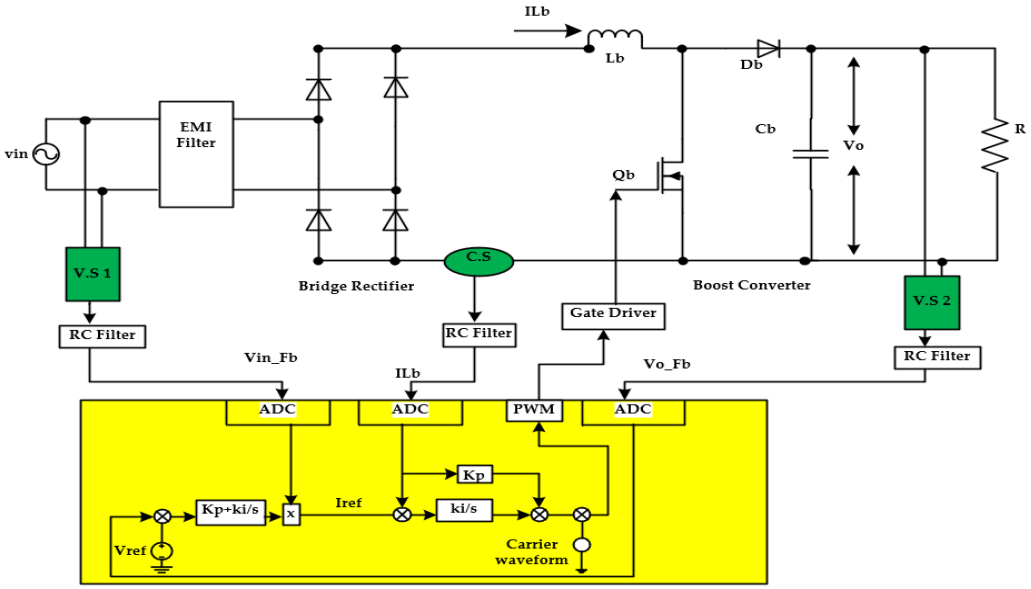

Figure 23. Complete schematic diagram of the CCM-PFC with the proposed digital control technique.

Figure 23 shows the Complete schematic diagram of the CCM-PFC converter with the proposed digital control technique which simulated in the PSIM software. EMI filter was designed based on the design report of the 2.5 kW PFC analog converter from Infineon [29]. Digital control circuit of the PFC converter was implemented using DSP TMS320F28335 with DSP speed set at 150 MHz, and the switching frequency of the pulse width modulation (PWM) generator at 100 kHz. In all sceneries of the current loop control, the voltage loop control has been implemented using the PI controller.

At the rated input of (220 V_{rms}, 60 Hz), and full load condition of P_o=2500 W, V_{bus}=400 V, Figure 24 shows the waveform of the inductor current (I_{Lb}) with the reference current (Iref) in case of PI current controller. From which we can clearly observe the distortion at the inductor current around the zero-crossing point due to that slow dynamic response of the PI controller around the zero-crossing point and the falling of the inductor current (I_{Lb}) to track the reference current (I_{ref}).

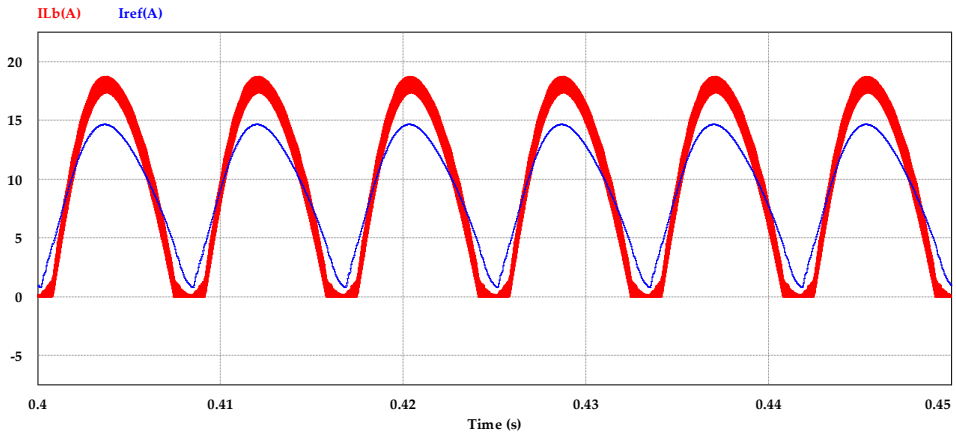

Figure 24. Waveforms of the inductor and reference currents with PI current controller.

The distortion of the inductor current (I_{Lb}) at the zero-crossing point cause current distortion in the supply current (I_{supply}) as shown in Figure 25, which we can observe the zero-crossing distortion (ZCD) period is about 1.45 ms at the supply current.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

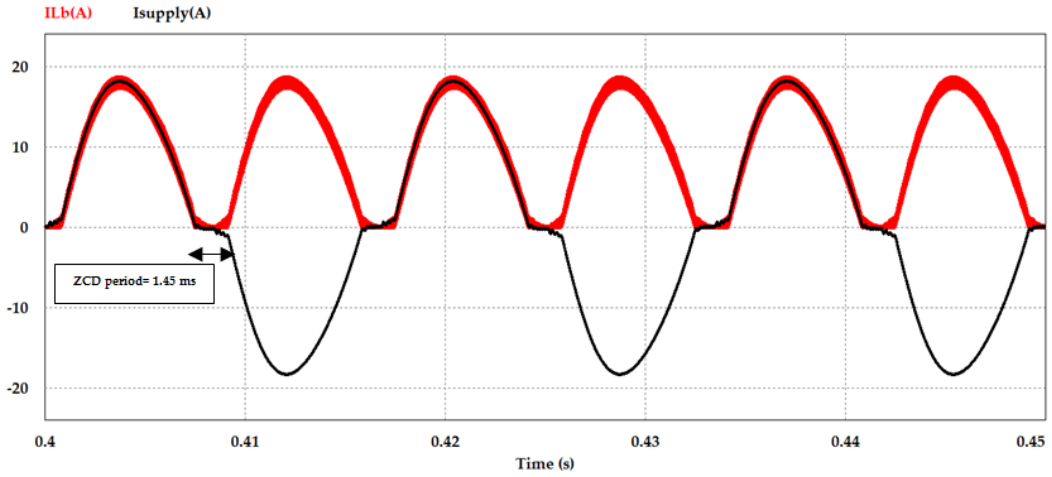

Figure 25. Waveforms of the inductor and supply currents with PI current controller.

The ZCD effected in the sinusoidal shape of the supply current where the current waveforms can't follow the sinusoidal waveform of the supply voltage (V_{supply}) as shown in the supply voltage-current waveforms in Figure 26.

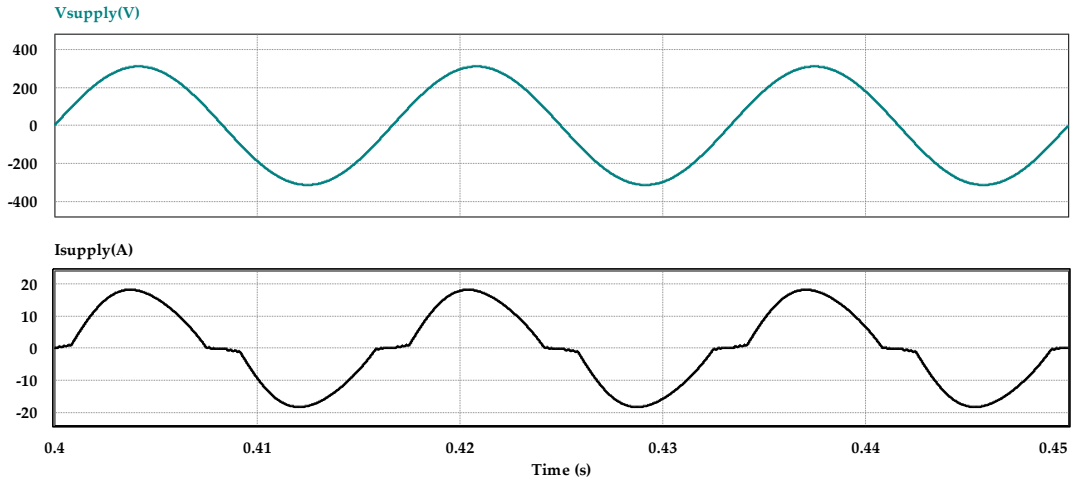

Figure 26. Waveforms of the supply current-voltage with PI current controller.

Figure 27 depicts the frequency spectrum of the supply current. The fundamental current at 60 Hz is about 16.58 A, and the odd harmonics (3, 5, 7, ….) are the dominant harmonics presented in the supply current frequency spectrum, where the third harmonic component about 1.81 A, the fifth harmonic about 0.95 A and the seven harmonics about 0.47 A. the THD in the supply current is 19.49% at full load condition.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

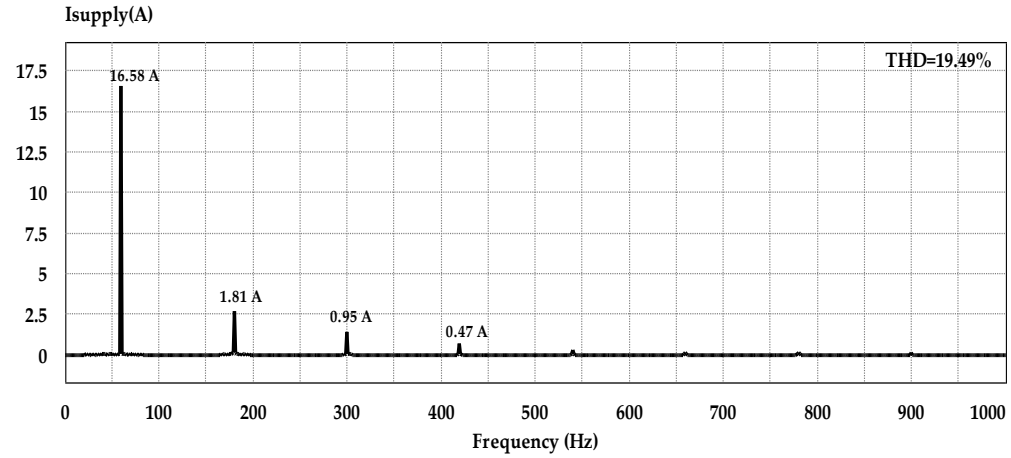

Figure 27. Frequency spectrum of the supply current at full load with PI current controller.

At the rated input of (220 V_{rms}, 60 Hz), and full load condition of P_o=2500 W, V_{bus}=400 V, IP digitally controller was applied on the inner current control loop in order to remove the distortion around the zero-crossing point. Figure 28 shows the waveform of the inductor current (I_{Lb}) with the reference current (I_{ref}) in case of the PI current controller. From which we can clearly observe that the inductor current (I_{Lb}) can successfully track the reference current (I_{ref}) and the ZCD was Significantly decreased.

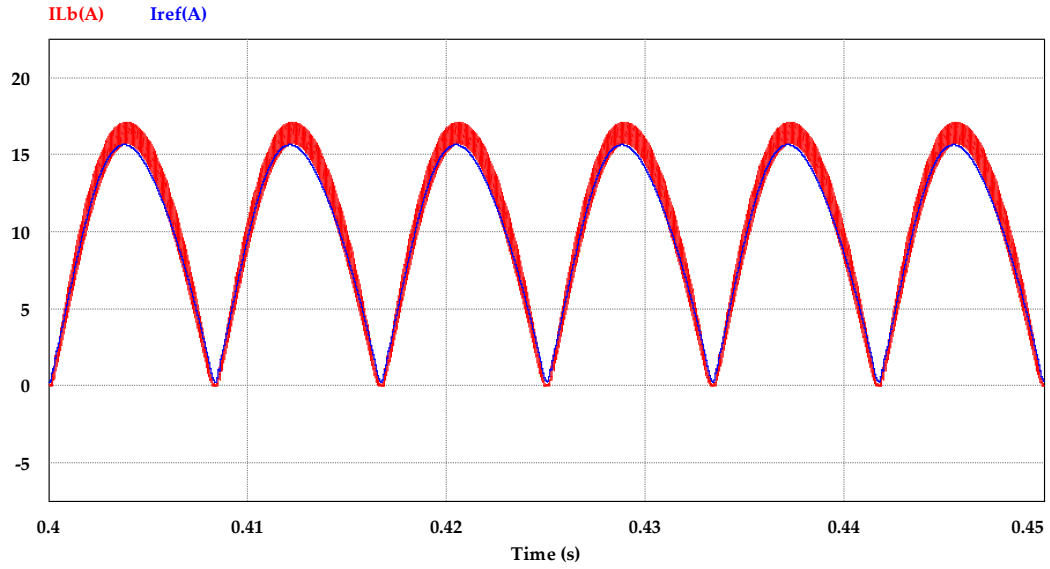

Figure 28. Waveforms of the inductor and reference currents with the proposed IP current controller.

Figure 29 shows Waveforms of the inductor and supply currents with the proposed IP current controller, which we can observe that the zero-crossing distortion (ZCD) period was decreased from 1.45 ms in case of PI controller to about 0.17 ms with using the proposed IP controller in the inner current control loop of the PFC boost converter.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

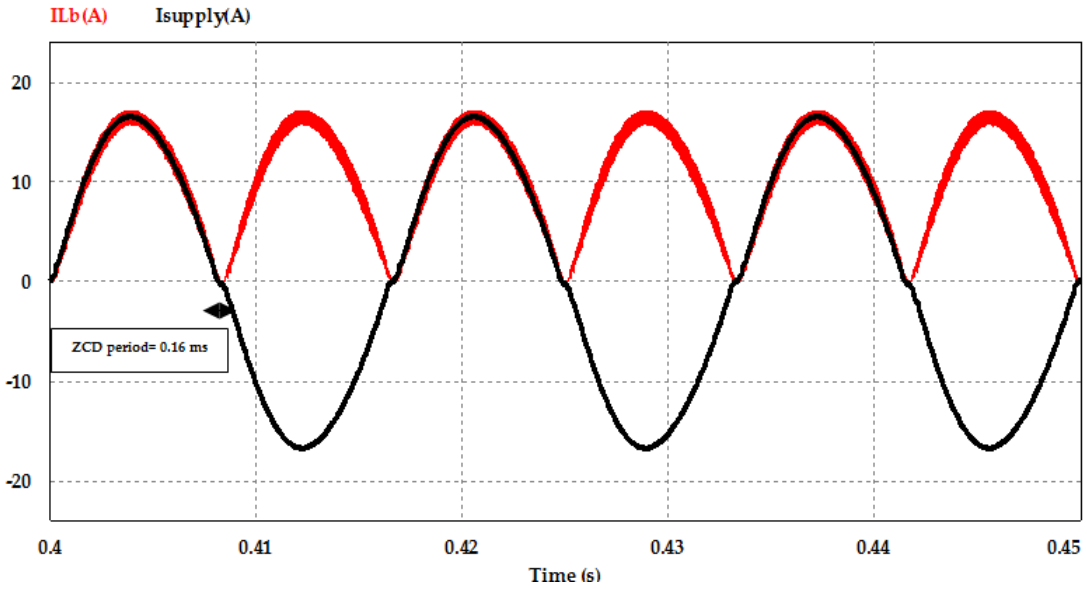

Figure 29. Waveforms of the inductor and supply currents with the proposed IP current controller.

Figure 30 shows the input supply voltage and current waveforms at full load condition and with using the proposed IP current controller, reduction of the ZCD period make the current waveform approximately sinusoidal shape and can follow the voltage waveform.

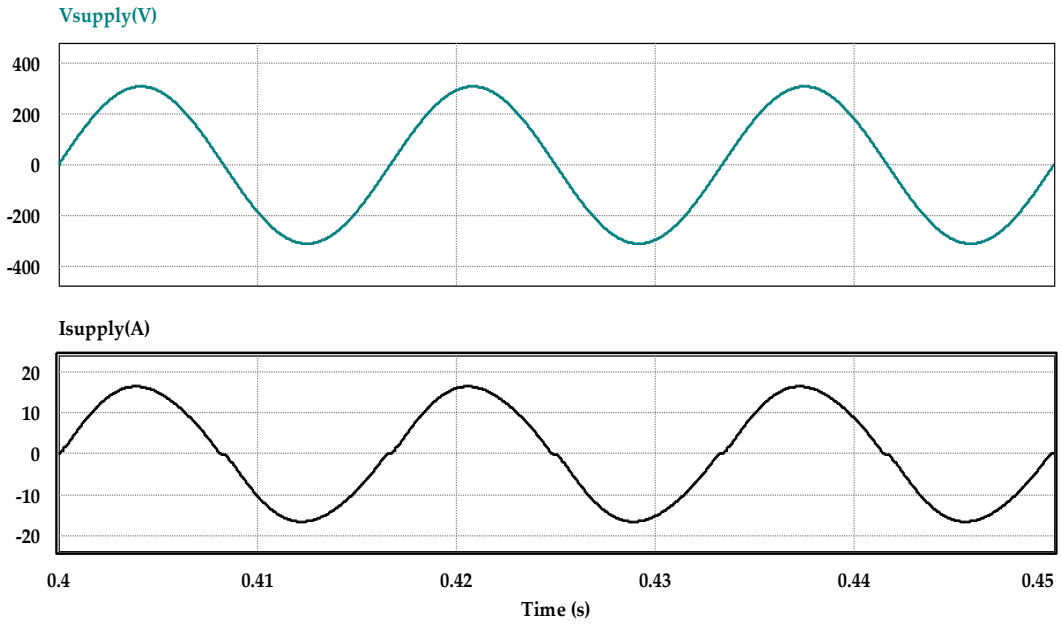

Figure 30. Waveforms of the supply current-voltage with the proposed IP current controller.

Figure 31 depicts the frequency spectrum of the supply current with using the proposed IP current controller in the inner current control loop. The fundamental current at 60 Hz is about 16.35 A, it can clear observe that with using IP current controller the third harmonic component was reduced from 1.810 A to about 0.403 A, the fifth harmonic component was reduced 0.95 A to 0.1855 A and the seven harmonics was reduced from 0.47 A to 0.1133 A, also, the THD in the supply current with full load condition was reduced from 19.49 % to about 5.23%.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 17 November 2020 doi:10.20944/preprints202011.0447.v1

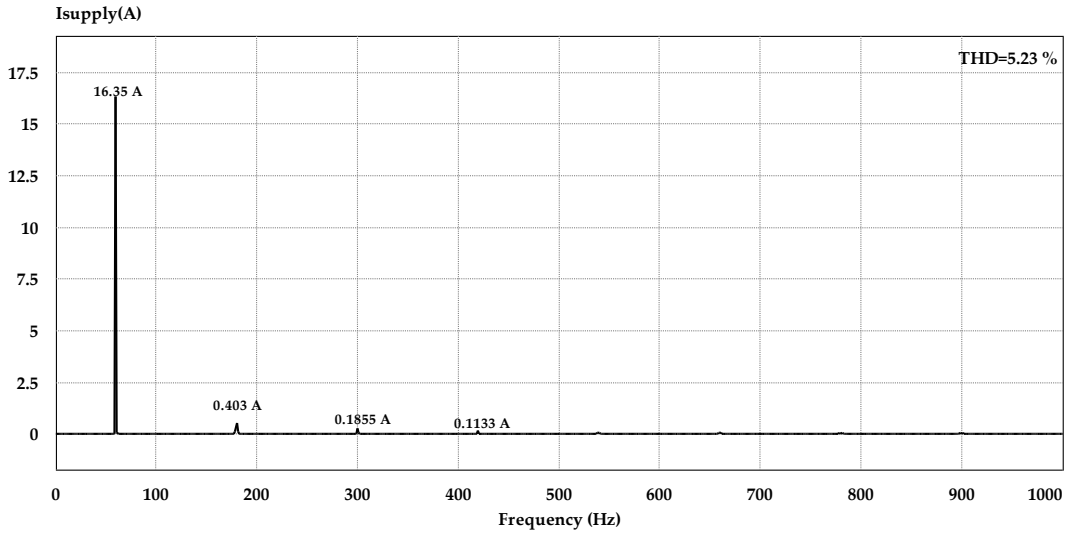

Figure 31. Frequency spectrum of the supply current at full load with the proposed IP current controller.

With different loading condition the performance of the designed PFC boost converter with different current control techniques was performed, Table 2 shows the PFC boost converter performance with loading conditions of (25%, 50%, 75%, and 100%) of the full load condition (2500 W). from the results, at full load condition the designed PFC boost converter with the proposed current controlling technique offer efficiency about 98.66 %, THD about 5.23 % and power factor about 99.93 %.

Table 2. Performance investigation of the designed CCM-PFC with different loading conditions.

Parameter	With conventional PI controller				With proposed IP controller			
Load condition(W)	625	1250	1875	2500	625	1250	1875	2500
THD%	34.80	26.50	21.39	19.37	30.20	20.70	11.00	5.23
P.F%	93.86	96.38	97.52	98.31	94.50	96.60	99.12	99.93
Power Losses (W)	15.69	22.90	30.90	38.40	11.40	18.00	26.10	34.00
Efficiency%	97.45	98.20	98.37	98.48	98.40	98.60	98.63	98.66

7. Conclusions and Future Work

Fast dynamic response IP current controller based on small signal stability modeling of the conventional PFC boost converter was proposed in this paper. Comparative analysis between using of the conventional PI and the proposed IP current controllers were also performed in this work which shows that inner current control loop of the PFC converter with the proposed IP controller reduced the THD around the zero-crossing point to about 5.23% at full load condition and offers PFC converter operation with power factor near to unity. Furthermore, two voltage sensors with economical price for the AC input and the DC output measurements of the digitally controlled PFC converter were proposed and used to interface with the DSP MCU TMS320F28335. The future plan will be focused in the experimental implementation and the design of the printed circuit board (PCB) of the digitally controlled PFC converter with the proposed IP current controller and isolated voltage sensors for the experimental performance investigation.

Author Contributions: The literature review and manuscript preparation, as well as the simulations, were carried out by Ahmed H. Okilly. Final review of manuscript corrections was done by Jeihoon Baek.

Funding: This research was funded by grant(2018R1D1A3B0704376413) from National Research Foundation of Korea(NRF) and grant(20CTAP-C152903-02) from Ministry of Land, Infrastructure and Transport of Korean government.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Garcia, O.; Cobos, J.A.; Prieto, R.; Alou, P.; Uceda, J. Single phase power factor correction: A survey. IEEE Trans. Power Electron. 2003, 18, 749–755.
2. Kim, Yun-Sung, Won-Yong Sung, and Byoung-Kuk Lee. "Comparative performance analysis of high density and efficiency PFC topologies." IEEE Trans. power electronics 29, no. 6 (2013): 2666-2679.
3. Figueiredo JP, Tofoli FL, Silva BL. A review of single-phase PFC topologies based on the boost converter. In2010 9th IEEE/IAS International Conference on Industry Applications-INDUSCON 2010 2010 Nov 8 (pp. 1-6). IEEE.
4. Okilly, A.H.; Kim, N.; Baek, J. Inrush Current Control of High-Power Density DC–DC Converter. Energies 2020, 13, 4301.
5. Liu Z. Design of Single-Phase Boost Power Factor Correction Circuit and Controller Applied in Electric Vehicle Charging System (Doctoral dissertation, Worcester Polytechnic Institute).
6. Xiong, Yun, Yu Huang, Zaimin Zhong, and Tong Zhang. "Research and design on digital PFC of 2kW On-board charger." World Electric Vehicle Journal 4, no. 1 (2010): 202-207.
7. "Power Factor Correction (PFC) Circuit Basics". Texas Instruments training course, available online, accessed (26/9/2020).
8. Mejía-Ruiz, Gabriel Eduardo, Nicolás Muñoz-Galeano, and Jesús María López-Lezama. "Modeling and development of a bridgeless PFC Boost rectifier." Revista Facultad de Ingeniería Universidad de Antioquia 82 (2017): 9-21.
9. Chen, Zhengge, Pooya Davari, and Huai Wang. "Single-Phase Bridgeless PFC Topology Derivation and Performance Benchmarking." IEEE Transactions on Power Electronics 35, no. 9 (2020): 9238-9250.
10. Laoprom, Ittipon, and Satean Tunyasrirut. "Design of PI Controller for Voltage Controller of Four-Phase Interleaved Boost Converter Using Particle Swarm Optimization." Journal of Control Science and Engineering 2020 (2020).
11. Xu, Hengshan, Diyi Chen, Fei Xue, and Xutao Li. "Optimal design method of interleaved boost PFC for improving efficiency from switching frequency, boost inductor, and output voltage." IEEE Transactions on Power Electronics 34, no. 7 (2018): 6088-6107.
12. Masresha, Habtamu, and Teklay Haile. "Investigation of optimized topology for AC/DC power supply unit in telecom industry." Master of Science Thesis, (2019).
13. Fu M, Chen Q (2001) A DSP based controller for power factor correction in a rectifier circuit. In:Proceedings of 16th Annual IEEE Applied Power Electronics Conference and Exposition, vol 1, pp 144–149.
14. Kwon, Yong-Dae, Jin-Hyuk Park, and Kyo-Beum Lee. "Improving line current distortion in single-phase Vienna rectifiers using model-based predictive control." Energies 11, no. 5 (2018): 1237.
15. Kim, Dae Joong, Jin-Hyuk Park, and Kyo-Beum Lee. "Scheme to improve the line current distortion of PFC using a predictive control algorithm." Journal of Power Electronics 15, no. 5 (2015): 1168-1177.
16. Fernández E, Paredes A, Sala V, Romeral L. A simple method for reducing THD and improving the efficiency in CSI topology based on SiC power devices. Energies. 2018 Oct;11(10):2798.
17. Institute of Electrical and Electronics Engineers (IEEE), IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems, IEEE Standard 519, 2014.
18. Institute of Electrical and Electronics Engineers (IEEE), IEEE Recommended Practice--Adoption of IEC 61000-4-15:2010, Electromagnetic compatibility (EMC)—Testing and measurement techniques--Flickermeter—Functional and design specifications, IEEE Standard 1453, 2011.
19. "Power Factor Correction (PFC) Handbook" - ON Semiconductor, Available online: https://www.onsemi.com/pub/Collateral/HBD853-D.PDF, accessed (10/9/2020).

20. Karaarslan, A., and I. Iskender. "A DSP based power factor correction converter to reduce total harmonic distortion of input current for improvement of power quality." Electrical Engineering 93, no. 4 (2011): 247-257.
21. Kim, Jung-Won, Je-Hyun Yi, and Bo-Hyung Cho. "Enhanced variable on-time control of critical conduction mode boost power factor correction converters." Journal of Power Electronics 14, no. 5 (2014): 890-898.
22. Wang, Jizhe, Haruhi Eto, and Fujio Kurokawa. "Optimal Zero-Voltage-Switching Method and Variable ON-Time Control for Predictive Boundary Conduction Mode Boost PFC Converter." IEEE Transactions on Industry Applications 56, no. 1 (2019): 527-540.
23. Ren X, Zhou Y, Guo Z, Wu Y, Zhang Z, Chen Q. Simple analog-based accurate variable on-time control for critical conduction mode boost power factor correction converters. IEEE Journal of Emerging and Selected Topics in Power Electronics. 2019 Jul 4.
24. Ji, Yi, Yong Yang, Jiale Zhou, Hao Ding, Xiaoqiang Guo, and Sanjeevikumar Padmanaban. "Control strategies of mitigating dead-time effect on power converters: An overview." Electronics 8, no. 2 (2019): 196.
25. Cui, Jing, Jiayu Ye, and Zhongyi Chu. "IP controller design for uncertain two-mass torsional system using time-frequency analysis." Shock and Vibration journal 2018 (2018).
26. Bhatti SA, Malik SA, Daraz A. Comparison of PI and IP controller by using Ziegler-Nichols tuning method for speed control of DC motor. In2016 International Conference on Intelligent Systems Engineering (ICISE) 2016 Jan 15 (pp. 330-334). IEEE.
27. Vasanthakumar D, Srikanth V. DC-DC converter control using IP controller. In2014 International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC) 2014 Apr 16 (pp. 245-249). IEEE.
28. Vasanthakumar D, Srikanth V. DC-DC converter control using IP controller. In2014 International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC) 2014 Apr 16 (pp. 245-249). IEEE.
29. 2.5kW PFC Evaluation Board with CCM PFC Controller ICE3PCS01G. Design Report, Infineon Company. Available online: https://www.infineon.com/cms/en/product/evaluation-boards/eval_2k5w_ccm_4p_v3/(accessed on 15 April 2020).
30. "Understanding ESR in electrolytic capacitors" Available online: https://www.avnet.com, (accessed on 11/9/2020).
31. "TMS320F28335 - C2000 real-time control MCUs" data sheet, Available online: https://www.ti.com/lit/gpn/tms320f28335. (accessed on 12/9/2020).
32. "AMC1311x High-Impedance, 2-V Input, Reinforced Isolated Amplifiers" data sheet, Available online, https://www.ti.com/lit/gpn/amc1311. (accessed on 12/9/2020).
33. "Precision, Zero-Crossover, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier" data sheet, Available online: https://www.ti.com/lit/gpn/opa320. Accessed 26/9/2020. (accessed 12/9/2020).