

Article

Modified Cascaded Z-Source High Step-Up Boost Converter

Navid Salehi ¹, Herminio Martinez-Garcia ^{1,*} and Guillermo Velasco-Quesada ¹

¹ Electronic Engineering Department, Universitat Politècnica de Catalunya (UPC) – BarcelonaTech, Barcelona, Spain;

* Correspondence: herminio.martinez@upc.edu; Tel.: +34664631211

Abstract: To improve the voltage gain of step-up converters, cascaded technique is considered as a possible solution in this paper. By considering the concept of cascading two Z-source networks in a conventional boost converter, the converter takes the advantages of both impedance source and cascaded converters. However, by applying some modifications, the proposed converter provides high voltage gain while the voltage stress of switch and diodes are still low. Moreover, the low input current ripple of the converter makes it absolutely appropriate for photovoltaic applications in order to expand the lifetime of PV panels. After analyzing the operation principles of the proposed converter, simulation and experimental results of a 100W prototype are presented to verify the proposed converter performance.

Keywords: High step-up converter; Impedance source converter; Z-source converter; Cascaded technique;

1. Introduction

By emerging the lack of energy and climate changes due to increasing the fossil fuel consumption over the last decades, using renewable energies could definitely survive the earth planet from future energy crisis [1]. However, in order to utilize the renewable energies, power electronics converters are inevitably essential to produce the required voltage and current for different applications. Among different types of renewable energies, solar energy is more popular as a limitless source of energy which is spread all over the world. Although the output voltage of photovoltaic (PV) cells are relatively low, applying high step-up DC-DC converters lead to increase voltage level without connecting series numerous PV panels to enhance the operation of photovoltaic system especially in low power applications [2].

Research on high step-up converters in recent years led to present diverse topologies in order to resolve the existence drawbacks such as high voltage stress of semiconductor devices, reverse recovery problem of diodes, and intense spike on switches which are mostly appear in conventional boost converter by increasing the duty cycle [3]-[4]. Consequently, the topological alteration of the conventional boost converter was proposed by researchers to extend the input to output voltage ratio meanwhile the circuit operation will enhance as well. To overcome the drawbacks of boost converter with high efficiency and their simple control scheme, based boost converters were proposed by researcher with different techniques such as coupled-inductor based boost converter, switched-capacitor based boost converter, cascaded boost converter, and interleaved boost converter [5]. All introduced converters have some weaknesses and strengths which make them restricted for specific applications. For this purpose, a better performance of a high step-up converter will be obtain if it would be possible to apply different techniques in a converter.

Inserting the coupled-inductors into the dc-dc converters is an effective method to increase the voltage gain by adjusting the turn ratio between the windings in a topology. Although by increasing the leakage inductance, due to inserting coupled-inductors, the reverse-recovery problem of diodes

can reduce effectively, the leakage energy induces high voltage spikes across the semiconductor switches. One approach in order to solve this problem is employing switched-capacitor technique as an active clamp circuit in order to recycle the leakage energy [6]. To reduce the topology complexity and cost, passive clamps are also considered as a possible solution. In [7], a passive clamp is replaced with an active clamp in a flyback converter to enhance the performance of converter by alleviating reverse-recovery problem and lower circulating current into the clamp circuit. Switched-capacitor converters are able to provide high voltage ratio for high power applications, however, high input ripple current in these converters make them inappropriate for renewable energy applications [5].

The other step-up converter topologies such as cascaded boost converter, interleaved boost converter and three-level boost converter effectively can take the advantages of mentioned techniques like coupled-inductor, switched capacitor and switched-inductors to cover the mentioned weaknesses and improve their performance. For instance, the reverse recovery problem of cascaded-boost converter can be compromised with coupled-inductor technique, although the converter efficiency in cascaded converters will be decreased due to two times energy processing [8]-[18]. Moreover, low input current ripple of interleaved converter can effectively employ switched-capacitor configurations to improve their static voltage gain and alleviate the adverse effect of their pulsating input current [9]. In [10], a three-level boost converter is proposed by employing the coupled-inductors to increase the voltage gain and active clamp to recycle the leakage inductance energy of the coupled-inductors. Consequently, it can be observed how incorporating step-up techniques can appropriately influence the operation of different step-up topologies.

Impedance sources converters are the other recent popular methods which are used widely in power electronic converters by inserting an impedance network between power source and main circuit. The first impedance source converter was proposed in [11] on 2003 for implementing DC-AC, AC-DC, DC-DC and AC-AC power conversion. The impedance source converters are able to totally change the operational characteristics of main converter [11], [12]. An impedance network could provide the following features for a high step-up DC-DC converters [13]: high voltage gain, low voltage stress for semiconductor devices, inherent short circuit immunity, and inherent open circuit immunity. Impedance source network consists of inductors, capacitors, and diodes with different configuration such as Z-source, Y-source, Δ -source, T-source, Γ -source, TZ-source, sigma-Z-source, and so on [14]. A Y-shaped impedance network by coupled-inductors implementation in order to obtain high voltage gain in small duty ratio is presented in [15]. In [16], a Δ -source converter is investigated by employing three coupled inductors and compared with Y-source impedance network. The investigation demonstrates in Δ -source converter smaller magnetizing current and winding loss can be attained compared with Y-source converter. Moreover, the adverse effect of leakage inductance caused by coupled-inductors is reduced significantly in Δ -source converter. In [19], the other Z-source high step-up converter is presented by utilizing two core for two sets of coupled inductors. Although the voltage conversion ratio increased in the mentioned proposed converter in [19], the core loss of the ferrite reduced the efficiency of the converter. In [13], different topologies of galvanically isolated impedance source DC-DC converter with wide range of input voltage and load regulation for distributed generation systems is surveyed. However, the operating principle of a common grounded Z-source DC-DC converter for photovoltaic application is proposed in [17]. The proposed converter with the common ground for input and output resulted in to have a low cost and small size step-up converter compared with the isolated ones.

Investigation in different types of high step-up converters, resulted in proposing a novel impedance source converter by cascading two Z-source network and employing switched-capacitor-inductor cells in order to obtain a converter with high voltage gain ratio, low voltage stress on semiconductor devices, and low input current ripple as expected from impedance source converters. However, the conventional configuration of cascading two Z-source network between input source and main converter lead to suffer from very high input current ripple and high voltage stress for the switch. Consequently, by modifying the proposed configuration, the converter became appropriate for high step-up applications with low input current ripple. Furthermore, further research can be

done to find out how cascading other impedance network configurations could affect the converter operation.

In this paper after elaborating the topology of the proposed converter and investigating the operational modes in section 2, analysing and design consideration of the proposed converter is studied in section 3 in order to find out the voltage conversion ratio and voltage stresses of the switch and diodes. Finally, section 4 involves the experimental results of a prototype converter to validate the theoretical analysis.

2. Proposed Converter and Principle of Operation

As it can be seen from Fig. 1, the proposed high step-up DC-DC impedance source based boost converter includes two cascaded Z-source network and two switched-capacitor-inductor cells. The converter hires a single ferrite core with six coupled inductors, which are involved into the impedance network and cells. Very high input current ripple and high voltage stress of the switch are two main problems in this converter. Therefore, some inevitable alteration are required in order to make the converter practically applicable. Although by adding a capacitor as shown in Fig. 2, the voltage stress of the switch clamps at a specific value, the high input current ripple still consider as a drawback in this converter. The dashed-line in Fig. 2 represents how the KVL loop clamps the switch voltage at a specific value. Eventually, the final modification into the converter configuration resulted in obtaining a high step-up converter with low input current ripple and low voltage stress for semiconductor devices. Fig. 3 shows the modified proposed high step-up impedance source converter with equivalent circuit of coupled inductors. The proposed converter composed of a single switch Q_1 , one diode in the impedance network D_1 , two diodes in the cells D_2 , D_3 , and one output diode D_4 , six coupled inductors L_1 , L_2 , L_3 , L_4 , L_5 , and L_6 , four capacitors in impedance network C_1 , C_2 , C_3 , and C_4 , two switched-capacitors C_5 and C_6 , and output capacitor C_7 .

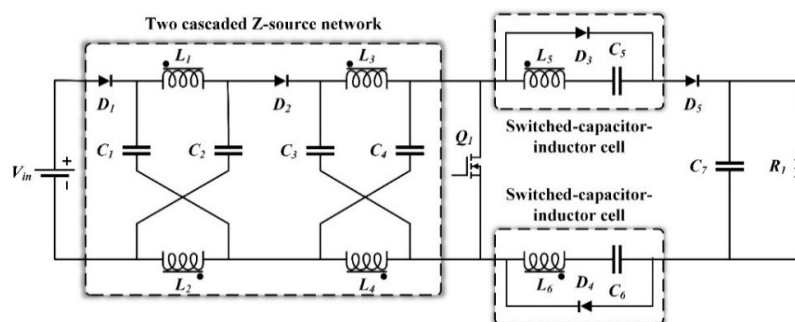


Figure 1. Two cascaded Z-source high step-up converter

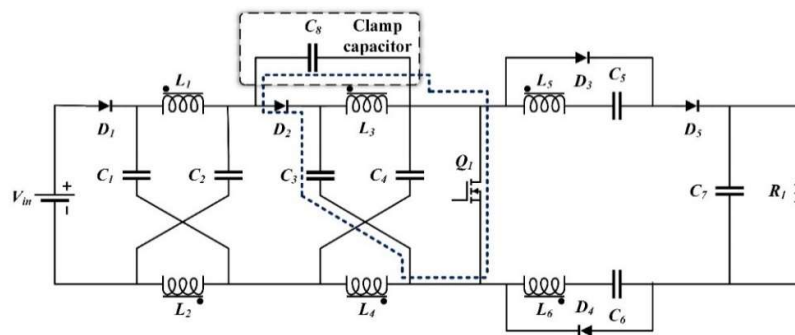


Figure 2. Modified converter by clamp capacitor

The converter has four time intervals within a switching cycle in the steady state operation. Fig. 4 illustrates the equivalent circuits for each operating interval, the capacitor C_2 can be not considered in the circuit due to being in parallel with input voltage source, and Fig. 5 is provided to show

theoretical waveforms of the proposed converter. To simplify the steady state analysis, the following assumptions are made:

- The converter operates in continuous conduction mode (CCM),
- The Switch, diodes, all inductors and capacitors are assumed ideal ,
- The magnetizing inductance is large enough to ignore its current ripple,
- The leakage inductance of all windings are equal,
- The output capacitors C_7 is large enough to make the output voltage constant,
- The switching capacitors C_5 and C_6 are equal.

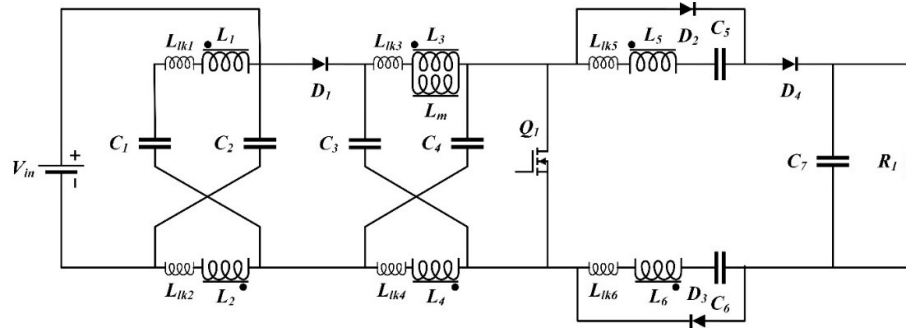


Figure 3. Circuit diagram of proposed converter with equivalent circuit of coupled-inductors

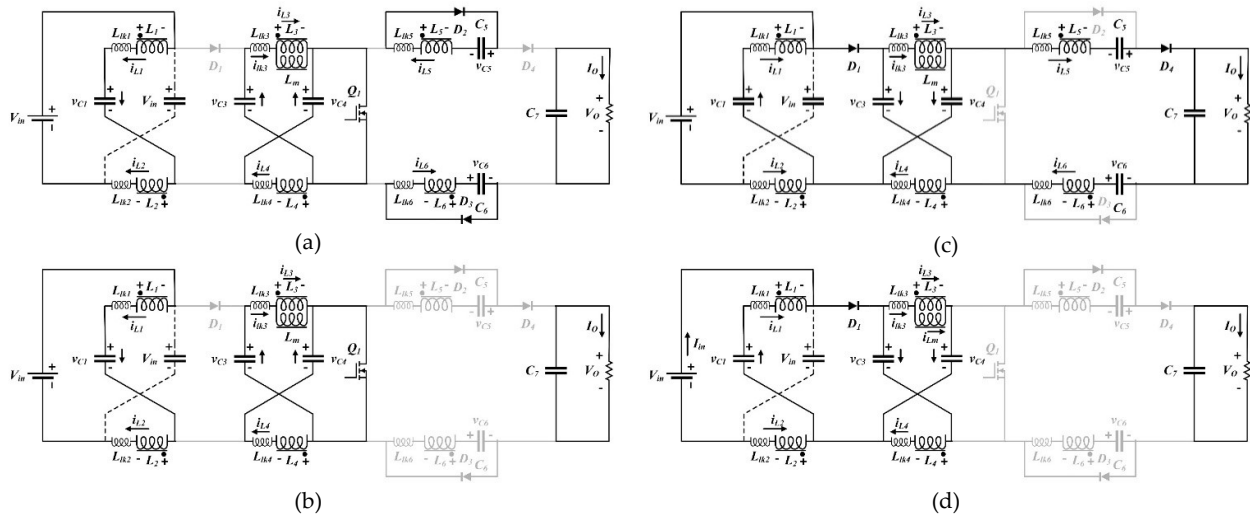


Figure 4. Equivalent circuits of the proposed converter for each operation mode

2.1. Operation Principles

Interval 1 [$t_0 < t < t_1$] (Fig. 4a): Before t_0 input diode D_1 is conducting and the other semiconductor devices are off. At t_0 , the switch Q turns on, diode D_1 becomes reverse-biased and $(2+n)V_C - V_{in}$ is applied across it. In addition, the current direction of capacitors C_3 and C_4 become reverse. In this operation mode, the capacitor voltage of C_3 and C_4 apply to inductors L_3 and L_4 , and consequently this voltage will be induced to other coupled inductors L_1 , L_2 , L_5 , and L_6 by considering the turn ratio. In this stage, the energy of leakage inductances L_1 and L_2 are recycled to the input voltage source, and the energy of leakage inductances L_5 and L_6 are absorbed by switched-capacitors C_5 and C_6 . The following equations are established in this time interval:

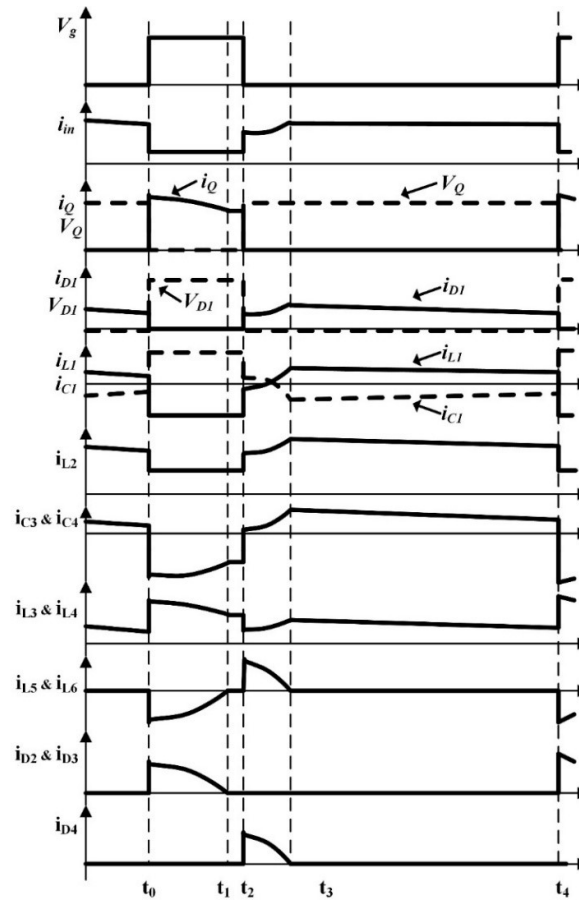


Figure 5. Theoretical waveforms of the proposed converter

$$V_{C_3} = V_{C_4} = V_C, \quad (1)$$

$$V_{L_3} = V_{L_4} = V_C, \quad (2)$$

$$V_{L_1} = V_{L_2} = V_{L_5} = V_{L_6} = nV_C, \quad (3)$$

where, n is the turn ratio of coupled inductors:

$$n = n_1/n_3 = n_2/n_3 = n_5/n_3 = n_6/n_3, \text{ and } n_3 = n_4 \quad (4)$$

$V_{C_5}(t_0)$ and $V_{C_6}(t_0)$ are less than coupled-inductor's voltage in their corresponding cells, so a resonance occurs between the leakage inductances and C_4 and C_5 to charge the capacitors through D_2 and D_3 over the half resonance period. The current and voltage of capacitor C_5 can be expressed as:

$$i_{C_5}(t) = \frac{V_{C_5}(t_0) - nV_C}{Z_{res}} \sin \omega_{res}(t - t_0) \quad (5)$$

$$v_{C_5}(t) = nV_C + [V_{C_5}(t_0) - nV_C] \cos \omega_{res}(t - t_0) \quad (6)$$

where $\omega_{res} = 1/\sqrt{L_{lk}C_5}$ and $Z_{res} = \sqrt{L_{lk}/C_5}$.

The capacitor C_3 and switch Q current are determined as:

$$i_{C_3} = I_{L_m} + i_{L_3} = I_{L_m} + ni_{C_5} \quad (7)$$

$$i_Q = I_{L_m} + 2ni_{C_5} \quad (8)$$

where i_{C_5} is given by (5).

This mode ends after half resonance period at once the current direction is going to be changed. Therefore, the diodes D_2 and D_3 turn-off at zero current.

Interval 2 [$t_1 < t < t_2$] (Fig. 4b): At this operation mode the switch Q is still on and all diodes are at the off state. Also the magnetizing inductance L_m is still charging by C_3 and C_4 . Diodes D_2 and D_3 are off in this stage due to reversing the current of inductors L_5 and L_6 which are blocked by diodes D_2 and D_3 , respectively. Therefore, the stored magnetic energy of transformer led to slightly increase the current of other coupling windings. This mode ends when the switch Q turns off. The current of inductor L_1 can be expressed as:

$$i_{L_1}(t) = \frac{nV_C - V_{C_5}(t_1)}{Z'_{res}} \sin \omega'_{res}(t - t_1) + I_1 \cos \omega'_{res}(t - t_1) \quad (9)$$

where $\omega'_{res} = 1/\sqrt{2L_{lk}C_1}$, $Z'_{res} = \sqrt{2L_{lk}/C_1}$, and regarding equation (5), I_1 is also equal to $ic_4(t_1)$ by considering the turn ratio.

Interval 3 [$t_2 < t < t_3$] (Fig. 4c): At $t=t_2$ the switch Q turns off, diodes D_1 and D_4 turn-on and energy transfer from input to the output during this stage. The stored energy of magnetizing inductance, and capacitors C_5 and C_6 also transfer to the load, and the capacitor C_3 and C_4 will be charge through diode D_1 , however, capacitor C_1 is discharged in this operation mode. The resonance between leakage inductance L_5 and C_5 and also leakage inductance L_6 and C_6 is occurred during the maximum time of half-resonant interval. This stage ends when the resonant current of ic_5 becomes zero and provide the ZCS turn-off for diode D_4 . In the following the corresponding voltage and current equations are expressed:

$$i_{C_5}(t) = \frac{V_{C_5}(t_2) - nV_C}{Z_{res}} \sin \omega_{res}(t - t_2) \quad (10)$$

$$V_{C_5}(t) = nV_C + [V_{C_5}(t_2) - nV_C] \cos \omega_{res}(t - t_2) \quad (11)$$

$$i_{D_1} = i_{L_m} + i_{L_3} \quad (12)$$

Interval 4 [$t_3 < t < t_4$] (Fig. 4d): In this stage the switch is still off and the output diode D_4 is also off by reversing the current of L_5 which was occurred in previous operation mode. However, the input diode D_1 remains on in this stage which makes the capacitors C_3 and C_4 keeping on their charging state from previous stage. Also, capacitor C_1 is discharged the same as operation mode 3. The current of L_1 can be stated as:

$$i_{L_1}(t) = \frac{nV_C - V_{C_5}(t_3)}{Z'_{res}} \sin \omega'_{res}(t - t_3) + I_3 \cos \omega'_{res}(t - t_3) \quad (13)$$

where I_3 is equal to $ic_4(t_3)$ by considering the turn ratio.

Moreover, the other current equations can be expressed as:

$$i_{D_1} = I_{in} + i_{L_1} \quad (14)$$

$$I_{L_m} = i_{C_5} + i_{C_4} - i_{L_3} \quad (15)$$

This operation mode ends when the switch will be turn-on again.

3. The Proposed Converter Analysis and Design Considerations

In this section different features of proposed converter such as voltage gain and voltage stresses of the switch and diodes are discussed and compared with other high step-up converters. Then, in order to compare the performance of proposed converter features, some graphs and tables are provided.

3.1. Conversion Ratio

When the input diode D_1 is on the capacitors C_3 and C_4 charge by input voltage source through magnetizing inductance L_m . However, at on-state of switch Q the capacitors C_3 and C_4 discharge themselves to L_m that makes increasing the voltage gain of the converter. By applying the magnetizing inductor L_m voltage-second balance equation V_C can be calculated as:

$$V_C = \frac{1-D}{1-(2+n)D} V_{in} \quad (16)$$

According to the interval 3, by applying a KVL the output voltage can be obtained as:

$$V_o = V_{in} + (V_{L_3} + V_{L_4}) + (V_{L_2} + V_{L_5} + V_{L_6}) + (V_{C_5} + V_{C_6}) \quad (17)$$

where the V_{C_5} and V_{C_6} can be expressed as:

$$V_{C_5} = V_{C_6} = n \frac{(1-D)}{1-(2+n)D} V_{in} \quad (18)$$

Therefore, the voltage gain of the proposed converter is equal to:

$$M = \frac{V_o}{V_{in}} = \frac{2n+1}{1-(2+n)D} \quad (19)$$

Fig. 6 shows the voltage gain of proposed converter by variation the duty cycle for different turn ratio of coupled inductors. As it can be seen, although by increasing the turn ratio of coupled inductors larger voltage gain can be obtained at lower duty cycle, the duty cycle range for step-up purpose in Z-source converter will be restricted. In fact, the following equation represents the range of duty cycle for proposed impedance source converter in step-up operation mode:

$$0 < D < \frac{1}{2+n} \quad (20)$$

Moreover, higher turn ratio results in higher power loss due to increasing the leakage inductance of coupled inductors. Also in Fig. 7, the voltage gain of the proposed converter is compared with converters in [12], [18]-[19]. As it can be observed voltage gain of proposed converter is higher than other three converters for variation of duty cycle from zero to 0.33 by considering the unity turn ratio of coupled inductors.

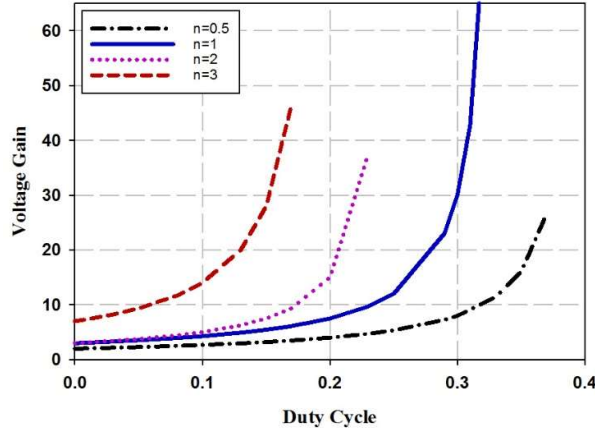


Figure 6. Voltage gain of proposed converter for different turn ratio of coupled inductors

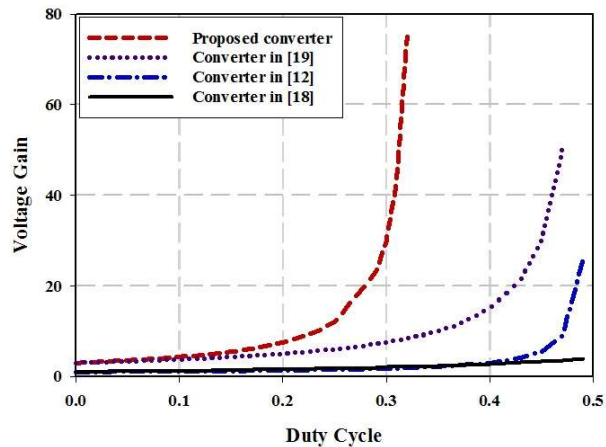


Figure 7. Voltage gain of proposed converter vs. converters in [12], [18]-[19]

3.2. Voltage Stresses of Switch and Diodes

By considering the corresponding time interval of converter operation mode, the voltage stress of semiconductor devices can be calculated. According to the interval 1, voltage stress of D_1 and D_4 can be determined as:

$$V_{D_1} = (2+n)V_C - V_{in} = \frac{1+n}{1-(2+n)D} V_{in} \quad (21)$$

$$V_{D_4} = V_o \quad (22)$$

Also the voltage stress of diodes D_2 and D_3 can be determined by considering interval 2 as:

$$V_{D_2} = V_{D_3} = \frac{V_o}{3} \quad (23)$$

To calculate the voltage stress of switch Q , a KVL is applied by considering interval 3, therefore, the following equation will be obtained:

$$V_{sw} = 2V_{L_3} + nV_{L_3} + V_{in} = (2+n)\left(\frac{V_c - V_{in}}{1+n}\right) + V_{in} \quad (24)$$

According to the equation (16), the voltage stress of the switch can be expressed as:

$$V_{sw} = \frac{1}{1-(2+n)D} V_{in} \quad (25)$$

Fig. 8 shows the voltage stress of the switch for different turn ratio of coupled inductors by varying the duty cycle, as it can be observed by increasing the turn ratio, the voltage stress increase as well. Moreover, Fig. 9 demonstrates the voltage stress of proposed converter compared with converters in [12], [18]-[19]. The voltage gain varies from 5 to 15 and the voltage stress of the switch for the converters compare with each other. As it can be seen from Fig. 9, stress voltage of the switch in proposed converter and converter in [19] is lower than two other converters.

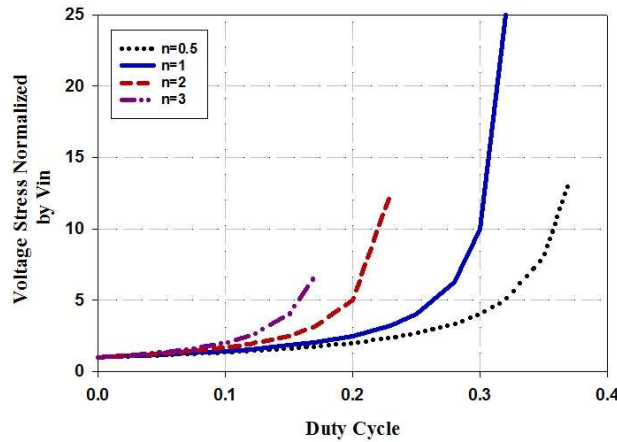


Figure 8. Voltage stress of the switch for different turn ratio of coupled inductors

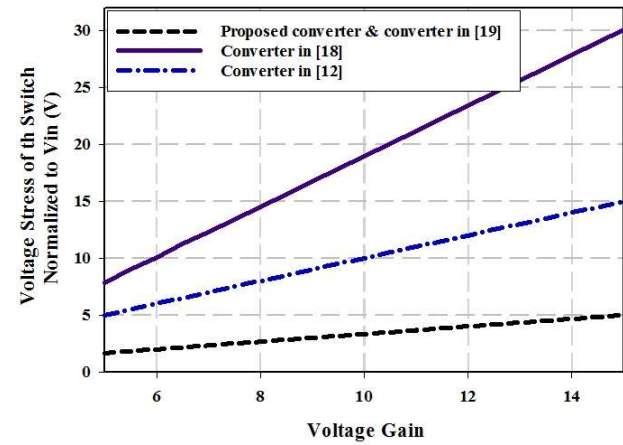


Figure 9. Voltage stress of the switch in proposed converter and converters in [12], [18]-[19]

3.3. Converter Analysis and Design Guideline

The ZCS occurs for the diodes D_2 , D_3 and D_4 for the sake of resonance between leakage inductance of L_5 (or L_6) and C_5 (or C_6). The full-resonance will be done if the following equation satisfied:

$$\frac{T_{res}}{2} < DT_{sw} \quad (26)$$

In order to stabilize the input current, the equation (26) is not satisfied in the proposed converter. However, the ZCS condition is still established, because only even begging part of the resonant waveform will be affected.

In addition, the diode D_4 is conducting current only in time interval 3 ($t_2 < t < t_3$). Therefore, it can be concluded, the average current of D_4 is equal to output current:

$$\langle I_{D_4} \rangle = I_o \quad (27)$$

Consequently, the leakage inductance can be calculated as:

$$L_{lk} = \frac{V_{C_5} - nV_c}{I_o} (1 - \cos \omega_{res} (t_3 - t_2)) \quad (28)$$

The duration $t_3 - t_2$ can be considered as maximum DT_{sw} . In addition, magnetizing inductance can be also calculated as following by considering desirable current ripple ΔI_L :

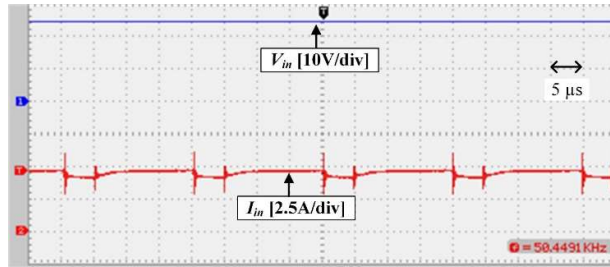
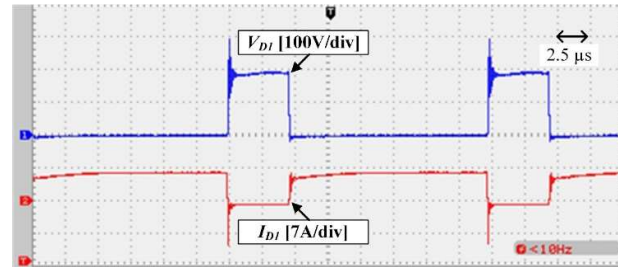
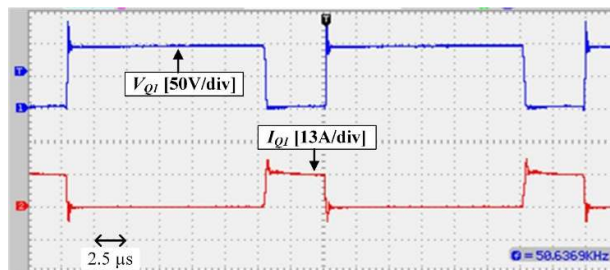
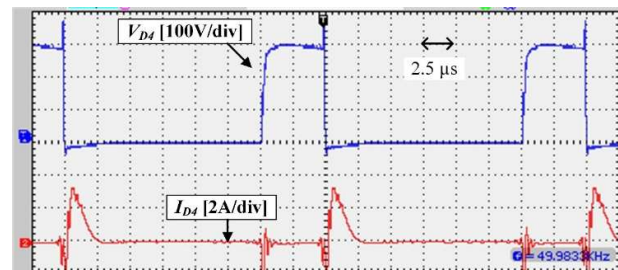
$$L_m = \frac{DV_c}{f_{sw} \Delta I_L} \quad (29)$$

Table 2. Important parameters of the implemented prototype

Parameters	Value
Input voltage V_{in}	25 V
Output voltage V_o	300 V
Output power P_o	100 W
Switching frequency (f_{sw})	50 kHz
Switch Q	IRFP3710
Input diode D_1	MUR880
Diodes D_2, D_3, D_4	MUR460
Coupled inductors core	380 μ H
$L_1, L_2, L_3, L_4, L_5, L_6$	90 turns
Turns of ($L_1 \dots L_6$)	1
Turns ratio n	1
Z-source network capacitors (C_1, C_2, C_3 and C_4)	15 μ F/100 V
Switched capacitors C_6, C_7	560 nF /100 V
Output capacitors C_8	10 μ F/400 V

Moreover, experimental waveforms of the implemented prototype are illustrated in Figure 11 to Figure 15. Input current and voltage of the converter are shown in Figure 11, the low input current ripple can be observed in this figure. Figure 12 shows the voltage and current of diode D_1 , also the voltage and current waveforms of the switch is shown in Figure 13. It can be seen that regarding output voltage of 300V, which is illustrated in Figure 15, the stress voltage of MOSFET is 100V. Finally, the voltage and current of diode D_4 can be seen in Figure 14.

The efficiency of proposed converter is calculated by measuring the input and output current and voltage of the converter by means of DC current and voltage meters, respectively. Fig. 16 shows the efficiency of the implemented proposed converter from 50 percent to 100 percent of full load condition and it is compared with converter in [19]. As it can be observed, by increasing the output power, conduction losses increase as well and lead to drop the efficiency slightly. Moreover, under full-load condition, the measured efficiency is 93%.

**Figure 11.** Input Voltage and current of the converter**Figure 12.** Voltage and current waveform of the diode D_1 **Figure 13.** Voltage and current waveform of the switch Q **Figure 14:** Voltage and current waveform of the diode D_4

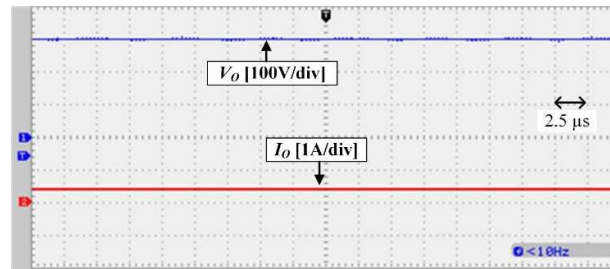


Figure 15. Output voltage and current waveform of the high step-up converter

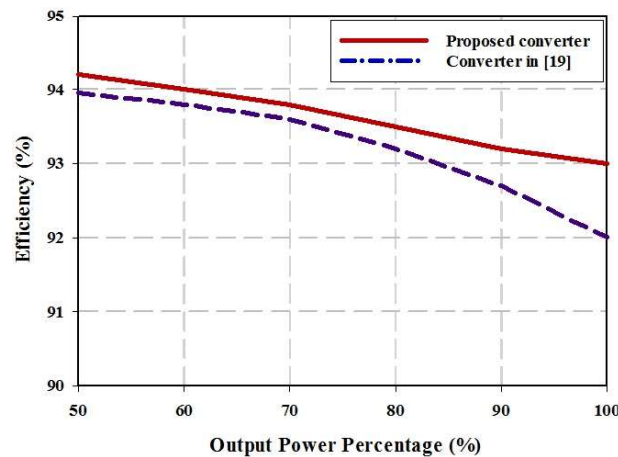


Figure 16. Efficiency plot of the implemented prototype under different load conditions

5. Conclusions

Among different step-up techniques which were applied on boost converter in order to improve the input to output voltage ratio, cascaded technique was chosen in this paper in order to cascade two Z-source networks and take the advantage of both cascade and impedance source converters. All inductors are coupled together in the proposed converter, therefore, the voltage gain increase only by utilizing a single core in the proposed configuration. Low duty cycle of the switch lead to reduce the reverse recovery problem of the output diode significantly and results in enhancing the efficiency due to reduction of loss power of switch and diodes. Furthermore, diodes D_2 , D_3 , and D_4 turn off under ZCS condition. The low input current ripple of this converter makes it appropriate to apply in renewable energy sources. A laboratory prototype of the proposed converter in order to justify the theoretic analysis is built and experimental waveforms presented for a 100W output power converter.

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