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Article

Design and Implementation of a Control Method for GaN-based Totem-Pole Boost-type PFC Rectifier in Energy Storage Systems

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Abstract: With the unceasing advancement in wide-bandgap (WBG) semiconductor technology, the minimal reverse-recovery charge Q_{rr} and other more powerful natures of WBG transistors enable totem-pole bridgeless PFC to become a dominant solution for energy storage systems (ESS). This paper focuses on design and implementation of a control structure for a totem-pole boost PFC with newfangled enhancement-mode Gallium Nitride (eGaN) FETs, not only to simplify the control implementation, but also to achieve high power quality and efficiency. The converter is designed to convert a 90-264-VAC input to a 385-VDC output for a 2.6-kW output power. Lastly, to validate the methodology, an experimental prototype is characterized and fabricated. The uttermost efficiency at 230 VAC attains 99.14%. The lowest total harmonic distortion in the current (ITHD) at high line condition (230 V) reaches 1.52% while the power factor gains 0.9985.

Keywords: Totem-pole power factor correction; energy storage systems (ESS); digital control; Gallium Nitride (GaN) based, current harmonic distortion mitigation; efficiency and power quality improvement

1. Introduction

Grid-tied energy storage system has been one of the most prevailing technological approaches for better harnessing the power generated from "clean" and "green" energy of natural resources, reducing carbon footprints, and providing resiliency to the grid [1-8]. The system can accumulate excess energy into battery packs and feed the stored energy from battery packs back into the utility grid whenever needed by handling power convertors. The change in the electric power from a form to another form of DC/DC, DC/AC and AC/DC converters occurs while the reliability, flexibility, stability, efficiency and power quality ought to be still secured [3,4,9,10]. Of all AC/DC converters, the totem-pole boost-type PFC rectifier has been a promising candidate for ESS applications thanks to superior benefits of bidirectional energy flow capability, high flexibility in control and the least device number [11,12]. Accordingly, as described in Figure 1, an interface with the totem-pole boost-type PFC rectifier is able to construct a bidirectional interconnection of ESS and the grid, thereby taking the advantages of the photovoltaic panels and wind turbines as well as enhancing the performance of the entire system [13].

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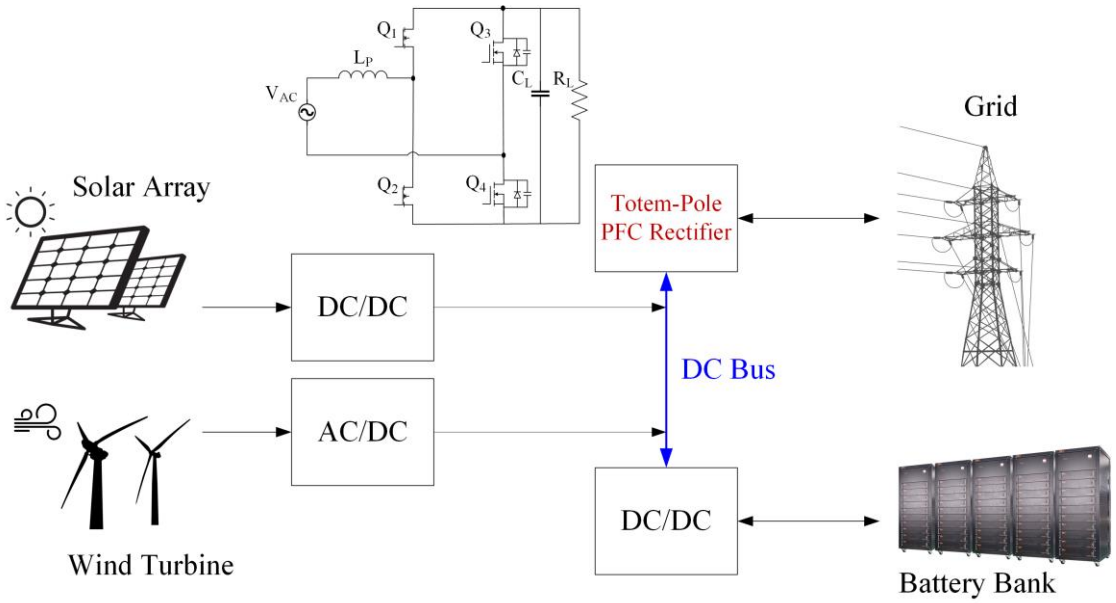

Figure 1. The totem-pole PFC rectifier in energy storage systems

Owing to slow body diode reverse-recovery charge, typical super junction MOSFETs based totem-pole bridgeless PFC has been restricted to critical-conduction mode operation (CRM) [14-17]. Even though operating in CRM with soft-switching method can achieve valley/zero-voltage-switching or zero-current-switching, it is unappealing for higher power applications due to high zero-current-detection subcircuit cost, high EMI noise and high input current ripple. By exploiting more advanced figure-of-merits (FOM) of fast switching WBG power electronic devices such as SiC MOSFETs and GaN FETs to substitute the Si power semiconductors, the WBG device-based totem-pole bridgeless PFC rectifier, has become practical for continuous conduction mode operation and improved the power density for the system [11,18-28]. One of the modified versions of the totem-pole bridgeless PFC, is implemented with full-bridge configuration in synchronous rectification mode, comprising active H-bridge switches (Q_1, Q_2, Q_3 and Q_4), which reduces the power dissipation when compared to the equivalent diodes [25,28]. These four active switches constructing two switching legs performs voltage step-up function and line rectification. As shown in Figure 1, two fast 650V eGaN FETs, which are opted for this work, play the same role as boost converters whereas two low resistance Silicon MOSFETs are placed to exterminate conducting diodes. Correspondingly, the power conduction path embraces one fast switch and one slow switch without related diode drop to ameliorate the efficiency.

Similar to most of the bridgeless topologies, it is evident that an inherent challenge of the totem-pole boost PFC is the conspicuous common-mode (CM) noises, especially a pounding current spike at zero-crossing interval of AC voltage, which significantly aggravates the current line quality, such as total harmonic distortion (THD) and power factor (PF) [29-32]. The high current harmonic distortion would destructively affect the grid as well as the other electrical equipment connecting to the grid whilst the low power factor would provoke the energy extravagance. As is known, the Si MOSFET is modeled as an ideal switch with a body diode and a parasitic capacitor. Aside from the cause of the abrupt alteration in the duty cycle, the zero-crossing distortion rooted by the poor reverse recovery characteristic of the body diode and sudden discharge of the parasitic output capacitance of the slow speed leg upper switch Q_3 (from positive to negative half-cycle transition point) or lower switch Q_4 (from negative to positive half-cycle transition point) when the corresponding fast leg active switch turns on. For example, during the swap from negative to positive mains half-line cycle of the input voltage, GaN FET Q_2 becomes the active switch in the high frequency leg. Since input voltage is approximately zero, in order to output voltage reaches 385 V, Q_2 has the widest duty while Q_4 was blocking 385 V during the negative half of the AC line cycle. For this reason, when Q_2 turns on, the charge stored in the parasitic output capacitance of Q_4 will incur a positive current spike on

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the input inductor. To gradually discharge the parasitic output capacitance of the slow-speed leg Si MOSFET, the soft start technique with multiple gate pulses of increasing small duty ratio are applied at zero-crossing area [33].

In order to circumvent the requirements on power performance and obstacles surrounding the bidirectional inductor current, lacking a bridge rectifier and the function interchange among switches, a new control structure is proposed with the harmony in both firmware and hardware to expedite the control algorithm and implementation. This paper is organized into five sections. Section 2 gives a proposed control architecture of the individual blocks over the totem-pole PFC converter topology. In Section 3, firmware considerations on the control strategy of the converter is presented in detail. Section 4 shows the experimental results, encompassing the measured waveforms, converter efficiency, PF and THD in the current under different conditions. Finally, conclusions and remarks are drawn in Section 5.

2. Proposed Control Structure

2.1. Block Diagram

The block diagram of the proposed control system for totem-pole PFC rectifier, which is displayed in Figure 2, consists of major parts: power stage and sensing circuit, digital signal processor (DSP) controller block and auxiliary logic circuit. Each block is described in more details in the following sections. Four signals including the Line voltage sensing signal, the Neutral voltage sensing signal, the inductor current sensing signal and the output voltage sensing signal are acquired from the power stage circuit by the signal conditioning and sensing circuits to feed to the digital control block.

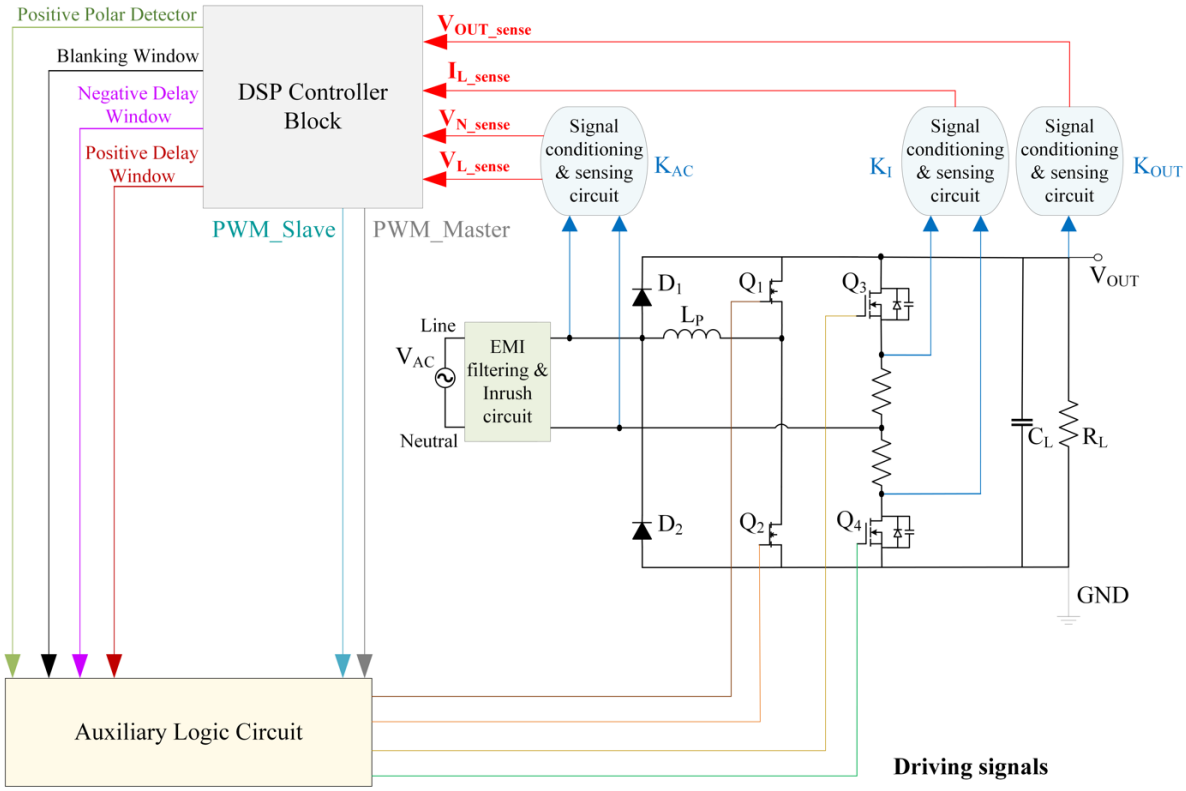

Figure 2. Simplified block diagram of the proposed structure

K_{AC}, K_I and K_{OUT} denotes the gain of the mains voltage sensing circuit, the gain of the current sensing circuit, and the gain of the output voltage sensing circuit, respectively. Because the measurement range of analog-to-digital (ADC) pins within DSP is from 0 to 3.3 V, the sensing signals are scaled in order not to be greater than the maximum value of 2.5 V. For this tolerance purpose, K_{AC}, K_I and K_{OUT} should be limited by

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$$K_{AC} \leq \frac{2.5}{\sqrt{2}V_{AC\_MAX}} \quad (1)$$

$$K_{I} \leq \frac{2.5}{\sqrt{2}I_{RMS\_MAX}} \quad (2)$$

where I_{RMS_MAX} is the maximum root-mean-square value of the input current

$$K_{OUT} \leq \frac{2.5}{V_{OUT\_MAX}} \quad (3)$$

2.2. Power Stage and Sensing Circuit

2.2.1. Power Stage

The power stage of totem-pole bridgeless PFC rectifier contains a pair of GaN FETs (Q_1, Q_2) that switches at PWM frequency and a pair of regular MOSFETs (Q_3, Q_4) that operates at line frequency. Apart from EMI filtering and inrush circuit, two diodes (D_1, D_2) are added in front of the PFC choke to cope with the huge current for the load capacitance pre-charge. The topology operates in two modes depending on the polarity of the AC voltage, where each fast-speed leg switch has to perform either master or slave mission as displayed schematically in Figure 3.

During the positive semi-period of the input voltage, Q_4 is in ON-state and Q_3 is in OFF-state: upper fast-speed leg switch Q_1, lower fast-speed leg switch Q_2 and power inductor L_P form a boost DC/DC stage where Q_2 acts as a master switch and Q_1 acts as slave switch. The operating states when the input AC voltage is positive are illustrated in Figure 3(a) and Figure 3(b). When the main switch Q_2 is ON with t = [0, DT_s] (where D is the duty cycle and T_s is the switching period), the current flows from the choke L_P to Q_4 through Q_2 and back to Neutral. The load is charged by the output capacitor at the same time in this half-line cycle. When Q_2 is open and Q_1 is closed with t = [DT_s, T_s], the current flows via Q_1, then via the output capacitor and load, and back to Neutral through Q_4. The ground of the output side is tied to Neutral potential as Q_4 is conducting all the time in positive half-line cycle. Another complete switching cycle repeats when Q2 switches on again by the gate-to-source voltage of the driver circuit. Similarly, during the negative half-line cycle Q_3 is in ON-state and Q_4 is in OFF-state: the operation in the negative half-line cycle is analogous except the role of the upper and lower switches are exchanged. Q_1 turns out to be the master switch and Q_2 becomes the slave switch. Figure 3(c) and Figure 3(d) depict the operation principle when the input AC voltage is negative. Relied on two major operating modes, together with optimizing the performance, a new control signal sequence is depicted and explained in the subsection 2.4.

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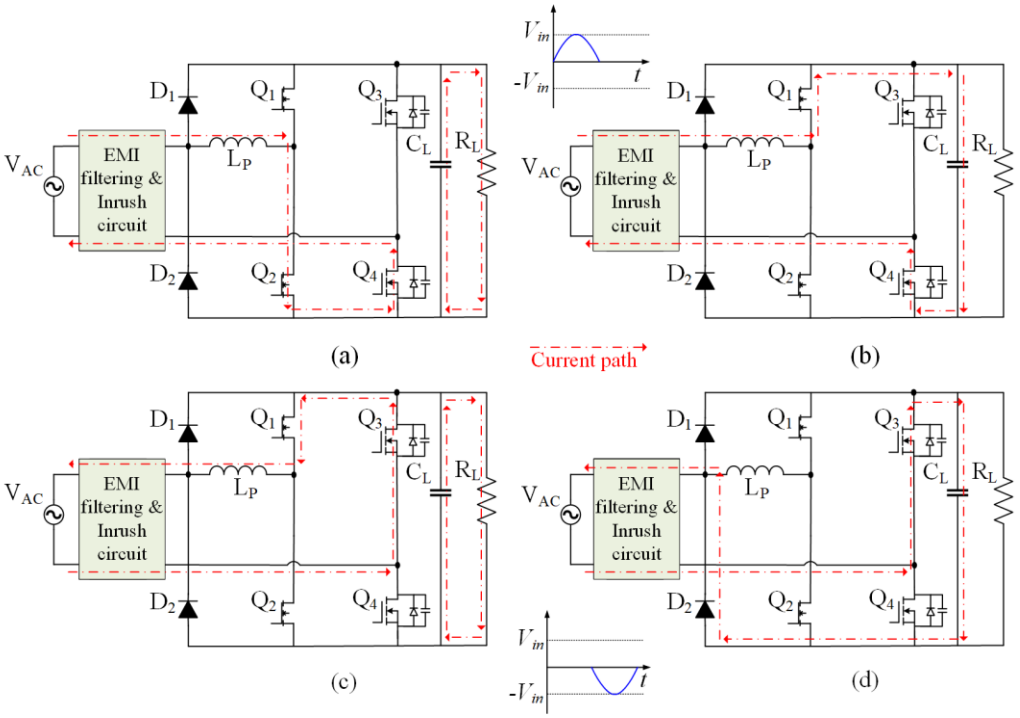

Figure 3. Current flows during positive and negative AC half cycles: (a) positive AC half cycles from 0 to DT_s; (b) positive AC half cycles from DT_s to T_s; (c) negative AC half cycles from 0 to DT_s; (d) negative AC half cycles from DT_s to T_s.

2.2.2. Signal Conditioning and Sensing Circuit

Referring to Figure 4, the signal conditioning and sensing circuit is the interface of power stage and control stage. For the sake of controller design, the system uses four sensing circuitries and filters to sense the vital signals, namely input current I_{L_sense}, bus voltage V_{OUT_sense}, input voltage Neutral V_{N_sense} and input voltage Line V_{L_sense}.

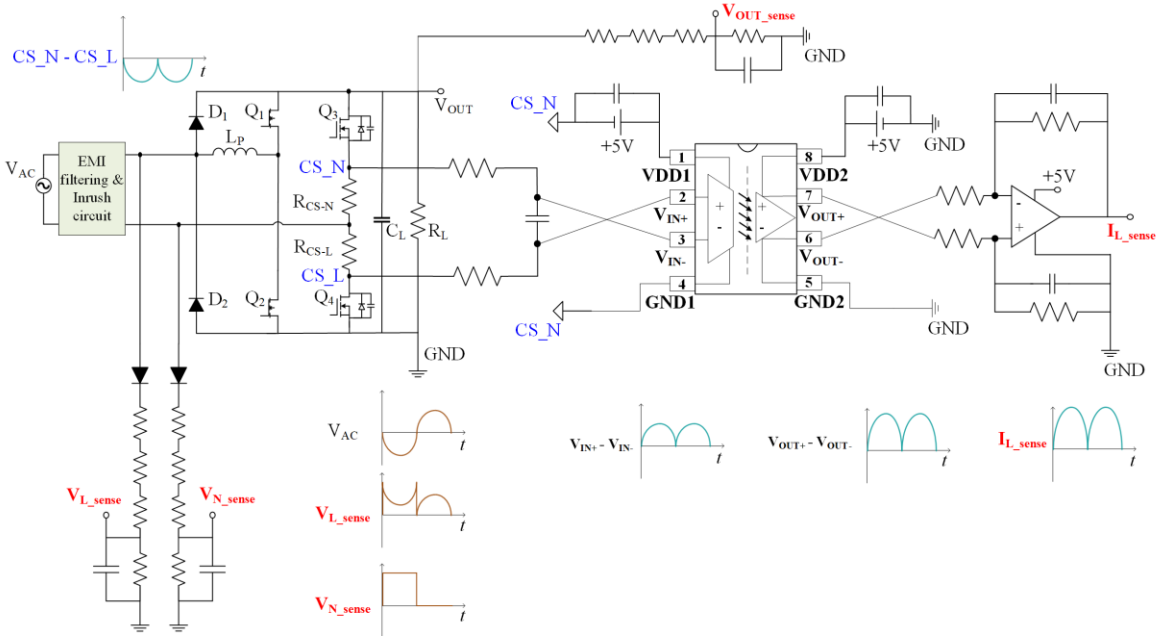

Figure 4. Sensing circuit of the proposed design

Similar to most members belonging to the bridgeless PFC family, the current of totem-pole PFC rectifier also withstands a fluctuating input line in regard of the output voltage ground and a

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continuous shift of direction due to the inactivity of a boost converter branch in either cycle, an isolation methodology is thus a must. In addition, the totem-pole PFC controller needs rectified current reference signal rather than the AC input current to realize PFC. To accomplish the requirement, two straightforward shunt resistors R_{CS_N} and R_{CS_L} are placed between the lower switch of slow speed phase leg Q_4 and neutral terminal of AC grid, upper switch Q_3 and neutral terminal, correspondingly.

An isolated sensing solution is applied with an isolation amplifier and an operational amplifier which are assembled in series after the current sensing resistors. The +5V supply voltage for input side VDD1 in respect of CS_N point is transported from the output of a low dropout voltage regulator IC, which also drives the upper switch Q_3. The input side ground GND1 of the isolation amplifier is referred to CS_N point while the output side ground GND2 is linked to the ground of power stage. It can be observed from the Figure 4 that the waveform of I_{L_sense} with desired gain and rectified positive shape is achieved as the output of the differential amplifier. The gain of the current sensing circuitry is able to be derived as

$$K_I = R_{CS} G_{Iso} G_{OA} \tag{4}$$

R_{CS}, G_{Iso} and G_{OA} are the expressions of the resistance of the current sensing resistor, the gain of the isolation amplifier and the gain of the op-amp, respectively. The inductor current obtains the highest value when the difference in the positive input voltage and the negative input voltage ($V_{IN+} - V_{IN-}$) reaches the maximum value, which is effortlessly inferred from the component datasheet. The value of current sensing resistors R_{CS_N} and R_{CS_L} should be selected depending mainly on the estimated division between the maximum value in the differential input voltage of the isolation amplifier and the peak value of the root-mean-square value of the input current.

$$R_{CS\_N} = R_{CS\_L} = \frac{(V_{IN+} - V_{IN-})_{MAX}}{\sqrt{2} I_{RMS\_MAX}} \tag{5}$$

Besides, in this design, the designated shunt resistors are non-inductive resistors in an attempt of minimizing the di/dt slew rate induced voltage spikes which might have a detrimental impact on the operation. In the aspect of sensing the input voltage, a low frequency transformer is regularly employed. Nevertheless, the transformer is costly, bulky and occupies a large area of the circuit, which makes it incompatible with the high efficiency-oriented application. The higher linearity optical coupler with wide operating range is a common solution for the voltage sensing as well. However, in comparison with the voltage dividers, the optical coupler is much more complicated. In this paper, the Line AC voltage and Neutral AC voltage are sensed separately by the voltage divider and then filtered to eliminate high frequency interference noises by low-pass filter with waveforms as displayed in Figure 4. Hence, the targeted sinusoidal V_{AC} is obtained through the rectification function in the DSP control block. The feedback circuit of DC output voltage is also implemented by a voltage divider in combination with an RC network for the simplicity.

2.3. DSP Control Block

The functional block diagram of the controller inside the DSP is introduced in Figure 5. In this paper, the controller is implemented by using digital control with 60 MHz Texas Instrument core - TMS320F28035. It is necessary to use four input signals I_{L_sense}, V_{OUT_sense}, V_{N_sense} and V_{L_sense} for compensators as well as different functions. These sensed signals are converted to digital by using 12-bit ADC modules for sampling and conversion process from the DSP. And then, based on the control method described in section 3, the duties for the master switch and the slave switch can be determined and implemented through enhanced pulse width modulation (EPWM) modules. In this way, by using the auxiliary control circuit, the accurate gating signals are delivered for controlling all switches at any operating condition by the logic control circuit. It is worth noting that the grid voltage V_{AC} is measured by sensing independently the V_{N_sense} and V_{L_sense}, thus the V_{AC_DSP} which is used for calculation in DSP should be derived as

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$$V_{AC_{DSP}} = \begin{cases} V_{L\_sense} - V_{N\_sense} & \text{when } V_{L\_sense} > V_{N\_sense} \\ V_{N\_sense} - V_{L\_sense} & \text{when } V_{N\_sense} > V_{L\_sense} \end{cases} \quad (6)$$

When the converter operates in the positive AC semicycle, the V_{AC_DSP} is equal to the difference of V_{L_sense} - V_{N_sense} while the V_{AC_DSP} is equal to the difference of $V_{n\_sense} - V_{L\_sense}$ during the negative half-line cycle.

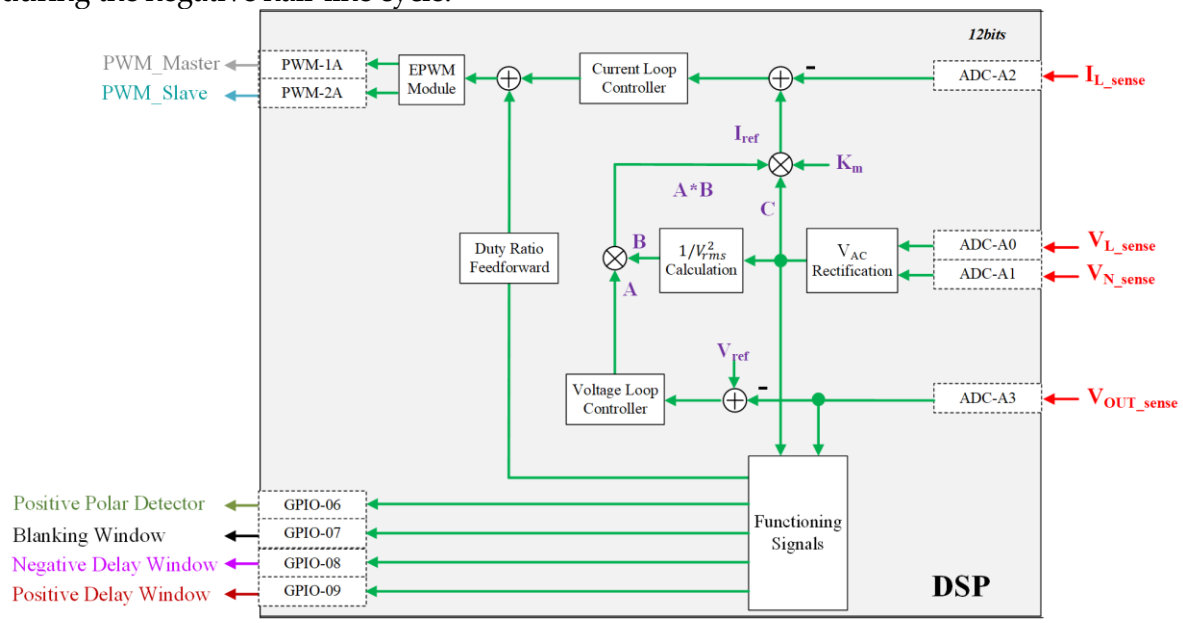

Figure 5. Functional block diagram of the controller within the DSP

Figure 5 also shows that the totem-pole PFC controller composes of two control loops: the voltage control loop is a low frequency outer loop which regulates the output voltage of boost power stage to be equal to a desired reference value while the current control loop is a high frequency inner loop whose target is to make certain the input current shape to be a replica of the AC voltage shape. In terms of the voltage control loop, V_{OUT_sense} is subtracted from the reference output voltage V_{cmd}. The resulting difference signal $V_{cmd} - V_{OUT\_sense}$ is then fed intro the voltage loop controller. The bandwidth of voltage loop must be far less than 120Hz to sufficiently attenuate second harmonic of output voltage. As for the current loop, I_{L_sense} is subtracted from I_{cmd}. The resulting difference signal ($I_{cmd} - I_{L\_sense}$) is then fed into the current loop Type II controller, whose output is sent to the EPWM module. However, only current loop controller cannot make the power qualities meet the requirements. An advanced technique, so called duty-ratio feedforward from [34], is combined with this duty cycle to create the PWM_Master and PWM_Slave in a suitable way. A deadtime is accompanied between these two EPWMs in the middle of switching events to be immune to shoot-through conditions while the master and slave switches fleetingly turn off. Moreover, it is important to note that the other four functioning signals Positive Polar Detector, Blanking Window, Negative Delay Window and Positive Delay Window are fashioned for different purposes, which is stated more visibly in the following auxiliary circuit.

2.4. Auxiliary Logic Circuit

The establishment of the auxiliary control logic circuit is based on the idea about exporting the turn-on and turn-off sequence of four switches Q_1, Q_2, Q_3 and Q_4 in a smooth and simple way. As shown in Figure 6, a straightforward signal sequence (in the left-hand side) and an auxiliary control logic circuit (in the right-hand side) are further elaborated to generate the expected signals for all switches.

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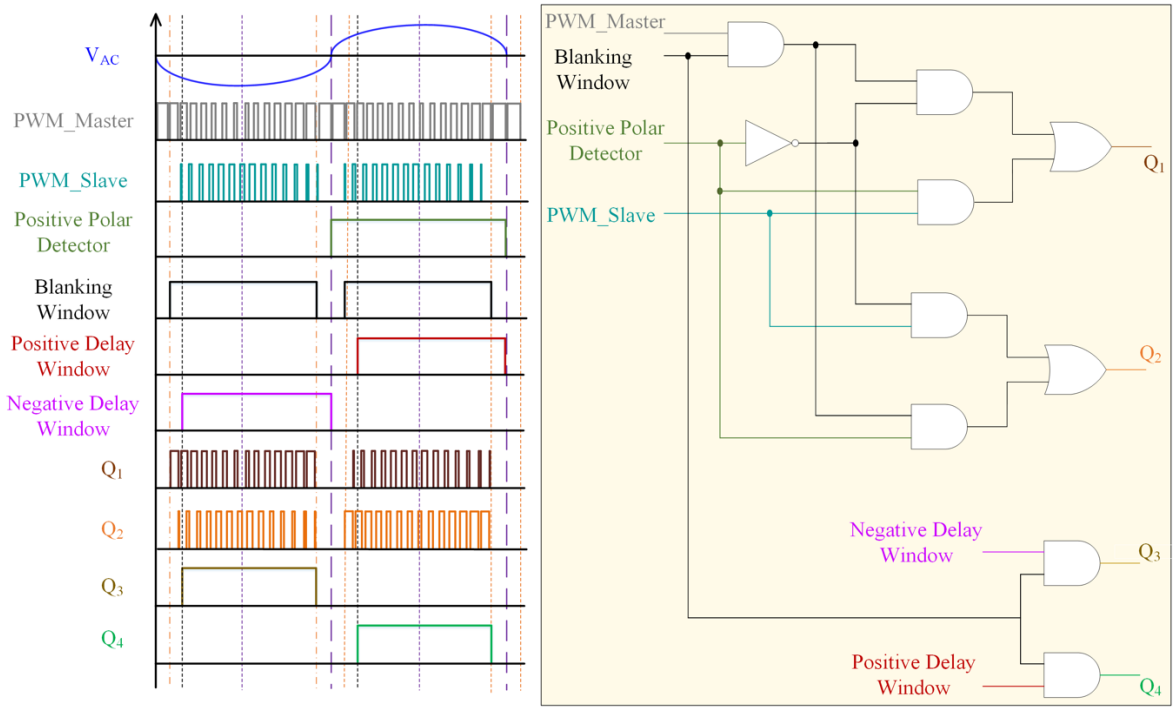

Figure 6. Key signal sequence (left) and auxiliary logic circuit (right) of the proposed control structure

There are six input signals of the control subcircuit sent from the DSP controller and four targeted output signals transmitted to the gating driver of switches. Amongst them, the duty cycle for the main switch PWM_Master and the duty cycle of the synchronous-rectifier switch PWM_Slave are directly routed from the output of the controller. One of the four remaining functioning-signals is Positive Polar Detector formed from sensing the input grid voltage V_{AC} to decide which switches work according to the distinct operating mode of the totem-pole PFC rectifier. The output signal of Positive Polar Detector is HIGH when the grid voltage goes positive. On the other hand, the output signal of Positive Polar Detector goes LOW as the grid voltage is negative. A NOT logic gate is used to invert the Positive Polar Detector signal in effort of avoiding the shoot-through of two fast-speed switches at the same time. These signals also have a capability of enabling and disabling AND gates to switch the PWM sequences alternately for each half-line period. Meanwhile, a Blanking Window is supplemented for safety purpose under abnormal conditions in which all switches are turned off during the commutation intervals at the boundaries of positive and negative half-line cycles. For the reason of evading unwanted issues instigated by the crossover current spikes, the Negative Delay Window and Positive Delay Window are proposed to insert the delay time between turn on moments of the fast speed leg and slow speed leg. More specifically, the Negative Delay Window and Positive Delay Window are realized by turning on Q_3/Q_4 after Q_1/Q_2 experiences a turn-on in either semicycle such that the slow-speed leg switches can completely reverse recover whereby the drive gating signals for line-frequency-switched devices and high-frequency-switched devices are fulfilled in an optimal way. This course is important since it contributes pointedly to downgrade the current spikes and the ITHD.

3. Firmware Design for the Control Strategy

3.1. Algorithm Flowchart

This prototype totem-pole PFC software is implemented by EPWM interrupt service routine (ISR) of DSP controller, with running all PFC functions and state machines in the periodical interrupts. In addition to the PFC functions and state machines, initializing the variables and clearing the controller parameters in the beginning handled in the main background loop. The control method is designed to form one compact software and can be easily integrated into DSP controller of the

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application for easing to use in the industrial environment. The entire PFC control software is implemented in two ISRs. The current loops are executed in the fast interrupt every 15.38 μs, the voltage loop and state machine are executed in the slower interrupt with a 30.76 μs period of execution. The flowchart of the ISR loop is shown in the following Figure 8.

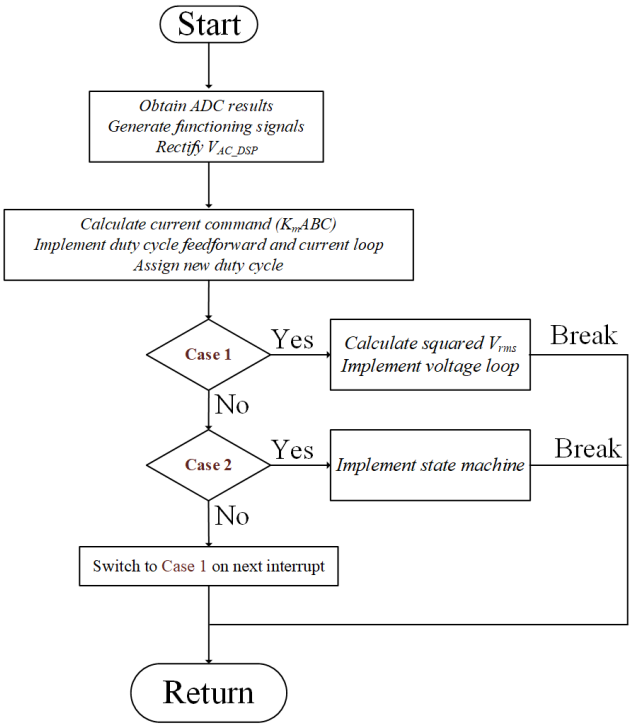

Figure 8. The principal software flowchart of the proposed control structure

The flowchart for PFC implementation is explained more detailed as below. These critical tasks are assigned in the ISR loop.

- *Obtain ADC results*: The task aims at acquiring 4 ADC channel values comprising the Line voltage sensing signal, the Neutral voltage sensing signal, the inductor current sensing signal and the output voltage sensing signal.
- *Generate functioning signals*: In the hardware design, employing the proper driving signals at auxiliary logic circuit for controlling GaN switches and MOSFETs results in the need of generating functioning signals such as Positive Polar Detector, Blanking Window, Negative Delay Window and Positive Delay Window. Accordingly, this task creates these functioning signals based on the ADC results of the Line voltage sensing signal, the Neutral voltage sensing signal and the output voltage sensing signal as aforesaid in subsection 2.3. Software counters are appropriately added to remove glitches or noises influencing these functioning signals adversely. For instance, in case of the Positive Polar Detector signal changes the state from HIGH to LOW but not at the zero-crossing zone, which enables the counter increment in a row, a threshold is programmed with such a higher value than this counter that the function can clear the improper signal. Otherwise, the controller will behave as if the AC grid swaps to negative semicycle, thus an enormous current spike will be produced by being shorted between the ground and output bus, resulting in the damage of the components.
- *Rectify Vac_DSP*: The task produces the rectified waveform (M-shape waveform) of AC mains voltage sensing signal to prepare for calculating of current command.
- *Calculate current command (ABCK_m)*: The task calculates the current command I_{cmd} where factors are established in corresponding as follows. The notation A is the output of voltage loop controller whose maximum value U_{V_MAX} and minimum value U_{V_MIN} contain

$$U_{V\_MAX} \geq A \geq U_{V\_MIN} \quad (7)$$

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Afterwards, the notation B which is the inverse of squared V_{rms} is derived to calculate within DSP by

$$B = \frac{1}{(\frac{4095}{3.3K_{AC}})^2}\frac{1}{{V_{RMS}}^2} \tag{8}$$

Where $\frac{4095}{3.3}$ is the DSP coefficient of 12-bit ADC. It should be noticed that both A and B are calculated in the previous interrupt service routine. Next, C denotes the AC mains voltage sensing signal.

$$C = \frac{4095}{3.3K_{AC}}V_{AC} \tag{9}$$

And then K_m is the multiplier gain which is specified as a constant designed in advance. To choose the proper K_m, some extra steps should be taken. The first action is expressing the current command from equations (7), (8) and (9)

$$I_{cmd} = A(\frac{1}{\left(\frac{4095K_{AC}}{3.3}\right)^2}\frac{1}{{V_{RMS}}^2})(\frac{4095}{3.3K_{AC}}V_{AC})K_m \tag{10}$$

Simplifying and substituting $V_{AC} = \sqrt{2}V_{RMS}|\sin(\omega t)|$, the equation (10) becomes

$$I_{cmd} = A(\frac{1}{\frac{4095K_{AC}}{3.3}}\frac{1}{V_{RMS}})(\sqrt{2}|\sin(\omega t)|)K_m \tag{11}$$

Meanwhile, the measured current value is given within DSP by

$$I_{msd} = I_{AC}\frac{4095}{3.3}K_I \tag{12}$$

Substituting $I_{AC} = \sqrt{2}I_{RMS}|\sin(\omega t)|$, the equation (12) becomes

$$I_{msd} = (\sqrt{2}I_{RMS}|\sin(\omega t)|)\frac{4095}{3.3}K_I \tag{13}$$

Following the current control law, the measured current value must be equal to the commanded current value $I_{cmd} = I_{msd}$, combining the equation (12) and (13) with $P_{AC} = V_{RMS}I_{RMS}PF = V_{RMS}I_{RMS}$due to the close-to-unity power factor, K_m is deducted as

$$K_m = P_{AC}\left(\frac{4095K_{AC}}{3.3}\right)^2\frac{K_{AC}K_I}{A} \tag{14}$$

- *Implement Duty-cycle feedforward and current loop*: The current loop controller is designed and implemented by DSP to catch improved duty cycles for PWM_Master and PWM_Slave.
- *Assign new duty cycle*: After implementing duty feedforward and current loop controller, the new duty value is available. Afterwards, an upper end limitation is imposed on this updated duty ratio to prevent from the excessive current and the instability when working at high duty ratio. Therefore, the objective of this task is assigning the novel duty cycle value to assure the duty of EPWMs signals placed on the correct gate drivers signal pin.

3.2. State Machine

Referring to Figure 9, five specific states of PFC state machine are described briefly with the state diagram.

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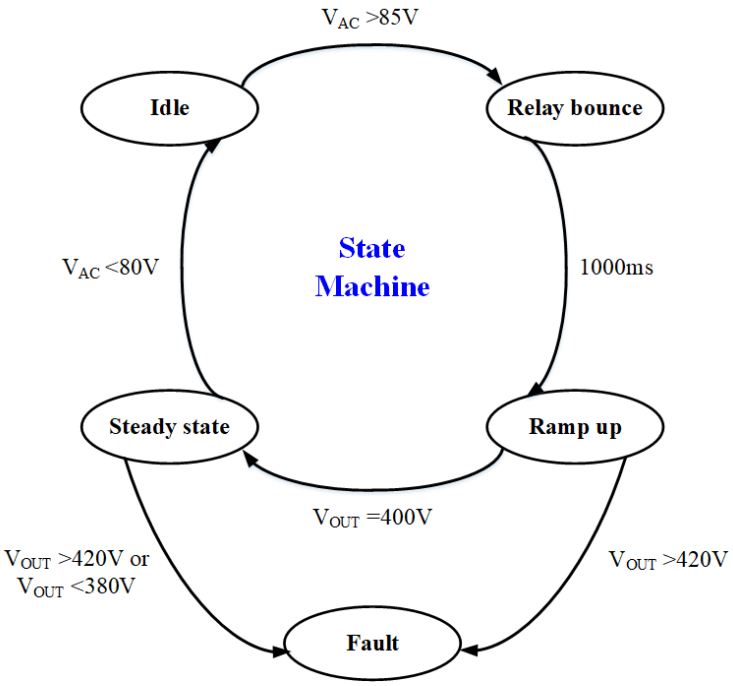

Figure 9. PFC state diagram running in ISR every two-switching cycle

- **Idle**: Inrush current relay is turned off rather than bypassing the inrush current resistor in the beginning. Inrush current relay is turned on (bypass the inrush current resistor) and moving to next state if V_{AC} is continually higher than 85 V during 100 ms. In the beginning of start-up, both outputs of the voltage loop and control loop are zero.
- **Relay bounce**: Checking V_{AC} is still higher than 85 V after the relay bounces. If V_{AC} is stable in a duration of 1000ms, the controller is enabled.
- **Ramp up**: The output voltage value is elevated linearly. The controller forces the output voltage to follow the reference value until the output voltage reaches the demanded value. This leads to protecting the circuit from the excessive starting-up current.
- **Steady state:** The normal condition of PFC operation and checking of over voltage condition.
- **Fault**: The incidents of fault state concerning the output voltage are determined by being out of range. Once the voltage exceeds more or less than 5% of its nominal value, the controller will activate the over voltage protection.

4. Experimental Results

To confirm the functionality and to measure the efficiency of the circuit, a pertinent experimental arrangement is formed. Figure 10 depicts a global view of the realized converter whereas the Table 1 tabulates the specification of the prototype. A 2.6 kW totem-pole PFC prototype is built with the standard grid voltage range of 90 to 264 VAC. The control daughter card is attached on the mother power stage board and works as the brain for the whole converter. The needed value for current sense resistors is 10 mOhm for each side of the slow-speed leg to compromise the measurement accuracy and the power dissipation as mentioned previously. To satisfy the required wattage, four 0.04 Ohm resistors are stacked in parallel. The footprint dimension of the designed circuit is 11.9 cm × 9.6 cm × 5.4 cm.

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Table 1. The specification and the parameters of the design

Item	Value/Model
Input supply voltage V_{AC}	90~264 Vac
Output voltage V_{OUT}	385 Vdc bus nominal
Input frequency f_{line}	43-63 Hz
Output power P_{OUT}	1 kW @ 90-132 V, with 115 V nominal 2.6 kW @ 180-264 V, with 230 V nominal
Switching frequency f_s	65 kHz
Semiconductor device Q_1, Q_2	GaN System's GS66516B as fast speed leg
Semiconductor device Q_3, Q_4	IXFH60N65X2 as slow speed leg
Power inductor L_P	604 μH
Output capacitor C_L	2 * 560 μF
Controller core	DSP TMS320F28035
Power factor	≥ 0.99
Peak efficiency	> 99.1%
Harmonic content	< 2% at 230 V and full load

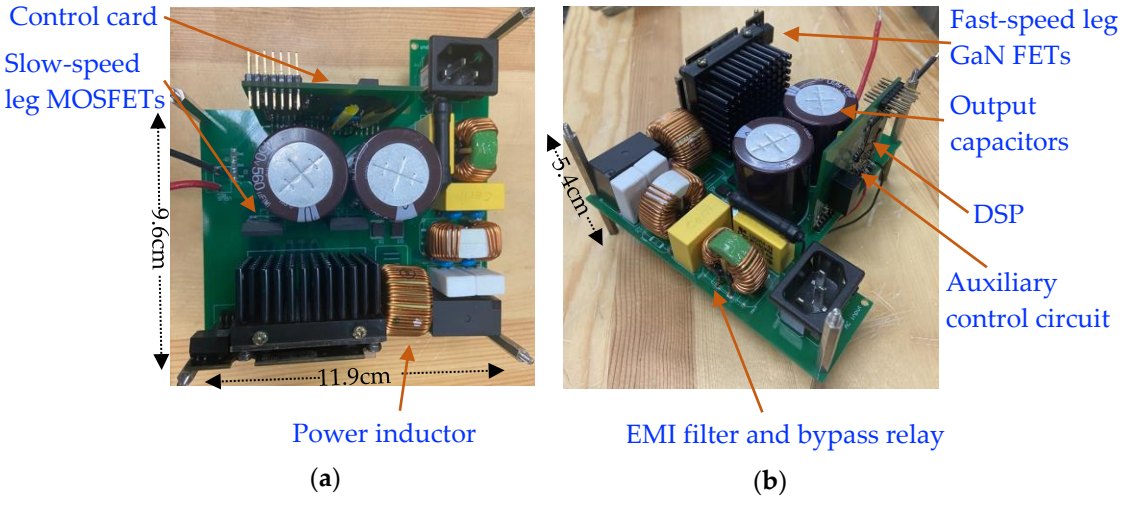

Figure 10. Perspective of the hardware prototype: (a) bird's eye view; (b) top side view

Figure 11 displays the experimental waveform of the input voltage and the inductor current under the full load condition of the 2.6 kW at 230 VAC and the 1 kW at 115 VAC. It can be shown that the inductor current (channel 2) is perfectly sinusoidal and in phase with the input voltage (channel 1) seamlessly.

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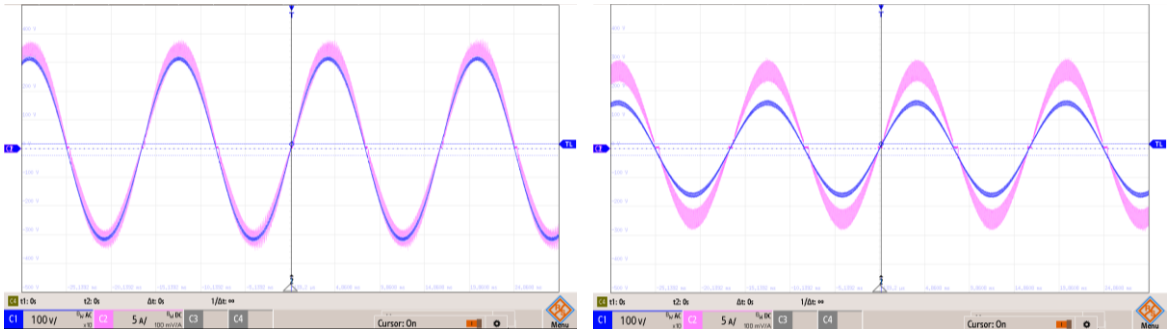
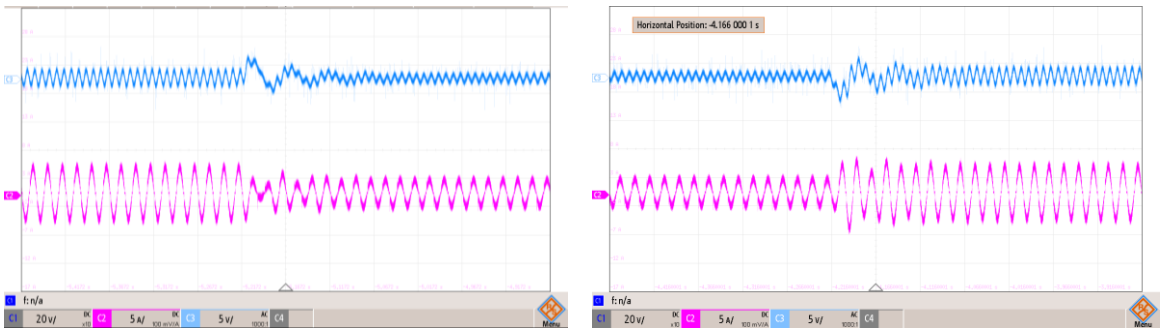


(**a**) (**b**)

Figure 11. Experimental waveforms of the totem-pole PFC rectifier running (a) at 230 VAC input and 2.6 kW output load; (b) at 115 VAC input and 1 kW output load (For both left and right figures: V_{AC} 100 V/division, channel 1 – I_L 5 A/division, channel 2. Time base 5 ms/division)

In order to reveal dynamic responses of the prototype, a load step from low to high and from high to low load with the output voltage tightly regulated at 385 VDC. Figure 12(a) and (b) display the transition conditions of load from 100% to 50% and 50% to 100%. The light blue curve shows the DC link voltage on the output terminal whereas the purple curve represents the inductor current. The input current hits to the new static operation point shortly after few mains period with a trivial overshoot at first. The bus voltage fully recovers within roughly 165 ms and discloses the maximum deviation of 24 V.

The prototype of the totem-pole PFC rectifier is also tested under start-up scheme of the converter at the mains voltage of 90 VAC and 230 VAC with a minimum load of 300 mA, as revealed in Figure 13(a) and 13(b). The light blue curve shows the DC link voltage on the output whereas the purple curve embodies the inductor current and the dark blue curve depicts the input voltage. Referring to these figures, the complete start-up procedure takes approximately 1950 ms. The input AC voltage achieves the start value after several first charging pulses. Subsequently, the input current rises in a linear way until the bus voltage achieves the designed value. As soon as V_{OUT} reaches to this point, the state machine turns into the **Steady state** and the circuit jumps to the regulation operation. This feature can deal with excessive power dissipation and reduce the device stress.



(**a**) (**b**)

Figure 12. Measurement result of the transient response (a) from 100 to 50 percent load; (b) from 50 to 100 percent load. (For both left and right figures: I_L 5 A/division, channel 2 – V_{OUT} 5 V/division in AC coupling mode, channel 3. Time base 50 ms/division)

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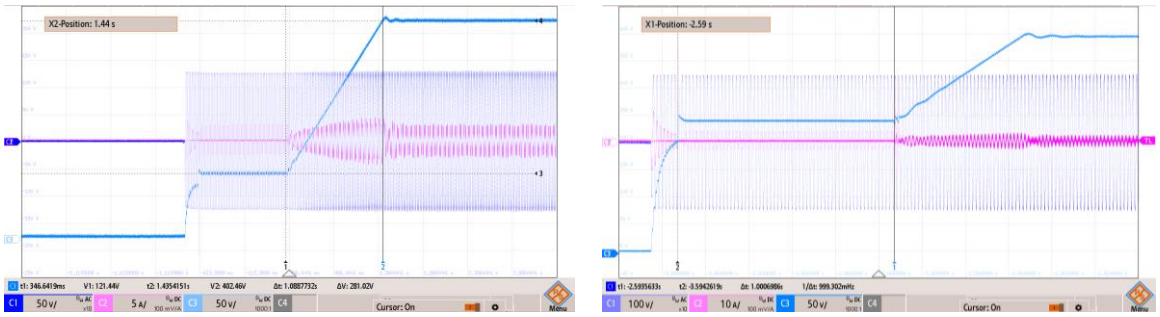

(a) (b)

Figure 13. Start-up waveforms of the totem-pole PFC (a) at 90 VAC with 300 mA load current; (V_{AC} 50 V/division in AC coupling mode, channel 1 – I_L 5 A/division, channel 2 – V_{OUT} 50 V/division, channel 3. Time base 500 ms/division) (b) at 230 VAC with 300 mA load current (V_{AC} 100 V/division in AC coupling mode, channel 1 – I_L 10 A/division, channel 2 – V_{OUT} 50 V/division, channel 3. Time base 200 ms/division)

The efficiency curve with relation to the continuous output power at 230 VAC line voltage is shown in Figure 14., where the efficiency achieves 99.14% at nominal high line condition and maintain over 98.5% for the whole load range.

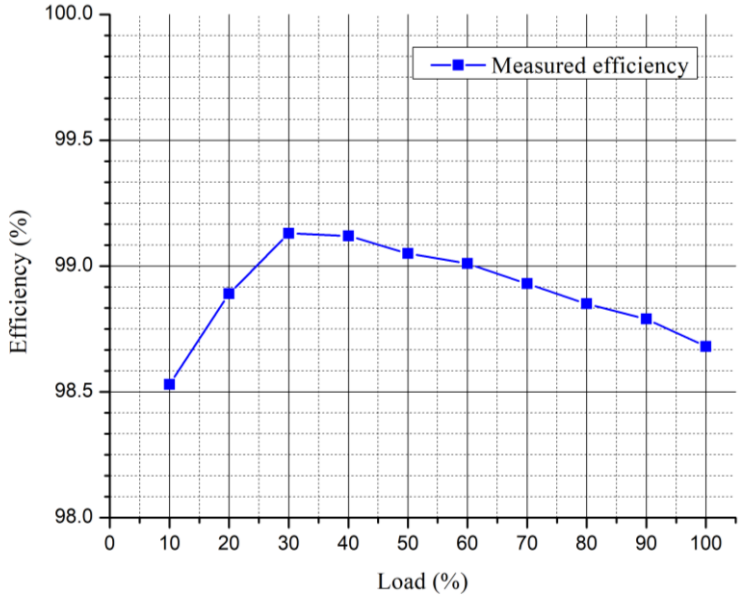

Figure 14. The efficiency curve with the overall load range of 2.6 kW at high line condition 230 VAC

The measured PF and ITHD values, which are the major reference for evaluating the power quality performance, are essentially decided by the control methodology and compensation rather than the power stage. Table 2 summarized the measured PF and THD of the proposed control structure at the minimum and maximum input AC voltage over ten different load levels. The PF and THD measured at maximum line full load are 0.998 and 2.79%, respectively whereas those at minimum line are 0.999 and 1.76%, respectively. Meanwhile, Figure 15 shows the power factor at low input voltage 115 VAC (dot-dashed line) and high input voltage 230 VAC (solid line). The power factor higher than 0.99 from 30% load to 100% load.

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Table 2. The measured THD and PF at the line voltage of 90 V and 264 V

Load (%)	V_{AC} = 90 V		V_{AC} = 264 V	
	PF	THD (%)	PF	THD (%)
10	0.981	6.13	0.911	8.72
20	0.991	4.55	0.983	4.61
30	0.996	3.18	0.988	3.79
40	0.997	2.67	0.993	3.51
50	0.998	2.39	0.995	3.31
60	0.998	2.17	0.997	3.17
70	0.998	2.08	0.998	3.08
80	0.999	2.01	0.998	2.91
90	0.999	1.81	0.998	2.83
100	0.999	1.76	0.998	2.79

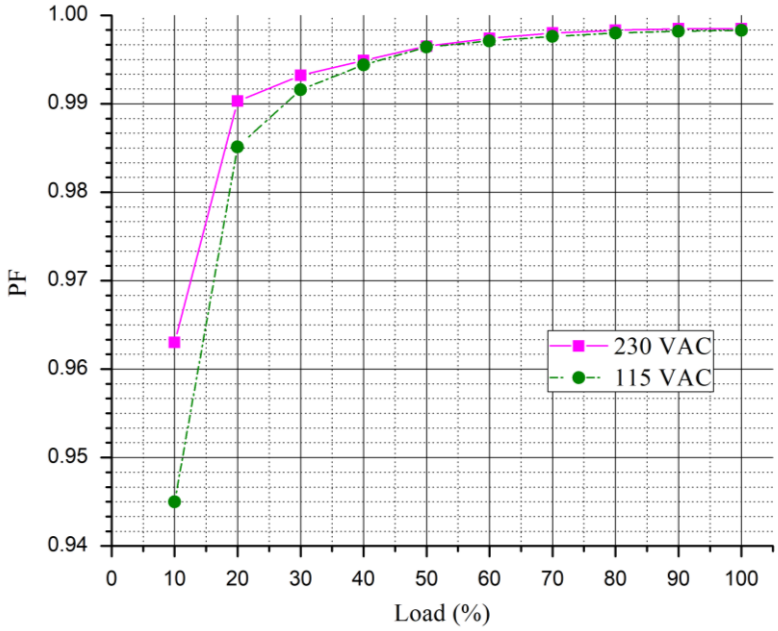

Figure 15. The measured PF curve with respect to the overall load range at low line 115 VAC and high line 230 VAC

As illustrated in Figure 16, the ITHD gains a further improvement when applying the functioning signals around the zero crossing. The blue curve shows the ITHD values with functioning signals applied while the red curve presents those without functioning signals. Compared to the ITHD of 3.74% under 230 VAC testing condition of the control strategy without functioning signals, the ITHD with offered functioning signals achieves 1.52% at the mid-range of output power and is always smaller than 3% only except at 10% load condition. As the power level is very low, the input of the amplifier for the current measurement is very small whereby the sensing current signal has larger error unmatched with the current reference, leading to a higher ITHD value. Such figure also shows the current spikes at zero crossings notably disappear when applying the functioning signals.

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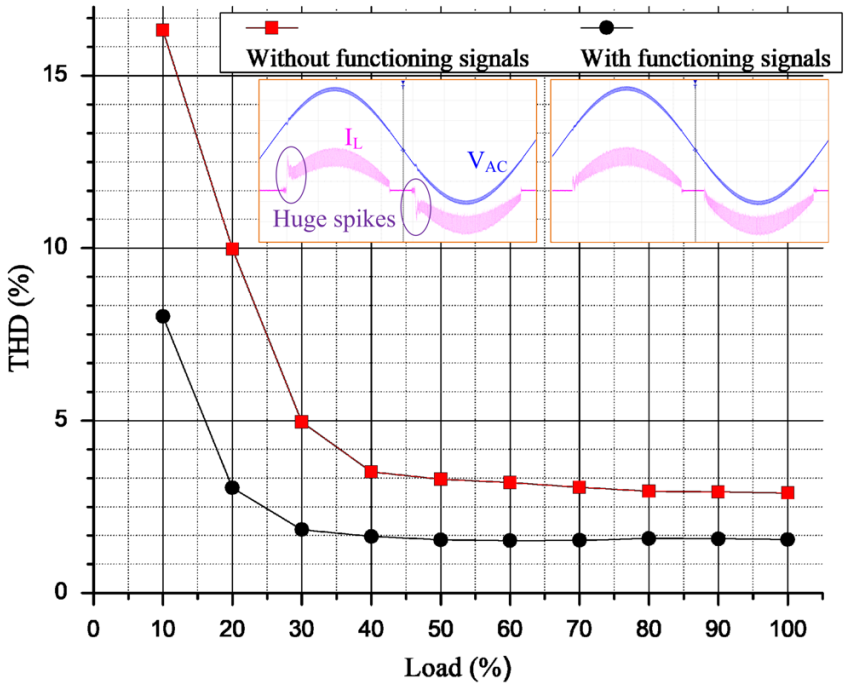

Figure 16. The measured ITHD and waveform comparisons with both presence and absence of the functioning signals at the grid voltage zero-crossing zone over the full range of load

5. Conclusions

The proposed solution has been implemented by combining hardware and firmware to optimize the performance of the e-mode GaN-based totem-pole PFC rectifier for grid-connected ESS no longer only at rated power but also throughout a wide load range. The adopted control structure has merits of easy implementation, simple algorithm with a digital controller on the DSP TMS320F28035, which is tough to be accomplished with a more intricate model owing to the obligatory calculation attempt. The analytic and experimental results on a 2.6 kW prototype have been demonstrate the excellent performance where the power factor can be improved to nearly unity, the efficiency surpasses 99% over the large load range and the input current total harmonic distortion reduces to 1.52. The control also diminishes considerably the component stress during soft start up procedure. The steady-state and dynamic behaviors are proceeded at a PCB size of 119 mm × 96 mm and a height of 54 mm to justify the prototype's feasibility as well.

Author Contributions: The author N.-N.D. conceived the control design method, verified with simulation and experiments, debugged the system and wrote the paper. The author B.-S.H. was responsible for investigating the literature resources, layout and hardware consideration. The author T.-T.N. was responsible for building some parts of hardware and software, as well as carrying out the experiments. The authors N.-T.P. and J.-H.W. were responsible for testing the circuit and data acquisition. The authors H.-J.C. and Y.-C.L. supervised the research, provided materials for experiments, and reviewed the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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