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One Cycle Control of A PWM Rectifier a new approach

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Abstract: In this work, it is analyzed a Digital Signal Processor, DSP, based One Cycle Control, OCC, strategy for a Power Factor Corrector, PFC, rectifier, which presents Common-mode Voltage, CMV, immunity. The proposed strategy utilizes an emulated-resistance-controller in closed-loop configuration to set up dc-link voltage and achieve unity power factor, UPF. It is shown that if PFC can achieve UPF condition and if phase voltage is only affected by CMV, then phase current is free from CMV, as well as a lead-lag compensator, LLC, to average phase current. Another possible condition is also analyzed. The proposal is verified by simulation and experiments.

Keywords: Power factor corrector; One cycle control; Common-mode voltage; Common-mode current.

0. INTRODUCTION

One-Cycle Control theory was proposed in [1]. OCC is a nonlinear control theory utilized to control switching converters with only one switching cycle. The controller achieves instantaneous dynamic control of an average value of one of the switching variables from the converter after a transient. The most important feature of OCC is the control of the carrier amplitude, in contrast to the Pulse Width Modulation, which controls the variable. One-Cycle control provides low complexity and low-cost implementation, disturbance rejection, robustness, good stability, and fast dynamic response. OCC has been mostly utilized in the literature to control power factor correction, and it has been applied in modular multilevel converters [2], a grid-tied single-stage buck-boost DC-AC micro-inverter [3] and Vienna Rectifiers [4], a novel multi-converter-based unified power quality conditioner (MCB-UPQC) [5]. The study and analysis of harmonics, energy consumption, and power quality of light-emitting diode (LED) lamps equipped in building lighting systems [6]. A novel, two-stage and hybrid approach based on variational mode decomposition (VMD) and the deep stochastic configuration network (DSCN) for power quality (PQ) disturbances detection and classification in power systems [7]. In power quality, two of the most significant concerns are harmonic currents and power factor, PF, caused by nonlinear loads. While the former may cause false triggering of protection devices and malfunctioning of motors and transformers, the later reduces available active power at the utility grid. The past few decades have witnessed extensive studies on power quality, mainly to satisfy specific standards, i.e., IEEE 519 – 1992 [8], that recommend limiting harmonics distortion. To solve these issues for

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end-consumer, a PWM rectifier is used to substitute each nonlinear load by an active resistance seen from the utility grid [9]. In that sense, this rectifier always tries to achieve unity power factor, UPF. If the grid voltage is sinusoidal, then the current drawn by the rectifier must be sinusoidal and in phase with the voltage, avoiding any current harmonics. Several methods have been proposed to achieve UPF in PWM rectifiers based on the enhanced control-loops concept [10], i.e., an inner current, an instantaneous power loop, and an outer voltage loop. To force the phase-current to follow voltage loop reference, it is necessary to sense three-phase voltages, a dc-link voltage, and three-phase currents [11] and eventually, use a phase-locked loop, PLL, to guarantee voltage and current synchronization [12]. The control techniques based on this concept use space vector modulation, SVM, Park/Clarke transformations and control coupled terms, like voltage oriented control, VOC, [14], direct power control, DPC, [13], model predictive control (MPC) [15], deadbeat control [16], fuzzy control [17] and neural networks [18]. Nevertheless, these methods are time-consuming, as they rely on system parameters, requiring complicated online calculation. Resistance-emulation is another technique employed in PWM rectifiers, generally using average value and PWM modulators. In this technique is always assumed that UPF is already achieved. There are two main methods based on open-loop, and closed-loop controls [9]. Open-loop controls estimate emulated-resistance, assuming a fixed value [19], while closed-loop methods adjust the emulated-resistance value by feedback [20]. Although these techniques were proposed for single-phase boost converters with diode rectifiers, they are complicated to implement as they employ the four arithmetical operations.

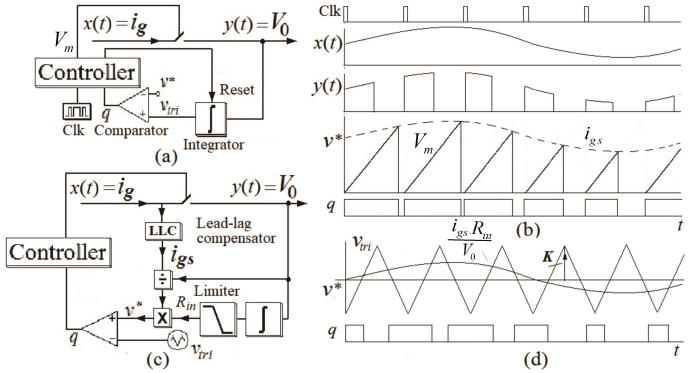

Figure 1. (a) Hardware OCC. (b) Associate waveforms.

Among open-loop methods, One Cycle Control, OCC, originally a hardware technique [21], Figure 1(a), has implemented by a few commercials ICs, or a single chip, constituting a kind of cost-effective solution. It uses a variable sawtooth-carrier-amplitude, Figure 1(b), and only adding and subtracting operations, contributing to its arithmetic simplicity and performing its control tasks in the only one switching cycle, therein the name OCC, despite this technique was also proposed for three-phase, six power-switches boost-converter. Besides enhanced control-loops technique, OCC has not utilized phase-locked loop (PLL), Park/Clarke transformations, or online parameter calculations, but achieves a high dynamic response and satisfies UPF condition. Moreover, it eliminates the need for three grid-voltage sensors, which adds control and hardware simplicity. Although this technique was applied several times, i.e., inactive power filters (APF) [22], [23], flexible ac transmission systems (FACTs), [28] and photo-voltaic grid-connected inverters (GCI) [24], [32], [27], OCC has presented such serious instability problems [21], [29], [30], which to solve them, it was necessary to add extra circuitry, sacrificing control and hardware simplicity.

Hence, in order to preserve control and hardware simplicity, OCC was emulated in a DSP system. So a DSP-based software-OCC was proposed in [31], see Figure 1(c) and Figure 1(d). This version enhances OCC with DSP calculation capability and uses closed-loop resistance emulation. Then, the software offers more possibilities to apply OCC to the most complex control issues than those of hardware [33], [34], [35]. Besides, unlike enhanced-loops methods mentioned above [11], [12], [14],

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[13], [15], [16], [17], [18], software-OCC does not need PLL, nor Park/Clarke transformations, nor online parameter calculations, achieving some control simplicity. However, it was not reported any further analysis, in spite DSPs have already applicated to OCC as a control core, i.e., for motor drivers [36], [37], and photovoltaics [32], while OCC runs as a sort of auxiliary circuit. Previous treatments to solve stability problems at no-load have sacrificed OCC simplicity once they use an additional bulky resistor at dc-link [21], [30]. Instead, in [38], [39], [26] to decrease current distortion, an artificial phase-current was created. However, despite the efforts, instability remains when load current falls below a certain limit [43], [28], [42]. On the other side, due to a lack of PLL synchronization, OCC has experienced PF derating at high-load [21], [39], [30], [42], [26]. To avoid this, OCC has sacrificed its simplicity again as they use input voltage multiplexers, and other additional analog and logic circuits [43], [23], [28], [42], [25], requiring the knowledge of 600 angular sectors and to select positive and negative peak voltages as reference current vectors. In [29], [41] was also necessary to sacrifice OCC simplicity by adding a few analog multipliers and heavy and bulky inductors (10mH), but sacrificing the cost-effectiveness of OCC solution. Hence, despite all the efforts, it is apparent that, to date, OCC has been not able, whatsoever, to solve its own problems fully. Above all, even though a few hardware methods have solve partially OCC stability issues at no-load [21], [38], [39], [26], [41], and at high-load [43], [29], [42], [25], they were never reported working together over a wide load range. Thus, one of the paper's major contributions is to present a simple and stable OCC system working at no-load and high-load.

In this paper, analysis, simulation, and experimental results prove, based on the resistance-emulated controller [31], that software-OCC does not possess instability issues and preserves OCC simplicity and dynamical response, also satisfying UPF condition. The paper is organized as follows: Section 1 presents a review of software-OCC fundamentals. Section 2 . shows OCC issues and discusses software-OCC solving method. Section 3 depicts DSP implementation and discusses the cost-effectiveness of software-OCC. Simulation and experimental results are shown in Section 4. Conclusions are shown in Section 5 .

1. FUNDAMENTALS Of SOFTWARE-OCC

Software-OCC is a PWM, where an average phase-current compares to carrier and control system is integrated into the modulator, similar to hardware-OCC of Figure $1(c)$ [21]. Nevertheless, unlike hardware-OCC, this version is not a circuit, but a software. Hence, software-OCC implements OCC features by programming embedded DSP devices and using just a few equations. However, a high-performance OCC system is obtained, as using a high-frequency DSP, the one switching-cycle control can be guaranteed. Figure $2(a)$ displays a three-phase, IGBT PWM rectifier. As in hardware-OCC, it is assumed that,

- The switching frequency f_C is much higher than line frequency f, hence the switching period T_C is much lower than the line period T, so $f_C >> f$ and $T_C << T$.
- The switches in each leg operate in a complementary fashion, i.e., the duty cycle for the upper and bottom switch is d_g and $d_{gn} = (1 - d_g)$, respectively $(g = a, b, c)$, $0 < d_g < 1$.
- Input impedance seen from the grid is a resistance, similar to the resistance emulation concept in [9]. Besides, software-OCC, Figure $1(c)$, present the following differences from hardware-OCC,

- i)Multipliers and dividers presence, as they are not much DSP time-consuming [44].
- ii) The average method, i.e., a Lead-Lag compensator, LLC, Figure $1(c)$, decreases delay response caused by the lagging part, using a leading constant.
- iii) Carrier generation uses a triangular waveshape, Figure $1(d)$, instead of a sawtooth carrier in the hardware OCC.
- iv) Fixed amplitude carrier because of a software DSP limitation.
- v) Closed-loop emulated resistance-control, guaranteeing UPF by feedback.
- vi) Use of limiters at resistance control output.

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Except for iv), these differences are a result of superior software-DSP-calculation capability over hardware technique. Applying Kirchhoff voltage law to the $r-L$ branch of Figure 2,

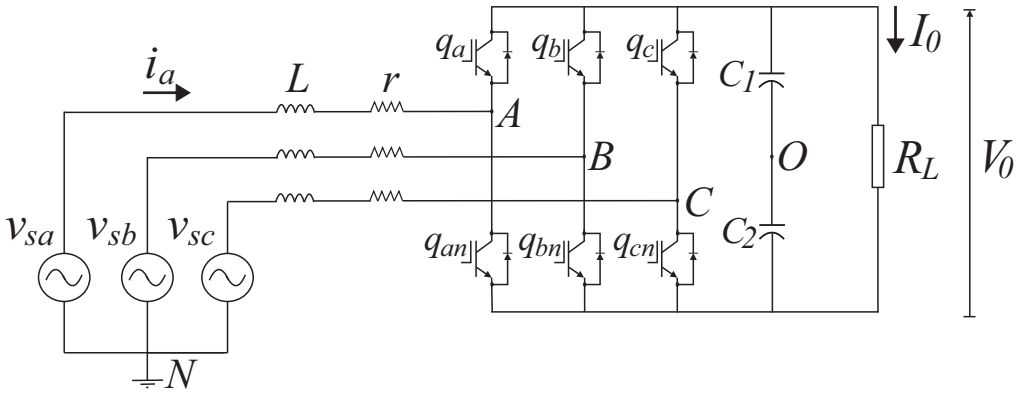

Figure 2. (a) Three phase, PWM rectifier.

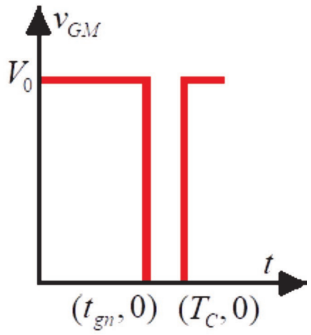

Figure 3. (b) Pole voltage, v_{GM}.

$$\begin{aligned} v_{Sa} - ri_a - L\frac{di_a}{dt} &= v_{AN} + v_{NO} \\ v_{Sb} - ri_b - L\frac{di_b}{dt} &= v_{BN} + v_{NO} \\ v_{Sc} - ri_c - L\frac{di_c}{dt} &= v_{CN} + v_{NO} \end{aligned} \tag{1}$$

where r is inductor resistance, L is inductor inductance; v_{Sg} and i_g are grid voltage and phase current, respectively; v_{GN} is pole voltage $(G = A, B, C)$, O is the middle point of dc-link capacitors C_1 and C_2, v_{NO} is the voltage between neutral of the utility grid and middle point N of dc-link voltage, and V_0 and I_0 are dc-link voltage and current respectively.

1.1. *Analysis of voltage v_{NO}*

Examining the former equation, it is apparent that to obtain an exact expression for phase-current, it is necessary to find an analytical expression for voltage v_{NO}. However, although some previous works indicate that this voltage does not depend on grid frequency [14], [40], the mathematical proof is missing. It is always possible to bypass the problem by assuming some control strategy, as it allows additional simplifications, [45], [46]. Hence, considering a balanced system,

$$\begin{aligned} v_{Sa} + v_{Sb} + v_{Sc} &= 0 \\ i_a + i_b + i_c &= 0 \end{aligned} \tag{2}$$

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Grid voltages are given by,

$$\begin{aligned} v_{Sa} &= V_p cos\omega t \\ v_{Sb} &= V_p cos(\omega t - \frac{2\pi}{3}) \\ v_{Sc} &= V_p cos(\omega t + \frac{2\pi}{3}) \end{aligned} \tag{3}$$

where V_p is voltage amplitude, $V_p > 0$. Although OCC does not use references [21],[43], for mathematical purposes, it could be useful to admit grid voltage, (3), as a virtual phase-current reference, as phase-current has the same waveshape and in phase with of the grid voltages. In addition, considering a balanced system, (2), and manipulating (1) gives:

$$V_{NO} = \frac{-1}{3}(V_{AN} + V_{BN} + V_{CN}) \tag{4}$$

The former equation says that voltage V_{NO} is related to pole voltage. Thus, to find an analytical expression for V_{NO} could be long and tedious as in a PWM modulator, pole voltage depends on Bessel functions and Fourier series [47]. The average of V_{NO} is: from the last equation,

$$\frac{1}{T_C}\int_0^{T_C} V_{NO}dt = \frac{-1}{3T_C}(\int_0^{T_C} V_{AN}dt + \int_0^{T_C} v_{BN}dt + \int_0^{T_C} v_{CN}dt) \tag{5}$$

To find average pole voltage, Figure 2(a), it should be noted that,

$$\frac{1}{T_C}\int_0^{T_C} V_{GN}dt = \frac{1}{T_C}\int_0^{T_C} V_{GM}dt - \frac{V_0}{2} \tag{6}$$

Since average value of pole voltage v_{GM} over switching period is given by (see Figure3(b)),

$$\frac{1}{T_C}\int_0^{T_C} V_{GM}dt = \frac{1}{T_C}[\int_0^{t_{gn}} V_0 dt + \int_{t_{gn}}^{T_C} 0dt] = V_0 d_{gn} \tag{7}$$

where $t_{gn} = d_{gn}T_C$. Hence, combining (6) and (7),

$$\frac{1}{T_C}\int_0^{T_C} V_{GN}dt = \frac{V_0}{2}(1 - 2d_{gn}) \tag{8}$$

Moreover, as duty cycle in a PWM modulator is proportional to its reference (3), provided that $f_C >> f$ [47]:

$$d_{gn} = D_p cos(\omega t + \phi) \tag{9}$$

where $0 < D_p < 1$, ϕ is such that, $\phi = 0$ for $g = a, \phi = \frac{-2\pi}{3}$ for $g = b, \phi = \frac{2\pi}{3}$ for $g = c$. Then, combining (5), (8) and (9) yields,

$$\frac{1}{T_C}\int_0^{T_C} V_{NO}dt = \frac{-V_0}{2} \tag{10}$$

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A common assumption in hardware OCC is that the current ripple is small and that inductor current works in current continuous mode, CCM [21], so phase-current is proportional to its average value. Thereby, using this assumption in software-OCC, phase-current can be written as,

$$i_g = \frac{K}{T_C}\int_0^{T_C} i_g(\gamma)d\gamma \tag{11}$$

where K is proportionality constant. Then, for any time $t > 0$,

$$t i_g(t) = K\int_0^{t} i_g(\gamma)d\gamma \tag{12}$$

Differentiating former equation,

$$t\frac{di_g}{dt} = (K-1)i_g \tag{13}$$

Combining (1) and (13),

$$V_{Sg} - r i_g = \frac{L}{t}(K-1)i_g = V_{GN} - V_{NO} \tag{14}$$

As input impedance seen from the utility grid is assumed a resistance (condition c),

$$V_{Sg} = R_{in}^0 i_g \tag{15}$$

where R_{in}^0 is assumed input resistance seen from the grid. This resistance is based on loss-free resistor concept [48], since it transfers all energy from the input to the output port and does not dissipate active power. Denoting $r' = (K-1)\frac{L}{t}$, where K is a constant ($K > 1$), and combining (14) and (15),

$$R_{in} i_g = V_{GN} - V_{NO} \tag{16}$$
$$R_{in} i_g = R_{in}^0 - (r + r') \tag{17}$$

Likewise, resistance R_{in} is input resistance seen from the grid. Nonetheless, this is the final resistance which is controlled by software-OCC, (21) [31], [34]. Averaging (16), it leads to,

$$R_{in}\frac{1}{T_C}\int_0^{T_C} i_g dt = \frac{1}{T_C}\int_0^{T_C} V_{GN}dt - \frac{1}{T_C}\int_0^{T_C} V_{NO}dt \tag{18}$$

Combining equations (8), (10) and (18),

$$R_{in} i_{gs} = -V_0(1 - d_{gn}) \tag{19}$$

where i_{gs} is average phase-current. The right term of the former equation is the variable amplitude of the hardware-OCC carrier. Minus $(-)$ signal means that carrier comes from $-V_0$, when duty cycle $d_{gn} = 0$, to 0 when $d_{gn} = 1$.

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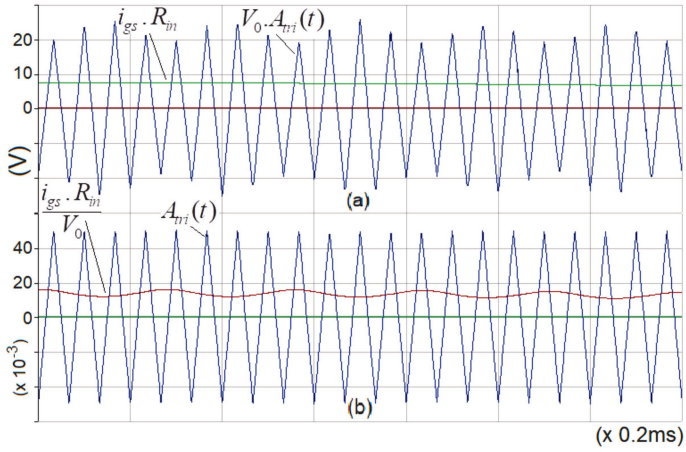

Figure 4. Software-OCC waveforms for illustration purposes. f_C = 15kHz, f=60Hz. To emphasize them, it was considered $V_0 = 450 + 67.5sin(2\pi f_2 t)V$, f_2 = 3.6kHz, $R_{in} = 1\Omega$. (a) Classical modulator, (23). (b) Modified modulator, (24).

The former equation is coherent to emulated resistance concept, as that resistance was assumed since operation beginning [9]. Furthermore, this constitutes a classical OCC equation as it achieves the same level of OCC simplicity, i.e., it uses a sawtooth carrier and does not employ coupled terms, nor Park/Clarke transformations [21] [43]. In addition, emulated resistance R_{in} satisfies,

$$V_{Sg} = R_{in} i_g \tag{20}$$

To ensure that resistance is seen from the grid, satisfying condition *c*, R_{in} can become a V_0 voltage controller. Because if R_{in} is a V_0 controller, it also controls active power P as it depends on V_0, since $P = V_0 I_0$, where I_0 is dc link current, Figure 2. Resistance R_{in} also controls power factor indirectly, since active power P, reactive power Q and apparent power S are related by the expression $S = \sqrt{P^2 + Q^2}$. In this sense, as S is fixed, if power P is set to a relatively high value (close to S), reactive power Q should be close to zero. So,

$$R_{in} = K_p(V_0^* - V_0) + K_I \int (V_0^* - V_0)dt \tag{21}$$

where V_0^* is dc link voltage reference, K_p, K_I is proportional and integrative PI constants, respectively. PI constants are positive $K_p > 0$, $K_I > 0$, to guarantee that $R_{in} > 0$, when $V_0^* > V_0$. R_{in} controller, named here emulated resistance control, leads to a resistive impedance seen from the grid. Moreover, in frequency domain, R_{in} controller can be expressed as a function of dc-link voltage error $(V_0^* - V_0)$ as,

$$R_{in} = (V_0^* - V_0)(K_{p1} + \frac{K_{I1}}{s}) \tag{22}$$

According to equation (19), the average current multiplied by R_{in} is compared to variable amplitude carrier, $V_0 A_{tri}(t)$, where carrier $A_{tri}(t) = -(1 - d_g)$. This could be the essence of the OCC method when implemented by hardware since a variable carrier amplitude is characteristical of hardware-OCC [21], [38]. However, as the goal of the system is a software implementation, DSP characteristics must be included. In this order, it would be useful to modify classical software-OCC modulator, (19), as,

$$q_{gn} = \begin{cases} 1, & when\ i_{gs}.R_{in} \geq V_0.A_{tri}(t) \\ 0, & otherwise \end{cases} \tag{23}$$

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where q_{gn} is the logical state at the gate of lower switch of power converter shown in Figure 1(a). Yet, as dc-link voltage is positive, $V_0 > 0$, former relation can be modified as,

$$q_{gn} = \begin{cases} 1, & when \ \frac{(i_{gs}R_{in})}{V_0} \geq A_{tri}(t) \\ 0, & otherwise \end{cases} \tag{24}$$

Former and latter relations are equivalent, as they generate the same firing pulses. The later represents OCC variable-amplitude carrier, Figure 4(a), while the former is adequate for DSP manipulation, Figure 4(b), as will see later in section IV. Besides, it resembles a PWM modulator with zero-sequence injection producing Space Vector PWM, SVPWM [49], or phase-clamping [50], but without phase-current distortion.

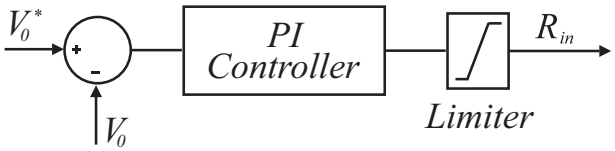

Figure 5. R_{in} controller and its maximum R_{in-max} and minimum R_{in-min} limits.

2. OCC STABILITY ANALYSIS

There is no simple method to analyze hardware-OCC stability by conventional control theory, as this technique is all except conventional, once control and hardware are integrated, while in software-OCC control and hardware are implemented and integrated by software. There are two main stability issues reported in hardware-OCC i.e., at no-load [21], [38], [30], and high-load [29]. However, control theory was not used to study them, but hardware analysis. This might be because OCC instability is provoked by over modulation [21] and hardware limitations [29] and not by poles or zeroes misplacement. Stability issues in hardware-OCC can be solved by using an emulated-resistance controller R_{in} of software-OCC [31], and it is max. and min. limiters, Figure 5. The next sub-section presents a model based on emulated-resistance control, which explains hardware-OCC instability and software-OCC solutions to the problem.

2.1. Hardware-OCC Theoretical Background.

In hardware-OCC, voltage V_m is a PI controller of dc voltage, given by [21],

$$V_m = (V_0^* - V_0)(K_{p1} + \frac{K_{I1}}{s}) \tag{25}$$

where V_m is carrier amplitude controller, Fig.5(a), in frequency domain, $s = j\omega$, V_m is defined by [21],

$$V_m = \frac{K_1 R_s V_0}{R_{in1}} \tag{26}$$

where K_1 is a parameter, $\frac{V_{Sg}}{V_0} < K_1 < 1 + \frac{V_{Sg}}{V_0}$, R_S is current sensor resistance ($R_S = 1\Omega$) and R_{in1} is emulated resistance, $R_{in1} > 0$, [21]. In addition, as in hardware-OCC firing pulses can be defined as [21], [43],

$$q_{gnh} = \begin{cases} 1, & when \ i_{gs} \geq V_m.A_{trih}(t) \\ 0, & otherwise \end{cases} \tag{27}$$

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where q_{gnh} is the logical state at the gate of lower switch of power converter, Figure 1(a), A_{trih} is fixed carrier amplitude. The former equation represents hardware-OCC modulator since modulating wave is compared to a variable-amplitude carrier, controlled by $V_m > 0$, (25). Note that this carrier leads to a multiplication operation, despite OCC arithmetic simplicity. Besides, as for a PWM rectifier, Figure 2, average dc voltage V_0 has a voltage ripple V_{0r} related to its peak value V_{0p} [51], see Figure 5, then $V_0 = V_{0p} + V_{0r}$. Hence,

$$V_0 = V_{0p} + \frac{I_0}{8C} T_{SW} \tag{28}$$

where $V_{0r} = \frac{-I_0}{8C}$, I_0 is dc-link current, R_L is dc-link load, $I_0 = \frac{V_0}{R_L}$, C is dc-link equivalent capacitor, $C = \frac{C_1 C_2}{(C_1+C_2)}$, T_{SW} is switching time period, $T_{SW} = 2T_0$, T_0 is time period between peaks of voltage ripple. Although dc-link capacitor C is assumed so large that voltage ripple is neglected and hence average and peak dc-link values are the same, $V_0 \approx V_{0p}$, [51]. Yet, for practical values of capacitance, only (28) is valid.

2.2. Hardware-OCC Issues

When this technique appeared at first offering a cost-effective and straightforward solution [21], [30], it arises two questions about what kind of simplicity and a solution to what. Answer to the later was hardware, control, and arithmetic simplicity [30]. Hardware and control simplicity was almost achieved, section I, but a lack of PLL synchronization could cause PF derating

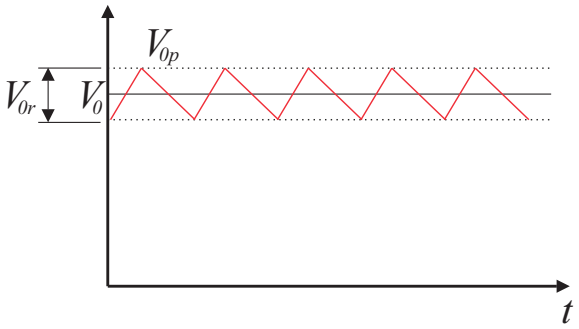

Figure 6. DC-link voltage in a PWM rectifier

due to a lack of grid synchronization mechanism, whatever a PLL or any other, and OCC had no one. Besides, arithmetic simplicity, i.e., arithmetic without multiplication and division, is most difficult to achieve. However, to avoid the later, the emblematic OCC variable-carrier was created, (27), but at the cost of instability at no-load [21]. As a result, through instability and PF derating, the offered OCC solution simplicity became no more than a nice try. Including the solution cost-effectiveness of the OCC. Above all, although the answer to the former question was power converters [43], [29], [1], [23], [28], [32], [27], it is still open, as it generates another question, (what if the OCC simplicity were true, what additional problems could solve).

1) Stability at no-load: In general, in a PWM rectifier, output power P_0 equals input power P_T minus power losses, P_L, $P_0 = P_T - P_L$. Then, admitting a proportionality between power losses and input power,

$$P_0 = K_3 P_T \tag{29}$$

where K_3 is proportional constant. In addition, assuming UPF, input power is given by,

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$$P_T = 3V_{Sg}I_g \tag{30}$$

where V_{Sg} and I_g denotes grid voltage and phase current in frequency domain, respectively, while output power is,

$$P_0 = V_0 I_0 \tag{31}$$

Then, combining (29), (30) and (31), it yields,

$$I_g = K_4 I_0 \tag{32}$$

where $K_4 = \frac{V_0}{(3K_3V_{Sg})}$, I_0 is dc current. The former equation says that phase-current I_g is proportional to I_0. Yet, (32) has practical limits given by the sensitivity of the technique. As a small phase-current could exist when I_0 is null, or lower than a threshold value, I_{0th}, causing phase-current distortion when Ig is greater than amplitude Vm, as reported in [21], [43], [38], [28], [39], [30], [42], [26]. This is since V_m becomes tiny at no-load when V_0 tends to its reference V_0^*, (25), which occurs when $V_0^* = V_{0p}$ and $I_0 = 0$, (28). To explain this phenomenon from an emulated-resistance approach, (26) can be rewritten as,

$$R_{in1} = \frac{K_1 V_0}{V_m} \tag{33}$$

Which leads to a virtual input resistance R_{in1}, as a sort of V_0 controller. Besides, as in OCC, phase-current varies according to [**?**],

$$R_{in1} = \frac{V_{Sg}}{R_e + sL} \tag{34}$$

where R_e denotes OCC input resistance in frequency domain. Hence, by making $R_e = R_{in1}$ and combining (25), (33) and (34),

$$m_a = \frac{I_g}{V_m} = \frac{V_{Sg}}{K_1 V_0 + L(V_0^* - V_0)(sK_{P1} + K_{I1})} \tag{35}$$

The equation (35) denotes modulation index m_a, as I_g is modulating and V_m is carrier amplitude [21]. Applying final value theorem to (35), for a unit step response $(\frac{1}{s})$ when $t \to +\infty$,

$$m_a = lim_{S\to 0} \frac{1}{S} S \frac{I_g}{V_m} \frac{V_{Sg}}{K_1 V_0 + LK_I(V_0^* - V_0)} \tag{36}$$

When $V_0^* = V_{0p}$ and $I_0 = 0$, $V_0^* = V_0$, (28), so equation (36) yields,

$$m_a = \frac{V_{Sg}}{K_1 V_0} \tag{37}$$

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Overmodulation ocurrs when $m_a > 1$, (37), as $\frac{V_p}{V_0} > K_1 > 0$, once $V_{Sg} = V_p cos\omega t$, (3), $m_a > 0$, i.e. $K_1 = 0.25\frac{V_p}{V_0}$, $m_a = 4$, $V_p > 0$, $V_0 > 0$. Above all, (37) can explain why previous works did not suppress fully overmodulation by growing or falling I_g [43], [38], [28], [39], [42], [26], once K_1 cannot be controlled.[21]. Figure 7 illustrates this by ploting m_a vs. K_1, (37), for $0.67 > K_1 > 0.19$, $V_p = 155.56$V, $V_0 = 467$V, when I_g grows 20%(A) and when I_g falls 20% (C). Notice that when $K_1 \leq 0.25$, the method does not work, as $m_a > 1$.

2) Hardware-OCC PF derating at high-load: As was mentioned earlier, PF derating occurs [29], through a lack of grid synchronization. However, this cannot be predicted by an open-loop resistance-emulator value, i.e., r_e [12], [21] as in frequency domain it leads to $R_e = \frac{r_e}{s}$, which combined to (34), it gives $I_g = s\frac{V_{Sg}}{(r_e+s^2L)}$, leading to an admittance angle $\phi_v = arctan(\frac{I_g}{V_{Sg}}) = \frac{\pi}{2}$, which is not true. However, a better prediction can be obtained by combining (25) and (35),

$$\frac{I_g}{V_{Sg}} = \frac{(V_0^* - V_0)(sK_{P1} + K_{I1})}{[sK_{P1}L(V_0^* - V_0) + K_{I1}L(V_0^* - V_0) + K_1V_0]s} \tag{38}$$

Then, combining former equation and (28), ϕ_v is given by,

$$\phi_v = \phi_1 - arctan[\frac{\omega LK_{P1}(8C(V_0^* - V_{0p}) + I_0T_{SW})}{LK_{I1}(8C(V_0^* - V_{0p}) + I_0T_{SW}) + K_1(8CV_{0p} + I_0T_{SW})}] \tag{39}$$

$$\frac{\partial\phi}{\partial I_0} = \frac{8\omega LCT_{SW}K_{P1}K_1V_0^*}{(LK_{I1}I_0T_{SW} + K_1(8CV_{0p} - I_0T_{SW}))^2 + (\omega LK_{P1}I_0T_{SW})^2} \tag{40}$$

where $V_{0p} = V_0^*$ was assumed for simplicity. It can be noticed that the former equation predicts PF derating because admittance angle ϕ_v is a decreasing function, confirming previous works [39], [30], [42], [26]. Figure 8 plots equation (39), for $V_p = 155.56$V, $V_{0p} = V_0^* = 467$V, $K_1 = 1$. $K_{p1} = 1$, $K_{I1} = 1$. This figure confirms that ϕ_v is decreasing when I_0 increases, i.e. from $I_0 = 10$A (P) to $I_0 = 20$A (N) and $I_0 = 30$A (M).

2.3. Software-OCC Solutions

Although subtle, the main difference between hardware-OCC and software-OCC is voltage controller location, which in the later is named V_m and controls carrier, (25), (27), while in the former is named R_{in} and controls modulating, (22), (24). However, only R_{in} allows OCC to solve instability and PF derating issues. It is not just a matter of implementation, 1) Stability at no-load: As was mentioned earlier, phase-current is proportional to dc current, (32), but only under practical limits, through the sensitivity of OCC modulator. Since a small distorted phase-current could appear when dc current is less than the threshold current, I_{0th}. In order to avoid this in software-OCC, maximum controller limiter R_{in-max} could be calibrated to set up minimum phase-current I_{gmin}, since $I_g = \frac{V_{Sg}}{R_{in}}$, (20). Then, as voltage V_{Sg} is fixed, minimum phase-current I_{gmin} occurs when the resistance R_{inmax} is reached, as $I_gR_{in} = V_{Sg}$ is a hyperbolic curve working at first quadrant, $I_g > 0$, $R_{in} > 0$. That is,

$$I_{gmin} = \frac{V_{Sg}}{R_{inmax}} \tag{41}$$

Thereby, to avoid phase-current distortion at no-load, R_{inmax} must be set up to achieve a minimum phase-current I_{gmin} when dc current is less than I_{0th} . Thus,

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$$I_g = \begin{cases} I_{gmin}, & when\ I_0 < I_{0th} \\ K_4 I_0, & when\ I_0 \geq I_{0th} \end{cases} \quad (42)$$

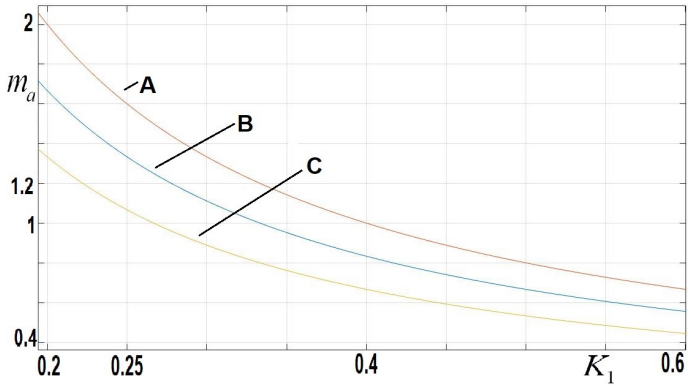

Figure 7. Hardware-OCC. (a) ma vs. K_1, (37), A: I_g grows 20% B: Without correction. C: I_g falls 20%

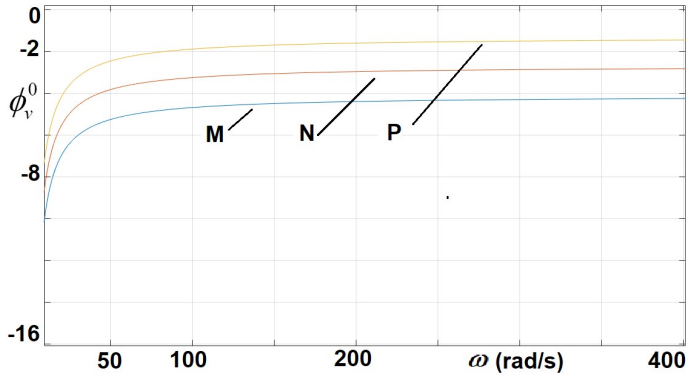

Figure 8. Hardware-OCC. (b) Angle ϕ_v (10/div) vs. angular frequency (rad/s) as a function of dc current I_0, $V_0^* = V_{0p} = 467V$, $T_{sw} = 8.33$ms, $C = 1000\mu F$, L=1mH, $K_{p1} = K_{I1} = K_I = 1$.

Figure 9 shows a plot of I_g vs. I_0, (32), when $I_{gmin} = 1.4$A, $I_{0th} = 0.5$A, $V_{Sg} = 110$V, $R_{inmax} = 78.01\Omega$. Unlike hardware-OCC, a tiny dc-controller value does not provoke overmodulation, so the current distortion becomes simpler to avoid.

2) Software-OCC PF derating at high-load: As at no-load, there is no current distortion, it would be necessary to check if at no-load PF derating could be generated. In this sense, the no-load and high-load case must be analyzed for PF derating. Thus, substituting $R_e = R_{in}$ in (34),

$$I_g = \frac{V_{Sg}}{R_{in} + sL} \quad (43)$$

Note in the former equation that if denominator left term is very greater than the right one, $R_{in} >> sL$, the equation becomes equivalent to (20). However, to achieve UPF, another expression can be found by combining equations (22) and (45), and relation $R_{in} >> sL$,

$$I_g = \frac{V_{Sg}}{(V_0^* - V_0)(K_P + \frac{K_I}{s})} \quad (44)$$

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Relation $R_{in} >> sL$ can be forced by setting resistance lower limit $R_{inmin} = 10\omega L$, Figure 5, since in practice this relation implies $R_{in} \geq 10\omega L$ $R_{in} \geq 10\omega L$. Besides, from expression (44), admittance angle $\phi = arctan(\frac{I_g}{V_{Sg}}$is given by,

$$\phi_v = \frac{\pi}{2} - arctan(\frac{\omega K_P}{K_I}) \tag{45}$$

It can be noticed that this angle does not depend on dc current, nor dc voltage. Figure 10 shows a plot of admittance angle $\phi_v$vs.ω, for software-OCC, (45), when $K_P = 1$, $K_I = 1$. This plot independs on dc current.

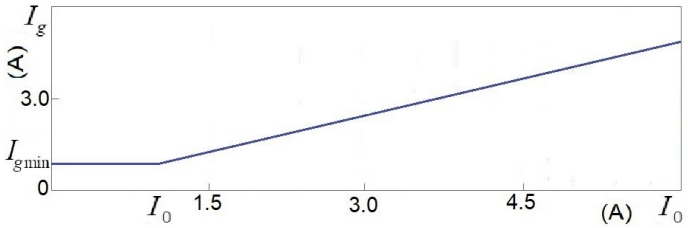

Figure 9. Software-OCC. (a) I_g vs. I_0, (34), with a minimum value, $I_{gmin} = 1$, $V_{Sg} = 110V$, $V_0^* = 467$V.

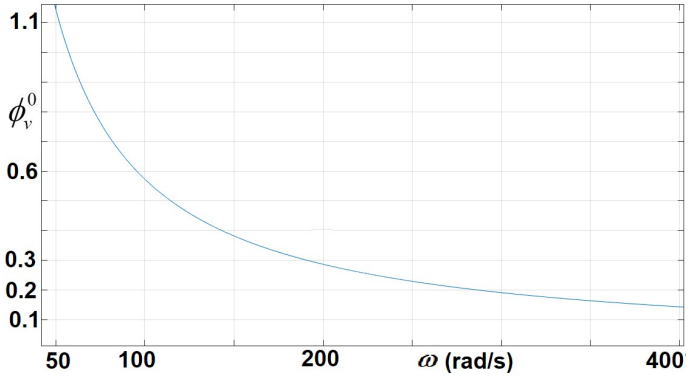

Figure 10. Software-OCC. (b) Angle $\phi_v(0.10/\text{div})$ vs. angular frequency (rad/s) as a function of dc current I_0, $V_0^* = V_{0p} = 467V$, $T_{SW} = 8.33$ms, $C = 1000\mu F$, L=1mH, $K_{p1} = K_{I1} = K_I = 1$.

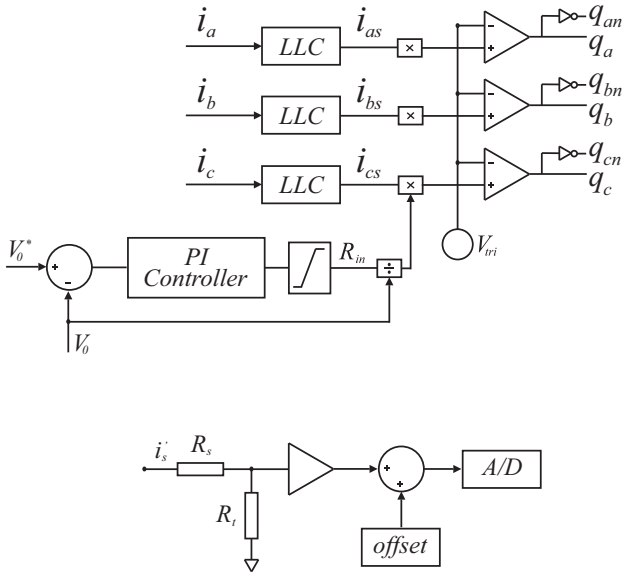

Figure 11. (a) Software-OCC. (b) Phase-current conditioner

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3. DSP IMPLEMENTATION

Software-OCC controller, Figure 11(a), employs embedded DSP devices like PWM modulators, analog to digital, A/D, converters and the arithmetic-logic unit, ALU, blocks to perform all its tasks digitally, i.e., arithmetic and logic operations (including multiplication and division), digital comparators, digital inverters, PI controllers, output limiters and lead-lag compensators, LLCs. Yet, it is necessary a phase-current conditioner, Figure 11(b), consisting of a Hall-effect current-sensor [52], some operational amplifiers, OP-AMPs, and a few resistors [53] to change phase-current over dc voltage and then transforms it into digital, through A/D converter, see Appendix A. Hence, it is used a Hall-effect resistor R_S (100Ω) to convert current into voltage and a resistor R_t (1$K\Omega$) to attenuate it. Then, a bunch of resistors and OP-AMPs (Att) amplifies this voltage and adds an offset to it to input it to A/D, as in DSP, A/D converter only works with positive voltages [53]. Hence, a proportionality between analog and digital is guaranteed for DSP to perform OCC control operations, once a scale factor K_S (bits /A) is maintained for all currents. For hardware-OCC, something similar occurs, but now the scale factor is a resistance R_S (V/A), since a current-sensor resistor is generally used in hardware systems. Anyway, for the sake of simplicity, to establish an equivalency between hardware and software-OCC, it is defined in the later, resistor R_S as unity, $R_S = 1\Omega$, denoting that phase-current corresponds to the digital value adopted in DSP control operations. After the digitalizing process, phase-current pass through software implemented LLC, which averages phase-current according to,

$$F(s) = G_0 \frac{(1 + s\tau_1)}{(1 + s\tau_2)} \tag{46}$$

where $F(s) = \frac{I_{gs}(s)}{I_g(s)}$, $I_{gs}(s)$, $I_g(s)$ in frequency domain corresponds to phase and average currents i_g and i_{gs}, respectively in time domain; G_0 is gain, τ_1 , τ_2 are lead and lag compensator constants. The main idea of former equation is to average phase-current i_g without unwanted delay on phase angle, manipulating τ_1 and τ_2 values. A further analysis of LLC on software-OCC is performed in [34]. On the other hand, for DSP, carrier waveshape (a sawtooth or a symmetrical triangle) is a choice of DSP-PWM modulator. Thus, in software-OCC, a triangle carrier is chosen since, for a sinusoidal modulating wave, it produces less current harmonics than those in a sawtooth carrier [54]. Another DSP choice is produced when carrier slope (rising or falling) intercepts current, generating an inherent delay related to the inverse of the carrier frequency. This does not jeopardize the time control algorithm, as DSP operations are performed between the interceptions. Yet, in software-OCC, a variation in carrier amplitude also involves a variation in carrier frequency, Table.1 [53]. Then, there is no direct method to change carrier amplitude without vary carrier frequency also. However, in order to solve this issue, focusing on generating the same firing pulses, the OCC modulator equation (23) is modified as (24), which becomes the most suitable expression for DSP implementation as it considers a fixed carrier amplitude. In fact, the software-OCC controller is based on equations (21), (24), Figure 11(a).

Table 1. CARRIER AMPLITUDE AND FREQUENCY FOR DSP TMS3020F335.

Carrier Amplitude (A)	f_C (kHz)
3750	20
5000	15
7500	10

3.1. COST-EFFECTIVENESS SOFTWARE-OCC DISCUSSION.

Although first work on hardware-OCC rectifier might constitute a cost-effective solution [21], it presented such serious stability problems, that its use was not practical, i.e., for APF [55], or for photovoltaics applications [32]. Later instability solutions performed by hardware at no-load were reported, but there was always current distortion when dc current falls below a certain level

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[43], [38], [28], [39], [42], [26], except when a bulky resistor was placed at dc-link [21], [30]. And at high-load where complicated circuits [43], [23], [28], [42], [25], or costly systems were used [29], [41]. Thereby, despite these works represent a nice try to solve specific problems, they do not provide a definitive solution, even sacrificing hardware simplicity, or cost-effectiveness of OCC [21], [30]. Furthermore, any of the abovementioned reported works were capable of operating both at no-load and at high-load. Thus, to compare the fair cost-effectiveness of existing hardware-OCC works with present software-OCC, it would be necessary to compare reported works of the same performance, that is, OCC rectifiers operating at a wide range of load. Otherwise, it is like comparing a calculator with a computer. Above all, although the present work was implemented by using a TMS 320F28335 evaluation board in a laboratory prototype, a pretty cost-effective solution could be found acquiring a DSP chip and its accessories separately, or by using a simpler DSP, or a microcontroller chip, i.e., a PIC. In any case, the present proposal results in a cost-effective solution on a full range of load, at least, for lack of another option.

4. SIMULATION AND EXPERIMENTAL RESULTS

The performance of software-OCC has been verified by simulation by using MATLAB and PSCAD/EMTDC and by experimental using DSP TMS320F28335, for PWM rectifier shown in Figure 12. The simulation was presented in Figures 14, 15 and 16 (PSCAD) and in Figure 8 and Figure 10 (MATLAB). Experimentals are in Figures 18-Figure 28. Parameter values are in Table. 2. In Figure 17 and Figure 24, Vgrms =110V and $V_0^* = 390$V, but in Figure18- Figure 23, due to technical problems, Vgrms =21V and $V_0^* = 100$V. Figure 14 presents a simulation result only with hardware-OCC evidencing its instability, while Figure 17 presents a simulation result on stability at no-load and high-load conditions for software-OCC. It can be observed that at no-load, it does not present hardware–OCC stability issues,

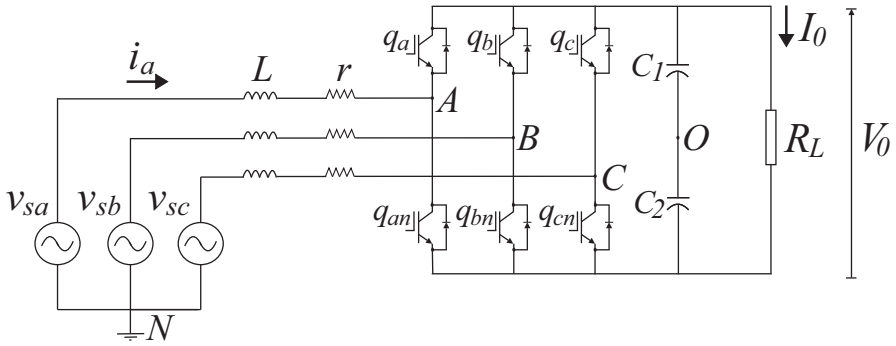

Figure 12. (a) PWM rectifier used in tests.

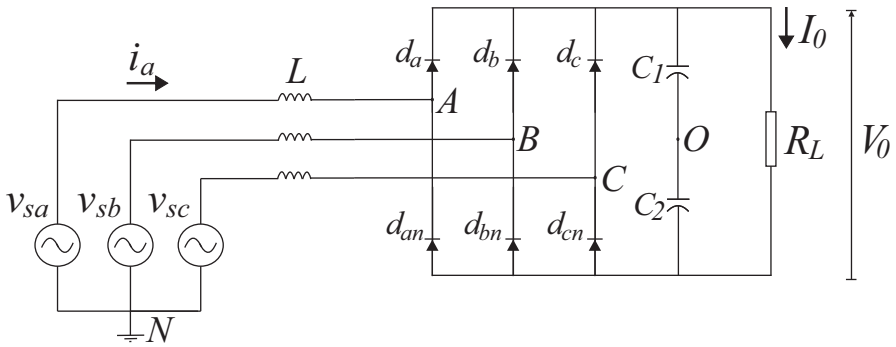

Figure 13. (b) PWM rectifier before start-up.

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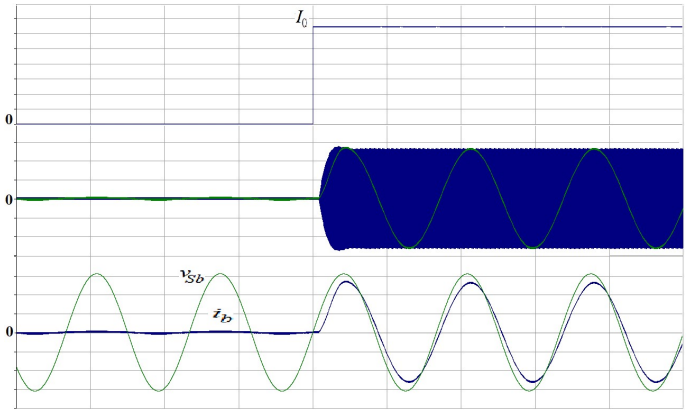

Figure 14. Hardware-OCC. (a) Overmodulation at no-load. Transitory from no-load to high-load (10ms/div). Upper: DC current I_0 (5A/div). Middle: Carrier and average current (2V/div). Down: Grid voltage (50V/div) and phase current x 10 (50A/div).

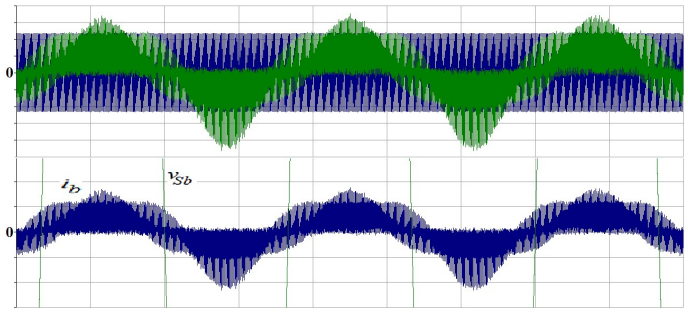

Figure 15. Overmodulation at no-load (5ms/div). Detailed view. Upper: Carrier and average current (0.05V/div). Down: Grid voltage (2.5V/div) and phase current x 10 (2.5A/div).

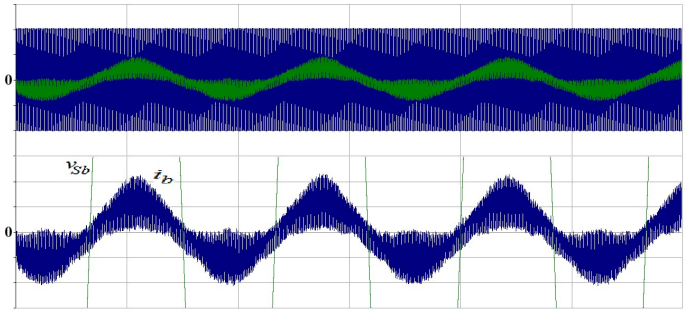

Figure 16. No overmodulation (5ms/div). Detailed view. Upper: Carrier and average current (0.05V/div). Down: Grid voltage (2.5V/div) and phase current x 10 (2.5A/div).

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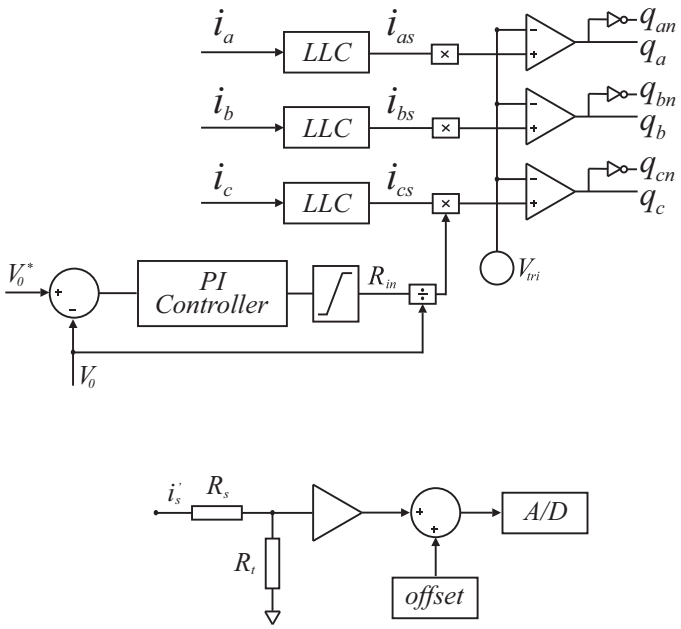

Figure 17. Software-OCC. Transitory from no-load to high-load (10 ms/div). Upper: DC current I_0 (5A/div). Middle: Carrier and average current (0.1u/div). Down: Grid voltage (50V/div) and phase currents x 10 (50A/div).

like overmodulation [21] (current distortion), nor present PF derating. This result verify equation (43) when $K_{P1} >> K_{I1}$. Experimental results in Figure 18-Figure 28 are dedicated to confirm former result, or enhance it. Figure 17 shows software-OCC behavior at start-up at no-load, verifying that there is no current distortion, unlike [21], nor even in smaller amount [38], [39], [26]. This is because to avoid current distortion, software-OCC can define minimum current when load current is null, by using R_{in-max}, (45). Figure 18 illustrates dc-link voltage response to a current step, from no-load to high-load, showing a relatively fast-software-OCC dynamic-response considering dc-link capacitors size, thus complementing Figures 14, 15 and Figure 16. Figure 19 shows phase-current and R_{in} controller response to a current step from no-load to high-load, presenting a high dynamic response, which is according to Figure 17.

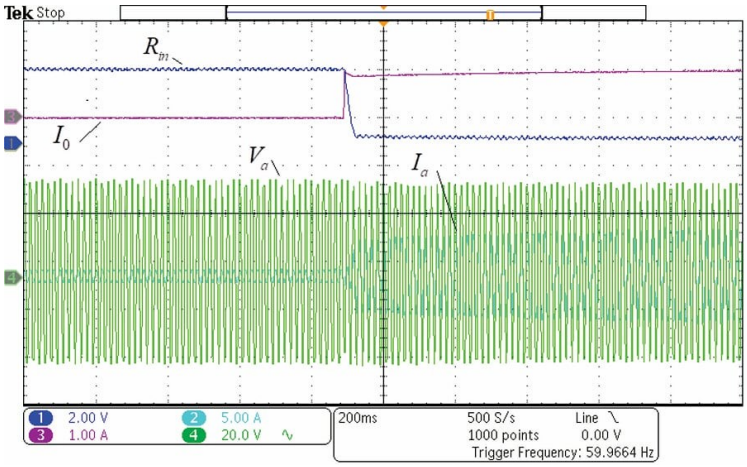

Figure 18. R_{in} controller ($x5\Omega/V$) (2V/div), dc-link current (1A/div), grid voltage (20V/div). and phase current (5A/div) for PWM rectifier transient from no -load to high -load. Hor. 40 ms/div.

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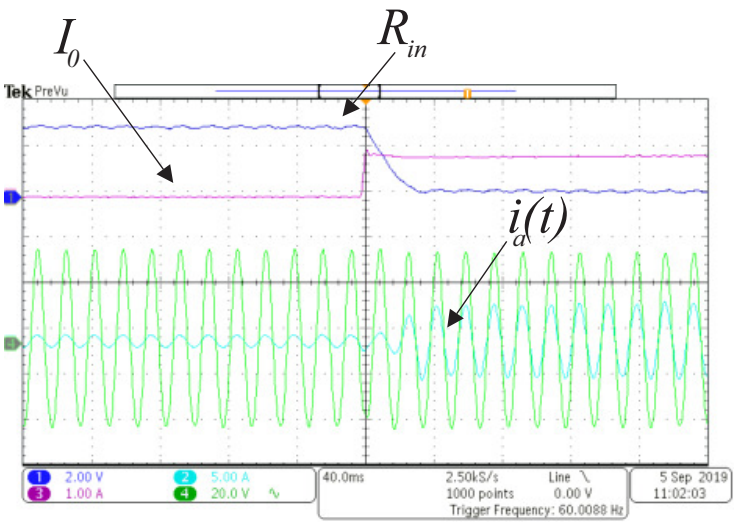

Figure 19. R_{in} controller ($x5\Omega/V$) (2V/div), dc-link current (1A/div), grid voltage (20V/div). and phase current (5A/div) for PWM rectifier transient from no -load to high -load. Hor. 40 ms/div.

Figure 20 is a Figure 19 amplification for current-shape better illustration. It can be noticed in the former figure, that at no-load, when $I_0 = 0$, phase-current is small, but it does not exhibit current distortion, as it could be expected considering power balancing in equation (41), but instead, regarding a minimum phase-current, according to equation (42), see Figure 19, Figure 20 and Figure 22. Also, it can be observed that there is no power factor derating, as occurs in conventional hardware-OCC [21], see Figure 21, and Figure 23, and to preserve power factor, it is not necessary to use bulky inductors, unlike [29], [41], Table. 2. Thus, also confirming Figure 17.

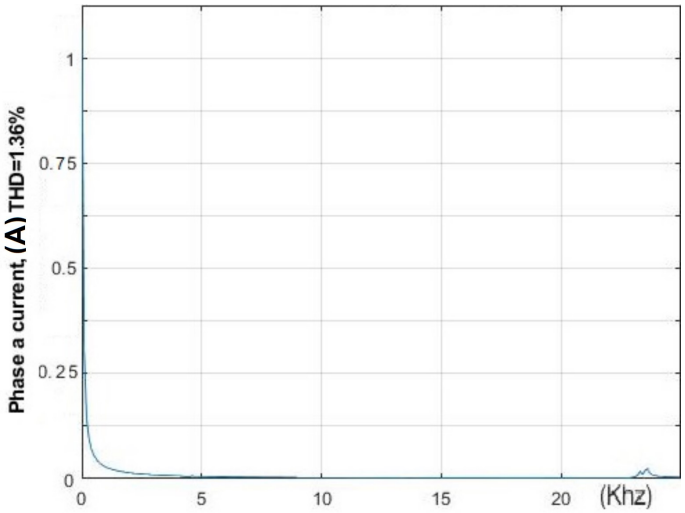

Figure 20. Harmonic spectrum. Phase a current, at no=load. $f_C = 24$kHz. THD=1.36%.

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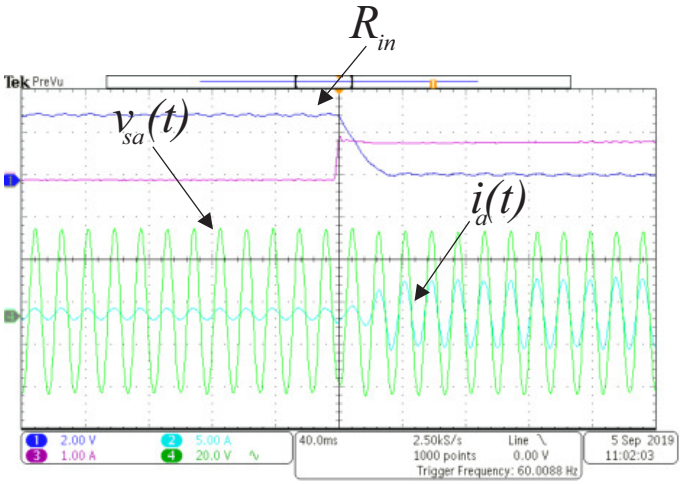

Figure 21. (20ms/div). Grid voltage (2V/div) and phase-current (1A/div) at high-load, $f_C = 24$ kHz. Phase a.

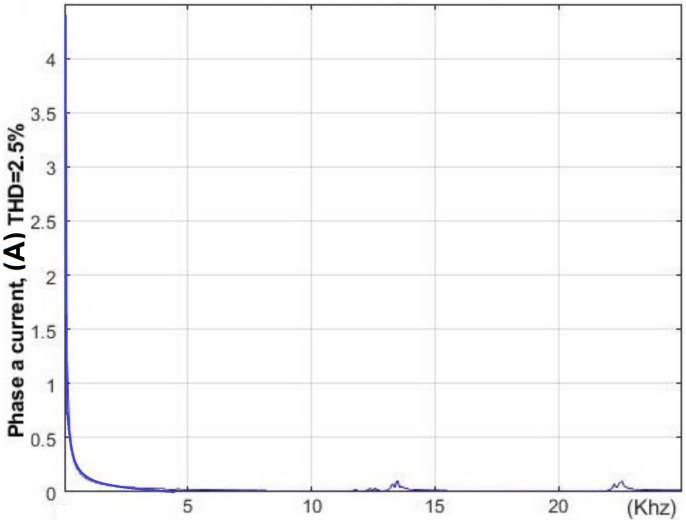

Figure 22. Harmonic spectrum. Phase a current, at high-load $f_C = 24$ kHz. THD=2.5%.

From Figure 20 and Figure 22, it can be deduced that the present proposal satisfies $IEEEStd519-1992$ [8], as current distortion is small. Figure 21 shows the proposed controller start-up when the load is high. It illustrates a high dynamic response of software-OCC at high-load and that in such conditions, there is no PF derating. This result could substitute Figure 19 and Figure 26 results, once these figures do not achieve high-load results. On the other hand, Figure 23 shows PF derating vs. phase current at different load conditions. Figure 23 was built from Figure 19 at no-load and Figure 21 at high-load. Figure 23 demonstrates that there is a tiny variation when phase currents change. Figure 24-Figure 26. illustrate dc-link voltage response to a current step, from high-load to no-load, showing a relatively fast software-OCC dynamic-response due to dc-link capacitors size, thus complementing Figure 17.

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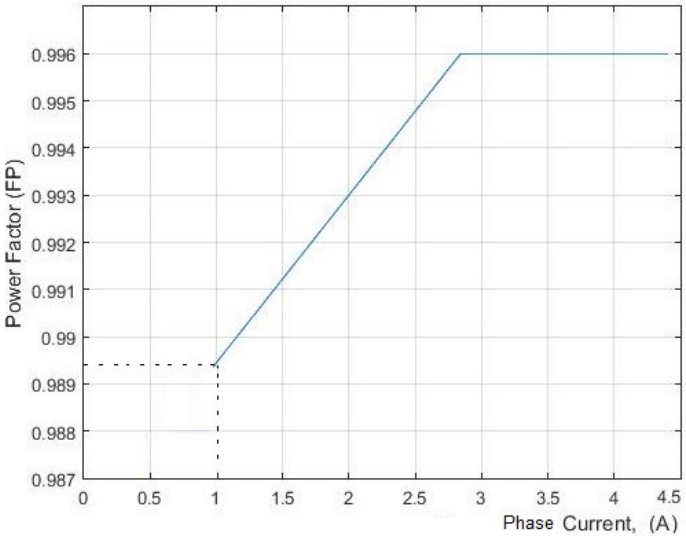

Figure 23. Power factor vs. phase current.

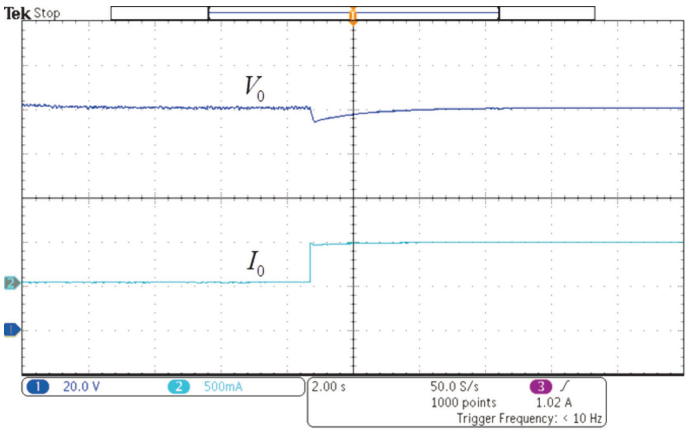

Figure 24. DC-link voltage V_0 (20V/div) and dc-link current I_0 (0.5A/div), for PWM rectifier transient from no-load to high-load. Vgrms =21V. Hor. 2 s/div.

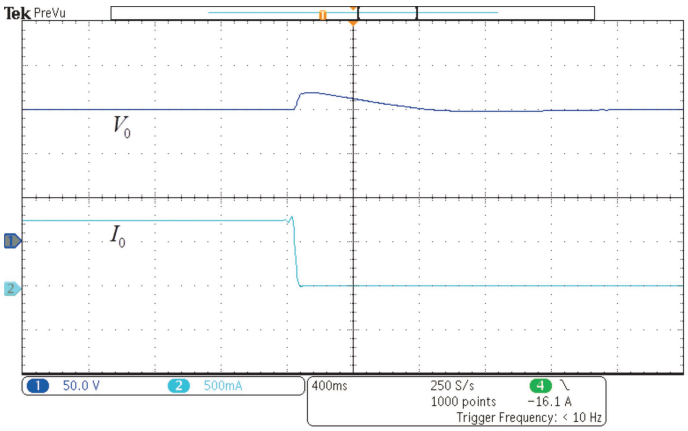

Figure 25. PWM rectifier transient from high-load to no-load. DC-link voltage (50V/div) and dc-link current (x4) (0.5A/div). Vgrms =21V. Hor. 0.4 s/div

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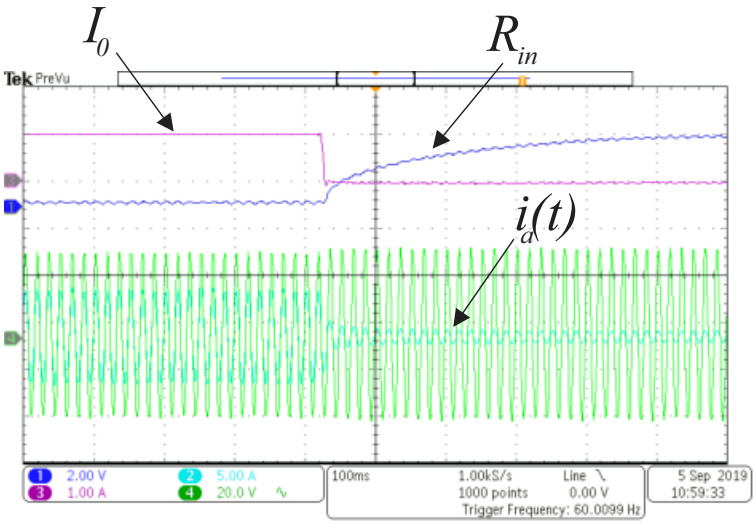

Figure 26. R_{in} controller ($x5\Omega/V$) (2V/div), dc-link current (1A/div), grid voltage(20V/div). and phase current (5A/div) for PWM rectifier transient from high-load to no-load. Hor. 40 ms/div.

Table 2. PARAMETERS ON SIMULATION AND EXPERIMENTALS.

Parameter	R (Ω)	ω(r/s)	L(mH)	$C_1(\mu F)$	$C_2(\mu F)$	V_{Sg} (V)	τ_1(ms)	τ_2(ms)	f_C(kHz)
Simulation	1	377	1	670	670	110	1	0.15	20
Experimental	1	377	1	2200	2200	110	1	0.15	25

Figure 27 illustrates the dynamic response of software PWM-OCC (switching frequency:24 kHz, R_L : 100Ω) as well as the charging capacitor of the dc-link voltage. It spends approximately 0.55s, which is consistent with C=1100μF, Table. 2, and R_L. Since the time constant $\tau = R_L C$ and charging capacitor should last 3τ approx. Although OCC systems use to have a high dynamic response, for dc-link capacitor charging, this response depends on the capacitor value that, in the present case, was not possible to change due to the physical stability of Semikron board and laboratory facilities setup, Figure 28.

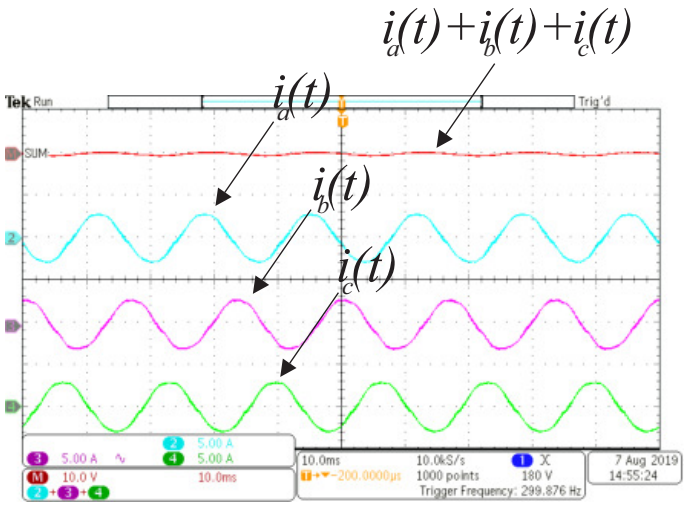

Figure 27. DC-link voltage V0 (300V/div) and phase currents i_a, i_b and i_c (14 A/div), $V_0^* = 390$V. Vgrms =110V. Hor: 100ms/div.

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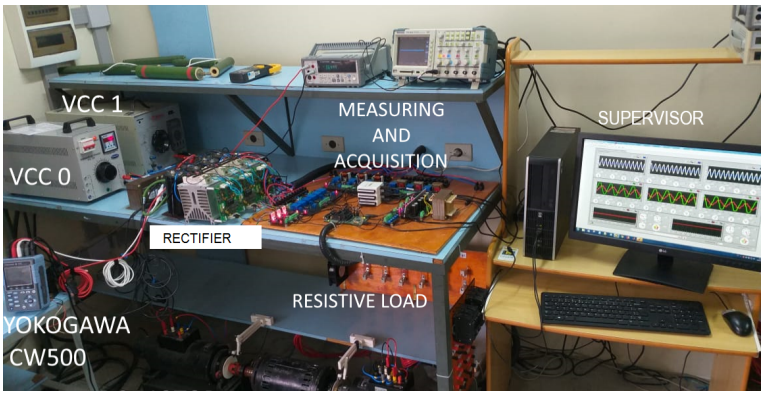

Figure 28. Experimental set-up

5. CONCLUSION

Despite the stability problems, the hardware-OCC contributions to power quality like hardware and control simplicity and high dynamic response are well known. Somehow, software-OCC raises as a solution to these problems and as a way to enhance and increase OCC contributions. According to the analysis performed in this work, the closed-loop emulated-resistance is, after all, with a dc-link voltage controller located in a different place than in hardware-OCC. It can manipulate active power and, at this moment, the power factor. Because of a DSP limitation, the DSP cannot emulate variable-carrier amplitude OCC in this software version, since carrier amplitude depends on the switching frequency. However, using a mathematical equivalency, gate pulses are fired in a similar way than that of hardware-OCC. This allows the resistance controller limiters to solve stability issues.

From the stability analysis of emulated-resistance controller for a PWM rectifier, it has stated that: Despite, several authors provide a solution to hardware-OCC instability at no-load, or at high-load separately. Any of these provide a full-load solution, i.e., at no-load and at high-load at the same time. Software-OCC does not present stability problems, even over a wide load range and presents a cost-effective solution, once DSP and its components were acquired separately, or a simpler DSP or a PIC was acquired. An easy way to improve stability and PF derating in hardware-OCC might be to emulate R_{in} controller by hardware, using analog multipliers, dividers, and limiters but sacrificing OCC simplicity and cost-effectiveness. The theoretical analysis is validated by simulation and experiments.

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Abbreviations

The following abbreviations are used in this manuscript:

DSP	Digital Signal Processor
OCC	One Cycle Control
CMV	Common-mode Voltage
LLC	lead-lag compensator
UPF	unity power factor
APF	active power filters
FACTs	flexible ac transmission systems
GCI	photo-voltaic grid-connected inverters.

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Sample Availability: Samples of the compounds ..... are available from the authors.