Digital Phase Plane for Analyzing Asymptotic Stability of Digital Systems

Qihong Ke
The University of Auckland, New Zealand

Qihongke1225@gmail.com

Abstract-Digital phase plane is presented in this paper. For constant input second order digital systems with arbitrary initial conditions for arbitrary quantizaters, this digital phase plane shows, in plot form, the state trajectory and the asymptotic stability, including the existence and the position of arbitrary period limit cycles.

1. Introduction

Many papers have been presented to discuss limit cycles (LC) due to finite word length in digital systems. Here, digital systems should be IIR filters or digital control systems. LC may cause the linear stable system unasymptotic stable. Now, the parameter regions in which the systems will be asymptotic stable have been presented Xu et al [3], Premaratne et al [5], Bose et al [7], Tran-Thong et al [11], and Lepschy et al [15]. Detailed discussions about the bounds of LCs can be found in Bauer et al [6], Munson et al [12], and Green et al [13]. While, nonzero input digital systems have not received widespread attention. Due to the nonlinearity of LCs, the asymptotic stability of a zero input digital system does not guarantee the asymptotic stability of the same system with nonzero input. Also the effects of initial condition on LCs have not been discussed. LCs still cannot be accurately calculated. As to these problems above, this paper introduces Digital Phase Plane, which shows, in plot form, the asymptotic stability of constant input second order digital systems, without need for calculation.

2. Digital Phase Plane

An n-order constant input digital system is described by

$$x(k) = -b_1 x(k-1) - \dots - b_n x(k-n) + a_0 u(k) + \dots + a_n u(k-m)$$
(1)

where x(k) is the state, u(k) = ... = u(k-m) = u is the constant input, and $b_1,...,b_n,a_0,...,a_m$ are the parameters of the system. Suppose one quantizater is applied, (1) can be implemented in the following way

$$Q[x(k)] = Q - b_1 x(k-1) - \dots - b_n x(k-n) + A(1)u = Q[p+\varepsilon] = p$$
(2)

where Q[] is the quantizater, $A(1) = \sum_{i=0}^{m} a_i$, and

$$p = Q[x(k)] \in (..., -2, -1, 0, 1, 2, ...)$$
(3)

$$\varepsilon_{-} \le \varepsilon = x(k) - Q[x(k)] \langle \varepsilon_{+}$$
 (4)

According to (2), provide $b_n \neq 0$, (1) can be written as,

$$x(k-n) = \left[-\frac{b_1}{b_n} x(k-1) - \dots - \frac{b_{n-1}}{b_n} x(k-n+1) \right] + \frac{A(1)}{b_n} u - \frac{p+\varepsilon}{b_n}$$
 (5)

From (3), (4), and (5), a digital phase space can be obtained to show the relations among the states of (2). For a second order digital system (SODS), this digital phase space is reduced to a plane named as Digital Phase Plane (DPP). Following is the procedure to produce DPP. In (2), let n = 2, the SODS is obtained as

$$Q[x(k)] = Q - b_1 x(k-1) - b_2 x(k-2) + A(1)u = Q[p+\varepsilon] = p.$$
(6)

If let $b_1 = -0.2$, $b_2 = -0.3$, A(1) = 1, then, (6) becomes

$$Q[x(k)] = Q[0.2x(k-1) + 0.3x(k-2) + u] = Q[p + \varepsilon] = p$$
(7)

and (5) becomes

$$x_2 = -\frac{-0.2}{-0.3}x_1 + \frac{u}{-0.3} - \frac{p+\varepsilon}{-0.3} = -0.6x_1 + 3.3(p+\varepsilon) - 3.3u$$
 (8)

where
$$x_1 = x(k-1), x_2 = x(k-2)$$
 (9)

$$\varepsilon_{-} = 0, \ \varepsilon_{+} = 1.$$
 (10)

 p_i indicates p = i. For instance, p_3 means p = 3. As two values of ε as in (10) are taken for each p_i , (8) produces a pair of equations. They describe the relations among x_1 , x_2 and u corresponding to this p_i . Since u is constant input, this pair of equations represents two lines in $x_2 - x_1$ plane. They are,

Lower bound line(LBL) of
$$p_i$$
, for $\varepsilon_- = 0$: $x_2 = -0.6x_1 + 3.3p_i - 3.3u$
Upper bound line(UBL) of p_i , for $\varepsilon_+ = 1$: $x_2 = -0.6x_1 + 3.3p_i + 3.3(1-u)$.

As p_i takes through all the values in (3), a group of such lines are produced. If the lines are drawn in $x_1 - x_2$ plane, it is the DPP for (7), as shown in Figure 1.

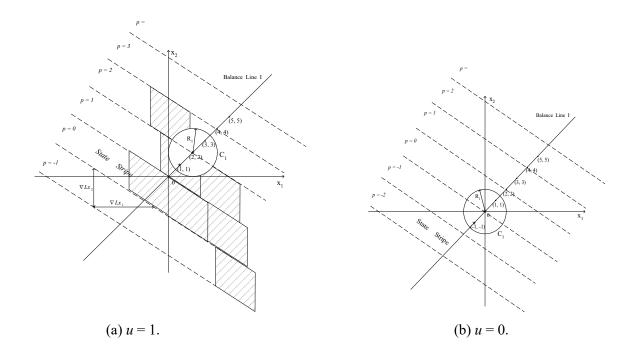


Figure 1. DPP for (7).

In Figure 1, some definitions are,

1) The area between the LBL of p_i and the UBL of p_i , and because of (4), including the LBL of p_i is known as State Stripe p_i . It is obviously

$$p_i = Q - b_1 x_1 - b_2 x_2 + A(1)u], \qquad \forall (x_1, x_2) \in State \ Stripe \ p_i.$$
 (12)

Here, (12) is true not only for (7), but also for (6).

2) p_i is State Stripe p_i value.

3)
$$x_2 = x_1$$
 (13)

is known as Balance Line I.

4) The Balance Line I value is defined as

$$x_{v} = \begin{cases} x_{1} & |x_{1}| \ge |x_{2}| \\ x_{2} & |x_{1}| < |x_{2}|. \end{cases}$$
 (14)

5) An integer point IP = (x_1, x_2) means that both x_1 and x_2 are integers.

In DPP, the states of (6) will go with following relation.

Corollary 1: If (x_1, x_2) is a point on the state trajectory of (6), then

$$(x_1(k+1), x_2(k+1)) = (p_i, x_1(k)), \quad \forall (x_1(k), x_2(k)) \in State \ Stripe \ p_i$$
 (15)

3. Limit Cycles in Digital Phase Plane

If a period I LC happens in (2), its steady state will be

$$x(k+I) = x(k), I \ge I. (16)$$

(16) means any steady state in stable digital systems is a LC. Now some results about LC are reached.

Corollary 2: In DPP, a period I LC existing in (6) is represented by I integer points which construct a close trajectory.

A stable (6) exists J steady states, or according to (16), exists J LCs, $J \ge I$. Provide the j^{th} steady state is a period I_j LC. Then, according to Corollary 2, in DPP, it is represented as

$$j^{th} LC = \{(x_{11j}, x_{21j}), \dots, (x_{1I_{jj}}, x_{2I_{jj}})\},$$
 $1 \le j \le J.$ (17)

Theorem 1: In DPP, an integer point IP = (x_1, x_2) represents a period 1 LC existing in (6), if and only if

$$x_1 = x_2 = p_i,$$
 $(x_1, x_2) \in State\ Stripe\ p_i.$ (18)

Theorem 2: In DPP, two integer points IP1 = (x_1, x_2) and IP2 = (x_2, x_1) represent a period 2 LC existing in (6), if and only if

$$IP1 = (x_1, x_2) \in State \ Stripe \ p_i, \ p_i = x_2, \ and$$

$$IP2 = (x_2, x_1) \in State \ Stripe \ p_j, \ p_j = x_1, \ x_1 \neq x_2$$
(19)

Based on (18), the IP representing a period 1 LC is always on Balance Line I. In (19), IP1 and IP2 symmetrize to Balance Line I; when $x_1 = x_2$, Theorem 2 becomes Theorem 1.

4. Stability and Initial Condition Effects in Digital Phase Plane

Provide Balance Line II: $x_2 = -x_1$, Balance Line III: $x_1 = 0$. They are shown in Figure 2. The Balance Line II value and the Balance Line III value are also defined by (14). Following are the conclusions about the stability of (6) in DPP.

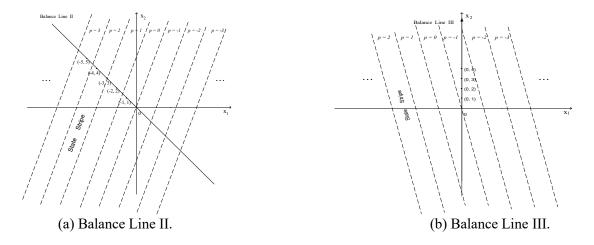


Figure 2. Balance Lines for (6).

Theorem 3: For the system $Q[x(k)] = Q[-b_1x(k-1) - b_2x(k-2) + A(1)u]$, if $\infty > \xi \ge 0$ exists, and all of the following S_l inequalities in DPP

$$|x_{v}| > |p_{il}| \Big|_{i=1\cdots S_{l}}, \qquad \forall x_{v} \in \{x_{v} : |x_{v}| = |Balance\ Line\ \chi_{il}\ value| \ge \xi\}$$

is true, the system is linear stable.

Theorem 4: For the system $Q[x(k)] = Q - b_1 x(k-1) - b_2 x(k-2) + A(1)u$, if $\infty > \xi \ge 0$ exists, and any of the following S_l inequalities in DPP

$$|x_{v}| < |p_{il}| \Big|_{i=1\cdots S_{v}}, \qquad \forall x_{v} \in \{x_{v} : |x_{v}| = |Balance\ Line\ \chi_{il}\ value| \ge \xi\}$$

is true, the system is unstable.

In the above two theorems, $(b_1, b_2) \in parameter area l, 1 \le l \le 5$; x_v is as in (14);

 $p_{il} = Q[-b_1x_1 - b_2x_2 + A(1)u]; (x_1, x_2) \in Balance Line \chi_{il};$ and

in parameter area 1: $\{b_1 > 1, b_2 \ge 0\}$, $S_1 = 2, \chi_{11} = II, \chi_{21} = III$

in parameter area 2: $\{1 \ge b_1 \ge -1, b_2 \ge 0\}$, $S_2 = 1, \chi_{12} = III$

in parameter area 3: $\{b_1 \langle -1, b_2 \geq 0\}, S_3 = 2, \chi_{13} = I, \chi_{23} = III$

in parameter area 4: $\{b_1 \le 0, b_2 < 0\}$, $S_4 = 1, \chi_{14} = I$

in parameter area 5: $\{b_1 > 0, b_2 < 0\}$, $S_5 = 1, \chi_{15} = II$.

Based on above discussion, the stability and LC in (6) are determined by the geometry structure of DPP which can be adjusted by $\nabla Lx_1 = -1/b_1$, $\nabla Lx_2 = -1/b_2$, as defined in (a) of Figure 1. The effects of initial condition will be explained in followings.

Corollary 3: If (6) is stable, the entire DPP can be divided into J parts which cover the entire DPP, and are not overlapped. J comes from (17).

Corollary 4: Provide the entire DPP has been divided into J parts, then, a stable (6) with initial condition which locates in the j^{th} part will converge to the j^{th} steady state or the j^{th} LC. In DPP, it means from (17),

$$(x_1(k), x_2(k))|_{k\to\infty} \to j^{th} LC = \{(x_{11j}, x_{21j}), \dots, (x_{1I_jj}, x_{2I_jj})\}, (x_1(0), x_2(0)) \in j^{th} part$$

here $1 \le j \le J$.

5. Further Discussions in Digital Phase Plane

Detailed investigations reveal following facts

- F1. The system $x(k) = Q b_1 x(k-1) b_2 x(k-2) + A(1)u$ is asymptotic stable, if and only if: 1). the system is linear stable and, 2).the system exists sole steady state which is a period 1 LC.
- F2. Both the magnitude of the constant input and the quantizater applied will affect LCs, or the asymptotic stability of digital systems;

- F3. J in (17) is determined by the parameters of system, quantizater applied, and the constant input;
- F4. in DPP, all LCs locate in circles. That is, from (17)

$$j^{th} LC = \{(x_{11j}, x_{21j}), \dots, (x_{1I_{ij}}, x_{2I_{ij}})\} \in C_{I_i} : (\rho = (x_0, x_0), R_{I_i})$$
 (20)

where $J \ge j \ge I$; C_{I_j} is known as balance circle; ρ is the center of C_{I_j} , and is on Balance Line I. x_0 is around the asymptotic stable state of (6). $R_{I_j} = k/B(I_j)$ is the radius of C_{I_j} . $B(I_j)$ is named as balance function.

6. Conclusion

DPP gives, in plot form, solutions to the asymptotic stability of (6). Based on (15) and Corollary 2, all LCs can be found in the circles of (20). Theorem 1 and Theorem 2 in this paper could be applied to nonlinear systems. It also should be possible to apply this technique to three or higher order digital systems.

7. References

- 1. Kar, H. and Singh, V., Stability Analysis of 1-D and 2-D Fixed-Point State-Space Digital Filters Using any Combination of Overflow and Quantization Nonlinearities, *IEEE Trans. Signal Processing*, Vol. 49, (2001), pp. 1097-1105.
- 2. Bauer, P. H. and Ralev, K. R., A Limit Cycle Suppressing Arithmetic Format for Digital Filters, *IEEE Trans. Circuits and Systems-I: Fundamental Theory and Applications*, Vol. 45, (1998), pp. 1104-1107.
- 3. Xu, G. F. and Bose, T., Elimination of Limit Cycles Due to Two's Complement Quantization in Normal Form Digital Filters, *IEEE Trans. Signal Processing*, Vol. 45, (1997), pp. 2892-2895.
- 4. Bauer, P. H. and Premaratne, K., Limit Cycle in Delta-Operator Formulated 1-D and m-D Discrete-Time Systems with Fixed-Point Arithmetic, *IEEE Trans. Circuits and Systems-I: Fundamental Theory and Applications*, Vol. 44, (1997), pp. 529-537.
- 5. Premaratne, K., Kulasekere, E. C., Bauer, P. H. and Leclerc, L.-J., An Exhaustive Search Algorithm for Ckeching Limit Cycle Behavior of Digital Filters, *IEEE Trans. Signal Processing*, Vol. 44, (1996), pp. 2405-2412.

- 6. Bauer, P. H. and Wang, J., Limit Cycle Bound for Floating Point Implementations of Second-Order Recursive Digital Filters, *IEEE Trans. Circuits and Systems-II: Analog and Digital Signal Processing*, Vol. 40, (1993), pp. 493-501.
- 7. Bose, T. and Chen, M. Q., Stability of Digital Filters Implemented with Two's Complement Truncation Quantization, *IEEE Trans. Signal Processing*, Vol. 40, (1992), pp. 24-31.
- 8. Bauer, P. H. and Leclerc, L.-J., A Computer-Aided Test for the Absence of Limit Cycle in Fixed-Point Digital Filters, *IEEE Trans. Signal Processing*, Vol. 39, (1991), pp. 2400-2410.
- 9. Bose, T. and Brown, D., Limit Cycle in Zero Input Digital Filters Due to Two's Complement Quantization, *IEEE Trans. Circuits and Systems*, Vol. 37, (1990), pp. 568-571.
- 10. Ralev, K. R. and Bauer, P. H., Realization of Block Floating-Point Digital Filters and Application to Block Implementations, *IEEE Trans. Signal Processing*, Vol. 47, (1999), pp. 1076-1086.
- 11. TRÂ *N*-THÔŃG and Liu, B., Limit Cycles in Combinatorial Implementation of Digital Filters, *IEEE Trans. Acoustics, Speech, and Signal Processing*, Vol. ASSP-24, (1976), pp. 248-256.
- 12. Munson, D. C., Strickland, J. H. and Walker, T. P., Maximum Amplitude Zero-Input Limit Cycles in Digital Filters, *IEEE Trans. Circuits and Systems*, Vol. CAS-31, (1984), pp. 266-275.
- 13. Green, B.D. and Turner, L.E., New Limit Cycle Bounds for Digital Filters, *IEEE Trans. Circuits and Systems*, Vol. 35, (1988), pp. 365-374.
- 14. Leclerc, L.-J. and Bauer, P. H., New Criteria for Asymptotic Stability of One- and Multidimensional State-Space Digital Filters in Fixed-Point Arithmetic, *IEEE Trans. Signal Processing*, Vol. 42, (1994), pp. 46-53.
- 15. Lepschy, A., Main, G.A. and Viaro, U., Effects of Quantization in Second-Order Fixed-Point Digital Filters with Two's Complement Truncation Quantizaters, *IEEE Trans. Circuits and Systems*, Vol. 35, (1988), pp. 461-466.