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Vertical organic permeable dual-base transistors for logic circuits

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Vertical-channel organic dual-gate/base transistors would be highly interesting since vertical organic transistors are the fastest organic transistors demonstrated today. However, incorporating a dual gate/base structure into an ultra-short channel vertical architecture represents a substantial challenge. Here, we successfully realize a new device concept of vertical organic permeable dual-base transistors (OPDBTs), where either of both base electrodes can be used to change the on-currents and tune the threshold voltages. The optimized devices yield a high on-current density of 1.54 A cm^{-2} and a large current gain of 9.2×10^5, corresponding to a high transmission value of 99.998%. The detailed operation mechanisms are investigated by calibrated TCAD simulations with the Poole-Frenkel mobility model, Gaussian density of states and tunneling model. Finally, high-performance logic circuits, e.g. inverter, NAND/AND computation functions are demonstrated with one single OPDBT operating at supply voltages of < 2.0 V. We believe that OPDBTs offer a compact and technologically simple hardware platform with excellent application potential for vertical-channel organic transistors in complex logic circuits.

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Introduction

Organic thin-film transistors (OTFTs) can be applied for flat panel displays[1–5], radio frequency identification tags[6], and sensor arrays[7,8] owing to their excellent properties for realizing flexible, large-area electronic devices[9,10]. Organic-transistor integrated circuits for driving paper-like displays and large-area sensors have been commercially manufactured in the last decades[11,12]. Despite these advances of organic transistors, one of the major remaining issues on organic-transistor integrated circuits is the control of their threshold voltages (V_{th})[13,14], i.e. the gate bias at which the transistor switches between the high current accumulation regime and the low current depletion regime. The threshold voltage control is crucial for the design and manufacture of complicated integrated circuits. For logic gates, the threshold voltage determines the trip point, which is the input bias at which the gate inverts the output signal[15]. For sensing applications, the threshold voltage signifies the bias at which the largest change in current occurs, i.e. the point of the highest sensitivity[16,17], Although there are reports in which the V_{th} of organic transistors is changed by doping of the organic semiconductors[18] and by modifying the surface of the gate dielectric layers[19,20], such approaches are still far from practical use due to the limited reliability of the manufacturing process.

To address the threshold control issue, dual-gate transistors, consisting of a single thin-film transistor with an additional second gate and second dielectric, have been developed[7,13,15,17,21]. Since the electrostatic potential and the carrier density in the whole film become a function of the second gate bias, threshold voltage V_{th} and the off-state current can be easily tuned. Lateral-channel organic dual-gate transistors with a steeper subthreshold slope, improved carrier mobility and an increased on/off ratio have been

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demonstrated[15,22]. The second gate effectively doubles the width of the channel, yielding a higher current. Additionally, the opposing gate improves the gate modulation by deeper depletion of the bulk semiconductor, leading to a steeper subthreshold slope. Furthermore, the threshold voltage shift in the transistors depends linearly on the capacitive coupling (ratio between the top and bottom gate capacitance), and the control of threshold voltages by the second gate has been demonstrated in logic and integrated circuits[15]. Dual-gate digital integrated circuits have been used to drive actuators in a Braille sheet display and to be configured as self-contained logic gates[7].

Vertical organic transistors have been intensively investigated in the last years[23–28]. Because of their short effective channel length, they can overcome the limits of conventional organic thin-film transistors such as a low on-state current density and a low switching speed. Organic permeable-base transistors (OPBTs)[29,30], including a central electrode (base) between two outer contacts (emitter and collector) separated by organic layers, have reached a record transition frequency of 40 MHz[31], exhibiting great potential for switching applications. Given that the lateral-channel organic dual-gate transistors can realize high-performance logic circuits via tuning V_{th}, thus powerful vertical stacked dual-gate/base organic transistors are highly desirable. However, to the best of our knowledge, there have been no vertical organic dual gate/base transistors reported until now. It is still challenging to precisely construct and control the dual gate/base in the vertical channel organic transistors.

Here, we report the new device concept of vertical organic permeable dual-base transistors (OPDBTs) combining two spatially separated base electrodes to simultaneously enable to change the on-currents and tune the threshold voltages.

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Accordingly, a high on-current density of 1.54 A cm^{-2}, a large current gain of 9.2×10^5, and a high transmission value of 99.998% are demonstrated in the present OPDBTs. Meanwhile, logic circuits acting as inverter, NAND gates and AND gates operation are realized in a single-stacked OPDBT combined with a resistive load.

Device structure and characterization

A schematic of an organic permeable dual-base transistor (OPDBT) is shown in Fig. 1a. The transistor consists of simple sandwich-like architecture, four parallel electrodes (gray and green) are separated by an organic semiconductor (orange). The electron conductive material C_{60} is used to realize an n-type OPDBT. All base contacts consist of a 15 nm-thick Al layer, which are covered by a thin native oxide layer formed after exposure to air. In this transistor, a 20 nm-thick layer of C_{60} doped with the efficient n-dopant $W_2(hpp)_4$ (n-C_{60}, dopant concentration of 1.0 wt.%) is inserted underneath the emitter electrode in order to reduce the contact resistance and enable an Ohmic-like injection from the metal electrode [32–34].

Cross-section transmission electron microscopy (TEM) in Fig. 1a shows the stacked layer of an OPDBT device. The top and bottom electrodes are made of Al and Cr, the C_{60} semiconductor layer with contact doping is interfacing the emitter electrode, and the oxide-passivated Al base electrodes, which are permeable for electrons are in the middle of the stack. The scanning electron microscopy (SEM) image in Fig. 1b depicts the surface morphology of the base electrode on the C_{60} film after exposure to ambient air for 15 minutes. The element distribution (Al, O) in Al electrodes have been analyzed in our previous publication, the AlOx thickness at bottom and top side of the base electrodes is about 5 nm, the density of pinholes is up to 50 μm^{-2}, and the diameter is

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about 5 nm[35]. The pinholes at grain boundaries of the Al film can effectively facilitate charge carrier transport across the electrode. To confine the active area of the devices, two insulating layers of thermally evaporated SiO are inserted before depositing the emitter (Fig. 1a). The insulating layers have two crossed stripe-like open windows which define a quadratic active area of 250 μm in length and 250 μm in width (see Fig. 1c) in OPDBTs. Fig. 1d shows our OPDBT devices on a glass substrate including four transistors.

Before we examine dual-base transistors, the quality of the permeable base electrodes in an OPDBT is firstly investigated by floating one base. In the following, all electrical measurements refer to the common-emitter configuration (emitter on ground). Figs. 2a and c depict the transfer characteristics of OPDBTs measured by floating base1 and base2, respectively. Both cases show a reliable transistor behavior with on-currents of greater than 1.19 A cm^{-2} when floating base1, and 2.25 A cm^{-2} when floating base2 at V_C = 2.0 V. Supplementary Table S1 summarizes the performance parameters of OPDBTs when floating one of the bases. Transfer curves of the OPDBTs with floating base1 reveal a transmission value of 99.996%, an on/off current ratio of 6.6 × 10^3, corresponding to a current gain of 7.7 × 10^5 at V_{B1} = V_C = 2.0 V. For floating base2, the device shows a transmission value of 99.965%, and an on/off current ratio of 1.6 × 10^4, corresponding to a current gain of 1.4 × 10^5 at V_{B2} = V_C = 2.0 V. The current gain (β = I_C/I_B) and transconductance (g_m = dI_C/dV_B) curves of OPDBTs operating when floating one of the bases are shown in Supplementary Figs. 1 and 2, respectively. High current gain values indicate that the base leakage current is effectively suppressed by the native oxide layer formed on the base electrodes. Furthermore, the capacitance and phase

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curves versus base voltages at different supplied frequencies (1 kHz, 10 kHz, and 100 kHz) are shown in Supplementary Fig. 3. The frequency independent depletion capacitance of the base oxide together with the phase remaining close to -90°, indicates good insulating properties of the base oxide layer[36–38].

The stability of OPDBTs measured by floating one of the bases is further studied (see Supplementary Fig. 4). After sweeping 100 cycles, semi-logarithmic *I*-*V* curves only show a small drop due to bias stress effects and degradation of the device characteristics[39]. The output curves are measured at different base voltages of the OPDBTs for floating base1 and base2 electrodes in Figs. 2b and d, respectively. The output curves show promising behavior with a large degree of current control and saturation, even though the curves exhibit a slight nonlinear behavior at low V_C due to the contact resistance at the electrode interface[40–42]. The breakdown voltages of OPDBTs are also tested, as shown in Supplementary Fig. 5. The transistor is set into the off-state by applying one base with a voltage of -0.5 V and floating another one. By varying the collector voltage, OPDBTs can withstand a potential drop of 15.0 V. Hence, OPDBTs are sufficiently robust for logic circuit operation and all these results confirm the promising nature for our OPDBTs and thus excellent potential for applications.

The electrical performance of our OPDBTs for simultaneous variation of the base1 and base2 potential is shown in Fig. 3. The transfer characteristics of the OPDBTs are measured in Fig. 3a. The corresponding calculated performance parameters of the transfer curves, e.g. transmission values, on-current density, on-off ratio, the threshold voltage (V_{th}), transconductance ($g_{m.max.}$), subthreshold swing (SS) and current gain ($\beta_{max.}$), are also summarized in Supplementary Table 2. Fig. 3a shows the I_C-V_{B2} curves of the

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OPDBTs measured with various V_{B1} from 0 to 2.0 V. When V_{B1} = 0 V, the collector current stays at the lowest value (~10^{-7} A) in the range of the base2 sweep bias, indicating the OPDBT stays in its off-state. As V_{B1} increases from 0 to 0.5 V, the OPDBTs can be turned on and the on-current (~10^{-5} A) at V_{B2} = 2.0 V increases by two orders of magnitude than that of the collector current at V_{B1}= 0 V. As the voltage of base1 further increases, the on-state current also increases sharply, the peak of on-current reaches 1.54 A cm^{-2}. Overall, the operation status of the OPDBTs is determined not only by the base2 voltage but also by the base1 voltage.

Importantly, for the base2 sweeps, the transfer curves shift with the applied base1 bias from 0.5 V to 2.0 V, so that the threshold voltages also gradually shift from 0.04 V to 0.52 V (the threshold voltage is extracted by the point where the collector current starts to rise exponentially with the base voltage). Similarly, for base1 sweeps (see Fig. 3c), transfer curves also present the on-current change and threshold voltage shifts (from 0.68 to 0.92 V) with the applied base2 bias from 0.5 V to 2.0 V. Moreover, as can be seen in Supplementary Table 2, the transmission values, on/off ratios, and the transconductance of the transfer curves increase as the bias of the other control base increases from 0 to 2.0 V. Accordingly, applying the voltage to one of the base electrodes allows us to modulate the charge transmission, further increasing induces more charges and higher on-current, and consequently sets the threshold voltages of transistors. The transfer characteristics at the highest base voltage of 2.0 V show that the on/off-current levels in Figs. 3a and c match well with the ones extracted in Figs. 2a and c.

Energy diagrams relating to the four operation modes of the OPDBTs are shown in Supplementary Fig. 6. When base1 is at low potential (Supplementary Fig. 6a), the

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electrons can not flow to the base1 electrode, representing the off-state of the OPDBTs. The built-in potential can lead to an electric field, which would push the electrons away from the base1 region and thus prevents the current flow through the base1 electrode. When the base1 is at a high potential and the base2 at a low potential, electrons will accumulate at base1 and can not pass through base2, as shown in Supplementary Fig. 6b. Because the base electrodes are wrapped by the native oxide layer, electrons can also not flow into base1, leading to the disturbing base1 leakage[43]. Hence, the desirable result that electrons can pass through the openings in both base layers and reach the collector only happens when the base1 potential is non-zero and base2 potential larger than that of base1 (see Supplementary Fig. 6c).

The base leakage currents for base1 sweeps with fixed base2 voltages from 0 to 2.0 V and for base2 sweep with fixed base1 voltages from 0 to 2.0 V are shown in Supplementary Figs. 7a and b, respectively. Compared to the base leakage in Fig. 2, the base leakage during dual-base measurement is lower than that of by floating one base. Consequently, we obtain a large current gain of 9.6×10^5 at a fixed V_{B1} of 2.0 V, and equal $V_C = V_{B2} = 2.0$ V in Fig. 3a, and 7.6×10^4 for the base2 sweeps (see Supplementary Fig. 8). Output characteristics of OPDBTs are measured and presented in Figs. 3b and d where a reasonable degree of saturation in the collector current is observed. It should be noted that the I_C-V_C curves are slightly nonlinear at low collector-emitter voltages, indicating the presence of the contact resistance at the electrode interface[40–42]. The bias stress stability of OPDBTs at a low voltage of $V_C = 2.0$ V and $V_{B2} = V_{B1} = 1.5$ V are also performed, as shown in Supplementary Fig. 9. It can be seen that the collector current,

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base1, and base2 currents are very stable during the stress measurement, small collector current change can be attributed to the charge trapping effects[44,45].

TCAD simulations of OPDBTs

A schematic cross-section of the simulated structure with the device dimensions listed in Supplementary Table 3, based on fabricated OPDBT is shown in Fig. 4a. The simulated 3D-OPDBT depicting charge density profile of the device at V_{B1} = V_{B2} = V_C = 2.0 V (Fig. 4b) where the carrier density through the pinholes is at its maximum. The device current I_C flowing from emitter to collector has to pass the two base layers through the pinholes. To further elucidate the charge transport and device behavior, the measured electrical response has been compared with theoretical models. A Poole-Frenkel mobility model with a square root dependence on the electric field, Gaussian density of states (DOS) and quantum tunneling current model have been used with their default values except for the calibrated values as shown in Supplementary Table 3[46]. The simulated DC characteristics (W = 250 μm and L = 250 μm) show a very good agreement between simulations (solid lines) and the experimental measurements (diamonds) (see Fig. 4c). Therefore, the calculated device characteristics mimic the measured behavior with high accuracy. Note that the base leakage current is quite small (see Fig. 2) and has a negligible impact on the collector current and has been neglected in the simulation. The calibrated simulator has been taken as a reference to further investigate the performance analysis of OPDBTs.

Figs. 4d-f display the electrostatic potential, charge, and current density profiles of the simulated OPDBT in the different operation regions at V_{B1} = V_C = 2.0 V and different base2 voltages V_{B2} = 0.5, 1.0, 1.5 and 2.0 V. The working principles and the theoretical

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behavior of the fabricated new OPDBTs have been investigated and explored based on the numerical simulation results. In Fig. 4e, when $V_{B1} = V_C = 2.0$ V and $V_{B2} = 0.5$ V, the semiconductor exhibits a higher density of accumulated charge carriers around base1 injected from the emitter. The charge density is very low around the base2 due to lower applied potential ($V_{B2} = 0.5$ V). The carriers accumulated at base1 start to move towards base2 when V_{B2} increases from 1.0 to 1.5 and to 2.0 V. Therefore, the charge density is increasing around base2, resulting in a control of the collector current I_C by modulating the voltage of base2.

It is worth noting that the applied base1 voltage of 2.0 V causes carrier injection from the emitter and leads to the accumulation of charges around the base1. Thus increasing the base2 voltages V_{B2}= 1.0, 1.5 and 2.0 V, causes carrier migration from base1 through the pinholes toward base2 and the pinholes, allowing more carriers to pass towards the collector. Thus the device total current I_C increases (see Fig. 4f). The highest density of charge carriers in the on-state is observed in the openings (pinholes) which have a diameter of a few nanometers.

Logic circuits realized by OPDBTs

By integrating a dual-base transistor with a resistive load, a logic inverter, NAND gate and AND gate circuits are realized experimentally, as illustrated in Fig. 5. The circuit diagram, voltage transfer characteristics (VTCs), and truth table of a resistive load inverter composed of a 400k Ω external resistance and an OPDBT are shown in Figs. 5a-c for different supply voltages, respectively. In this configuration, only one of the base electrodes of the OPDBTs is employed while the other one is kept floating. The VTCs are fine-tuned by changing V_{CC} and the highest voltage gain (dV_{out}/dV_{in}) is 14 as the input

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varies from 0 to 2.0 V (see Supplementary Fig. 10). Besides the exceptionally small supply voltage, this gain is among the best values reported for unipolar inverters based on organic transistors[47,48]. A good performance and the highest voltage gain of 23 is also obtained for inverters with a depletion load as shown in Supplementary Fig. 11. In this case, the base of a second OPDBT is connected to the output of the inverter while the voltage of base1 is swept again between 0 and 2.0 V (V_{CC}= 2.0 V). Thus, the logic inverters can be simply implemented by using OPDBTs with one base input.

In Figs. 5d-f, the NAND gate operation is realized with an OPDBT as a function of base2 input voltage (V_{IN2}) and fixed base1 voltage (V_{IN1}= 0, 2.0 V), under a supply voltage of 2.0 V. While, Figs. 5g-i show the VTCs of an AND gate when the base1 voltages (V_{IN1}) are fixed at 0 and 2.0 V and the base2 voltage (V_{IN2}) is swept from 0 to 2.0 V under a supply voltage of V_{CC} = 2.0 V. The VTCs in Figs. 5e and h exhibit well high and low states which are the result of the steep transfer curves of the OPDBTs in the logics.

We conclude that logic circuits can be easily realized with our OPDBTs by using two base inputs simultaneously. Unlike conventional unipolar NAND/AND gates consisting of at least two transistors, we implement the NAND/AND gate by using only one vertically stacked dual-base transistors. The independent base control enables the transistor to work at different states by tuning the voltages of two bases (two inputs). OPDBTs with two inputs simplify the fabrication of logic circuits without compromising performance and the reduction of the total number of transistors offers great advantages for integrated circuits (ICs). Hence, since OPDBTs represent a compact and technologically simple hardware platform, they offer excellent application perspectives of vertical-channel organic transistors in complex logic circuits. Furthermore, since OPBTs

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are the fastest organic transistors reported today, OPDBTs also have great potential to be used in the fast logic circuits.

Conclusions

In summary, a new device concept of organic dual-base transistors has been demonstrated. By employing this vertical-channel dual-base structures in organic transistors, we can easily control the threshold voltage which is a main requirement for designing efficient logic circuits. Excellent electrical performance is obtained for this transistor design, e.g. a high on-current density of 1.54 A cm^{-2}, a large current gain of 9.2×10^{5}, and an on/off current ratio of 8×10^{3}, corresponding to a high transmission value of 99.998%, which is almost comparable to single-base OPBTs, the fastest organic transistor reported. The numerical TCAD simulation of the new structure will help to study structure engineering towards optimizing the performance of OPDBTs. The good agreement between experimental data and numerical simulation confirms the viability of the proposed novel device design with a channel length in the range of obly a few hundreds of nanometers. The new functionality enhanced device structure enables to design logic circuits with just one single transistor. To prove the advantage and feasibility of the new design, which are investigated as building blocks of the large-scale circuits, we also demonstrate logic gates including inverters, AND gates and NAND gates which are operating at a voltage as low as 2.0 V and with an excellent gain.

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Methods

Device fabrication. The organic permeable dual-base transistors (OPDBTs) presented are fabricated in a single chamber UHV-tool and one glass substrate previously cleaned with N-Methylpyrrolidone, distilled water, ethanol, and Ultra Violet Ozone Cleaning System. By using thermal vapor deposition at high vacuum ($p < 10^{-7}$ mbar), the layer stack (Fig. 1a) is realized by subsequently depositing thin films through laser-cut, stainless steel shadow masks. The deposition system includes a wedge for realizing samples of different layer thicknesses in one run while other layers remain equal. The layer stack, evaporation rates and treatments of the OPDBTs are: Al 100 nm (2 Å s^{-1})/Cr 10 nm (0.1 Å s^{-1})/i-C_{60} 100 nm (1 Å s^{-1})/Al 15 nm (1 Å s^{-1})/15 min oxidation in ambient air/i-C_{60} 60 nm (1 Å s^{-1})/ Al 15 nm (1 Å s^{-1})/15 min oxidation in ambient air/ i-C_{60} 100 nm (1 Å s^{-1})/ n-C_{60} 20 nm (0.4 Å s^{-1}) co-evaporating C_{60} with W_2 $(hpp)_4$ (purchased from Novaled AG, Dresden) using 1 wt.%/1 x or 2 x (perpendicular to each other) SiO 100 nm with a free stripe of 0.2 mm (1 Å s^{-1})/Cr 10 nm (0.1 Å s^{-1})/Al 100 nm (2 Å s^{-1})/encapsulation under nitrogen atmosphere (<1 ppm O_2 and H_2O) using UV cured epoxy glue and cavity glasses without UV exposure of the active area/annealing for 2 h at 150 °C on a hotplate in a nitrogen glove-box.

Device characterization. Transistor characteristics are measured by using two Keithley 236 together with a Keithley 2400 SMU in a glovebox. For the impedance spectroscopy, an HP 4284A LCR-Meter is used. The optical image is taken by optical microscopy. The scanning electron microscope (SEM) images are captured using a Zeiss Gemini SEM 500. Transmission electron microscopy (TEM) measurements are carried out with a Libra200 (Carl Zeiss Microscopy GmbH, Germany) operated at an acceleration voltage

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of 200 kV. The lamella for TEM is prepared by lift-out focused ion beam (FIB) technique in NEON40 FIB/SEM (Carl Zeiss Microscopy GmbH, Germany).

TCAD simulation. Synopsys' Sentaurus TCAD simulator has been used to simulate 3D structures. The device structure is created by a 3D Sentaurus structure editor. It incorporates advanced physical models and robust numeric methods and simulates the electrical behavior of semiconductor devices. The non-local tunneling model is used to include the contributions of the total tunneling current. Gaussian Density-of-States has been used to better represent effective DOS in disordered organic semiconductors. A simple constant carrier generation model is used.

Data Availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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Author Contributions

Z.W., H.K. and K.L. proposed and supervised the project. E.G. and Z.W. designed the experiment. E.G., Z.W., S.X. and S.W. performed the device characterization. G.D. and A.K. performed the TCAD simulation. A.T. did the SEM analysis and M.G. prepared the FIB lamella for TEM. E.G., Z.W., G.D., H.K. and K.L. analyzed the data and co-wrote the manuscript. All authors discussed the results and commented on the manuscript.

Competing Interests

The authors declare no competing interests.

Additional Information

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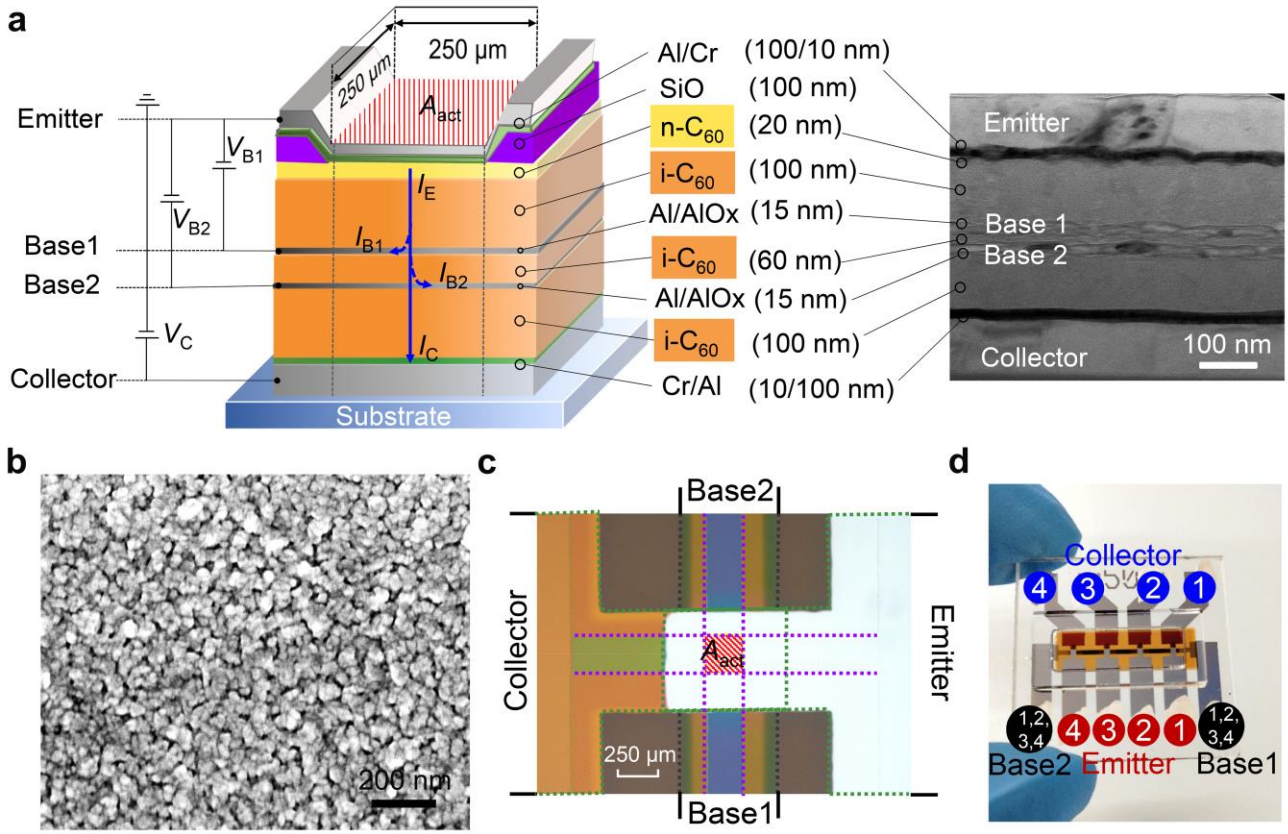

Fig. 1 | Device structure and characterization. **a**, Structure schematic view of an OPDBT measured using common emitter configuration, and cross-section TEM image of an OPDBT. **b**, SEM image of a 15 nm-thick Al covered on a C_{60} layer after oxidation in ambient air. **c**, Optical image of the active area in OPDBT. The active area A_{act} is defined by the overlap of four electrodes: the emitter (E), base1 (B1), base2 (B2), and collector (C). An insulating layer of SiO is used to confine the active area. The current flow happens in an effective region of 250 μm × 250 μm. **d**, Photograph of our OPDBTs on a glass substrate (edge length: 1 in.), including four active OPDBT pixels. With applying base1-emitter voltage (V_{B1}) and base2-emitter voltage (V_{B2}), electrons can pass through the base and hence reach the collector (see **a**). Except for a minor leakage current into the base I_{B1} and I_{B2} (blue dotted arrows), emitter current I_E (solid blue arrow) can finally arrive at the collector, forming collector current I_C.

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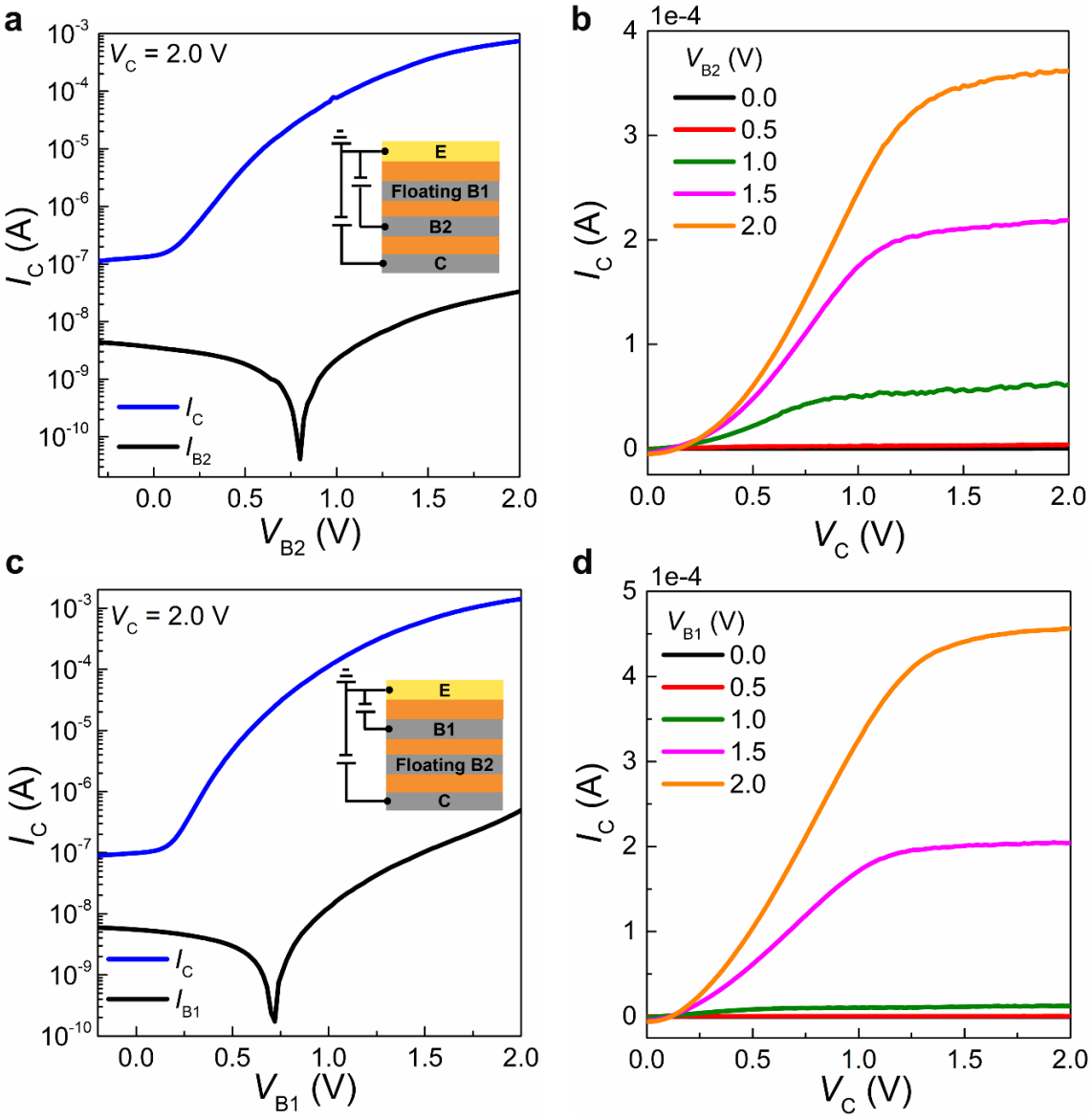

Fig. 2 | Electrical characteristics of OPDBTs measured by floating one base. a-c, Transfer characteristics (**a**) and output characteristics (**b**) of OPDBTs for floating base1. **c-d**, Transfer characteristics (**c**) and output characteristics (**d**) of OPDBTs for floating base2. The insets in **a** and **c** show the circuit connections used for the measurements. Base leakage in two base contacts is negligible compared to collector current, which underlines the high quality of our permeable base electrodes.

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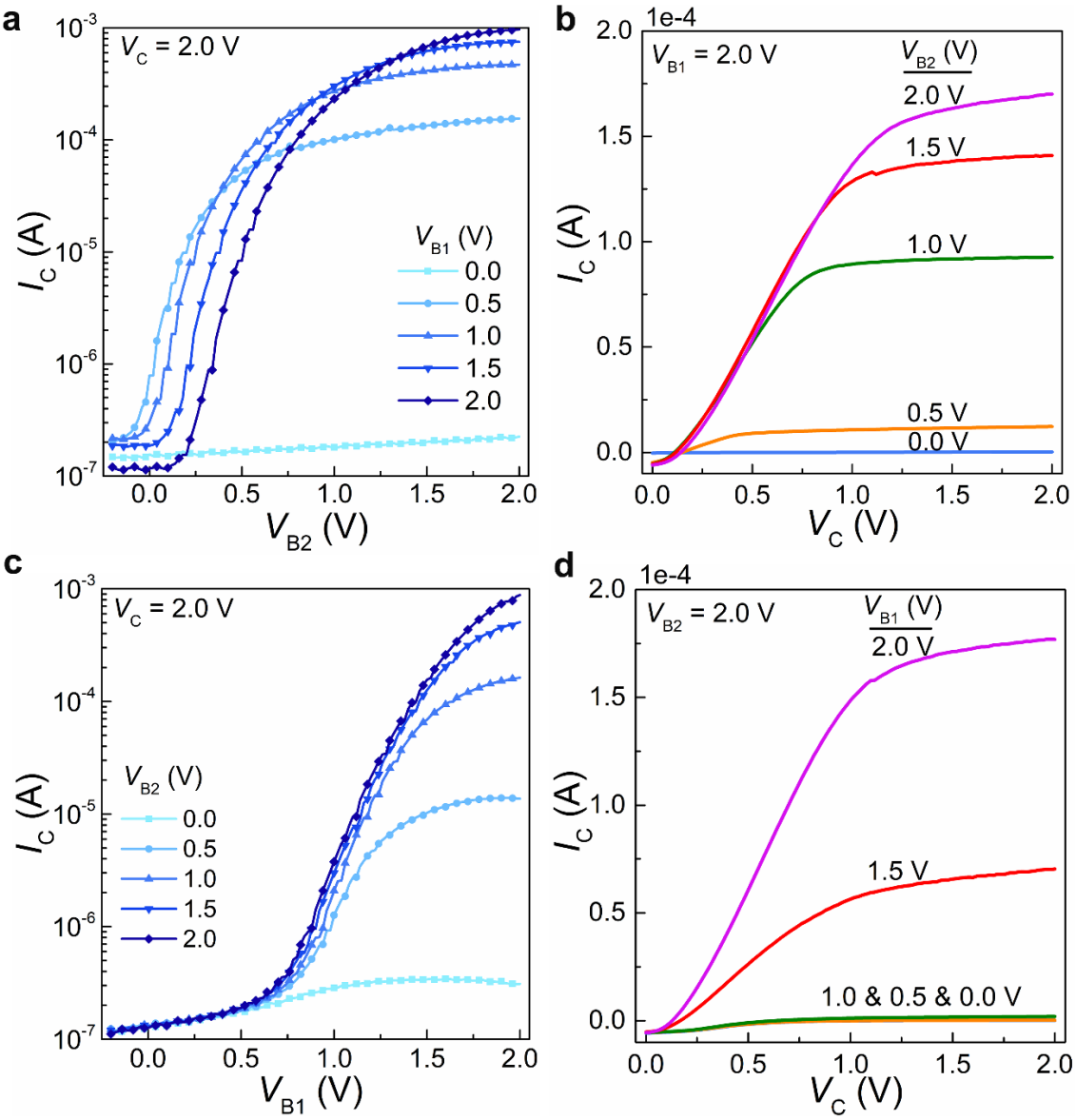

Fig. 3 | Electrical characteristics of OPDBTs. a, Transfer curves as a function of V_{B2} at different V_{B1} of 0, 0.5, 1.0, 1.5 and 2.0 V, respectively. **b**, Output curves of OPDBTs measured under a constant V_{B1} of 2.0 V and V_{B2} of 0, 0.5, 1.0, 1.5 and 2.0 V, respectively. **c**, Transfer curves as a function of V_{B1} at different V_{B2} of 0, 0.5, 1.0, 1.5 and 2.0 V, respectively. **d**, Output curves of OPDBTs measured under a constant V_{B2} of 2.0 V and V_{B1} of 0, 0.5, 1.0, 1.5 and 2.0 V, respectively.

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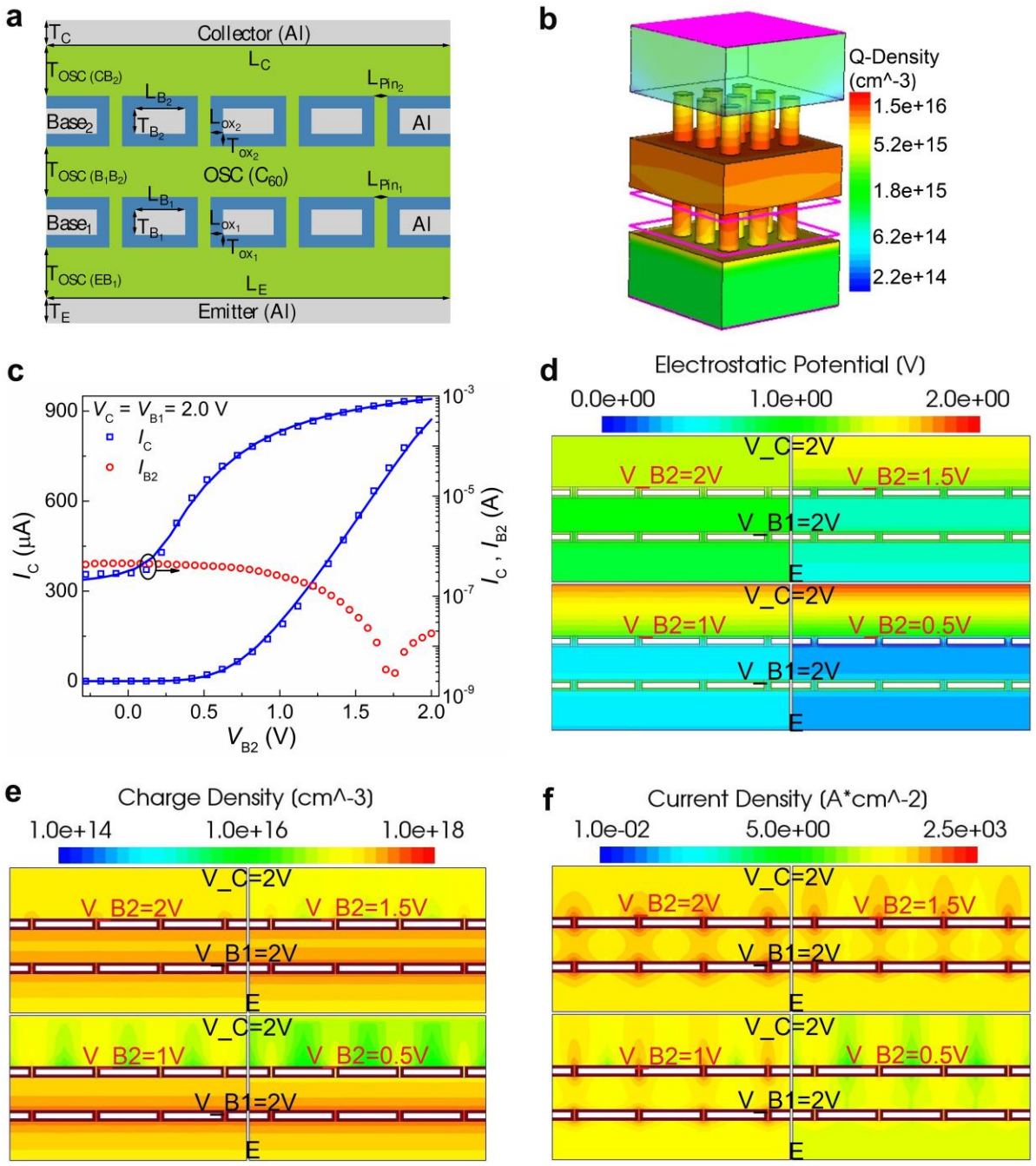

Fig. 4 | TCAD simulation of OPDBTs. **a**, Schematic cross-section of the simulated OPDBT used for Sentaurus TCAD setup. **b**, 3D-OPDBT structure depicting simulated charge density of the same number of pinholes in base1 and base2 $N_{Pin1} = N_{Pin2} = 9$, with the emitter being bottom contact and collector the top contact at $V_{B1} = V_{B2} = V_C = 2.0$ V. **c**, Transfer characteristics: Collector current I_C from experimental data (diamonds) compared with data from TCAD simulation (solid lines), including the neglgible measured base2 leakage current I_{B2} (circles) at $V_{B1} = V_C = 2.0$ V. **d**-**f**, Electrostatic potential (**d**), charge carrier density (**e**), and current density (**f**) profiles of OPDBTs at $V_{B1} = V_C = 2.0$ V and $V_{B2} = 0.5$, 1.0, 1.5 and 2.0 V, respectively.

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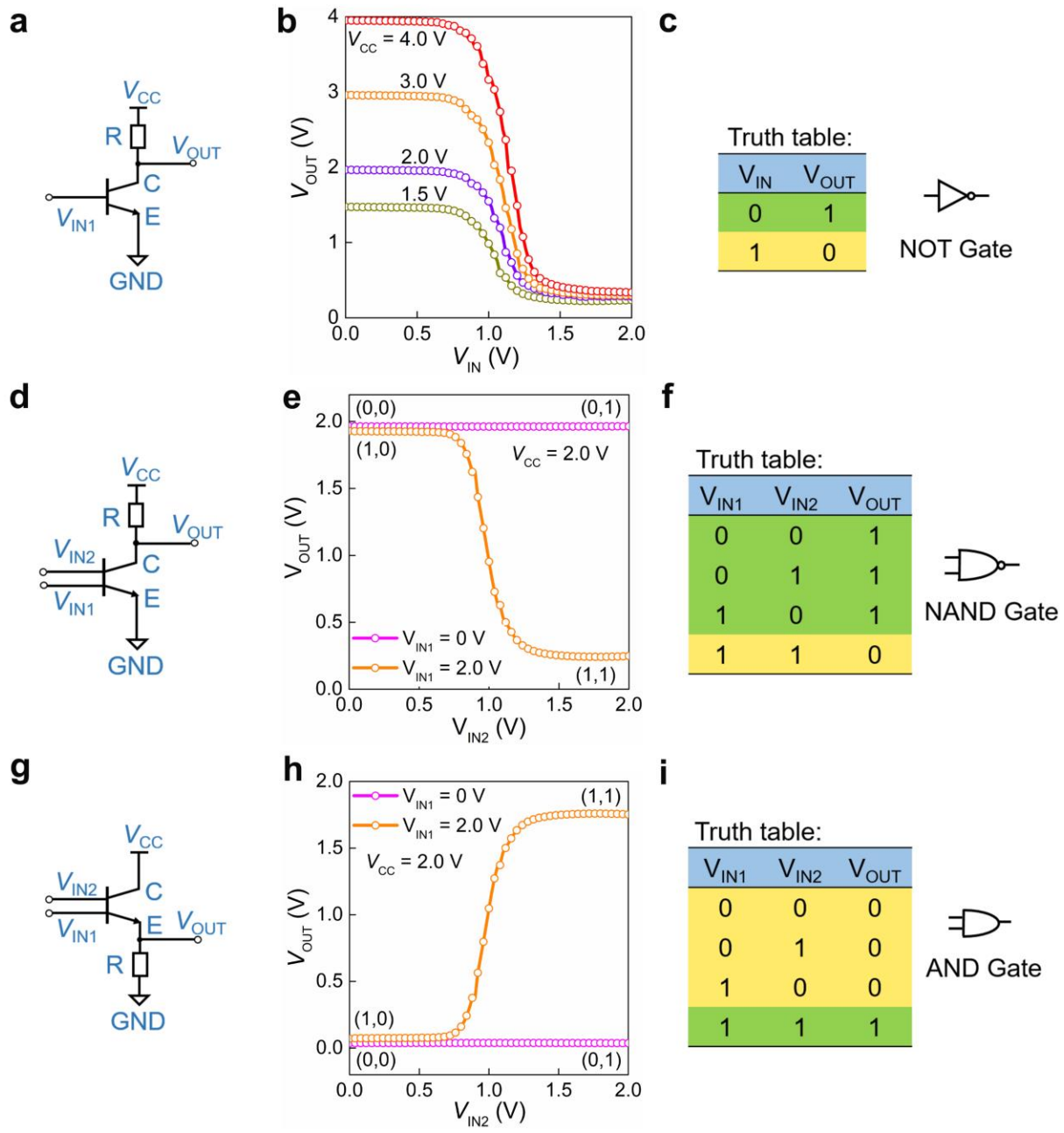

Fig. 5 | Resistive load logics realized by OPDBTs. a-c, Circuit diagram (**a**), voltage transfer characteristics (**b**), and truth table (**c**) of a resistive load inverter realized by an OPDBT and a 400k Ω external resistor as swept by base1 bias under different V_{CC}. **d-f**, Circuit diagram (**d**), voltage transfer characteristics (**e**), and truth table (**f**) of a NAND gate logic circuit as a function of base2 input with fixed base1 bias under V_{CC}= 2.0 V. **g-i**, Circuit diagram (**g**), voltage transfer characteristics (**h**), and truth table (**i**) of an AND gate logic circuit as a function of base2 input with fixed base1 bias under V_{CC}= 2.0 V. GND represents the ground.

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-Supplementary Information-

Vertical organic permeable dual-base transistors for logic circuits

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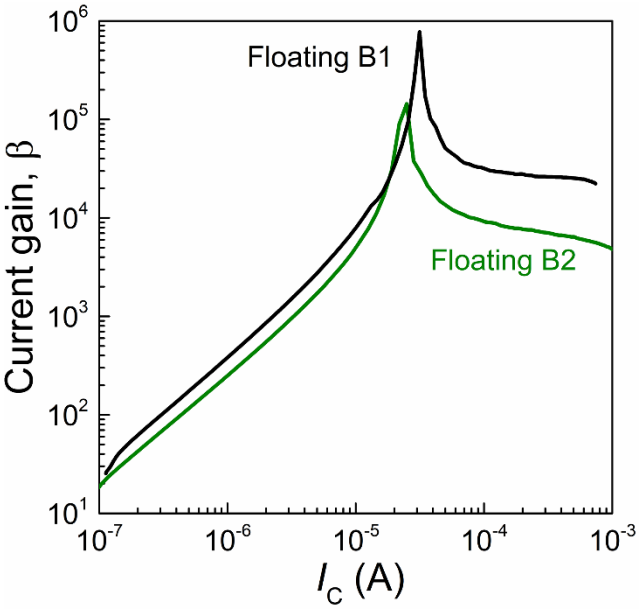
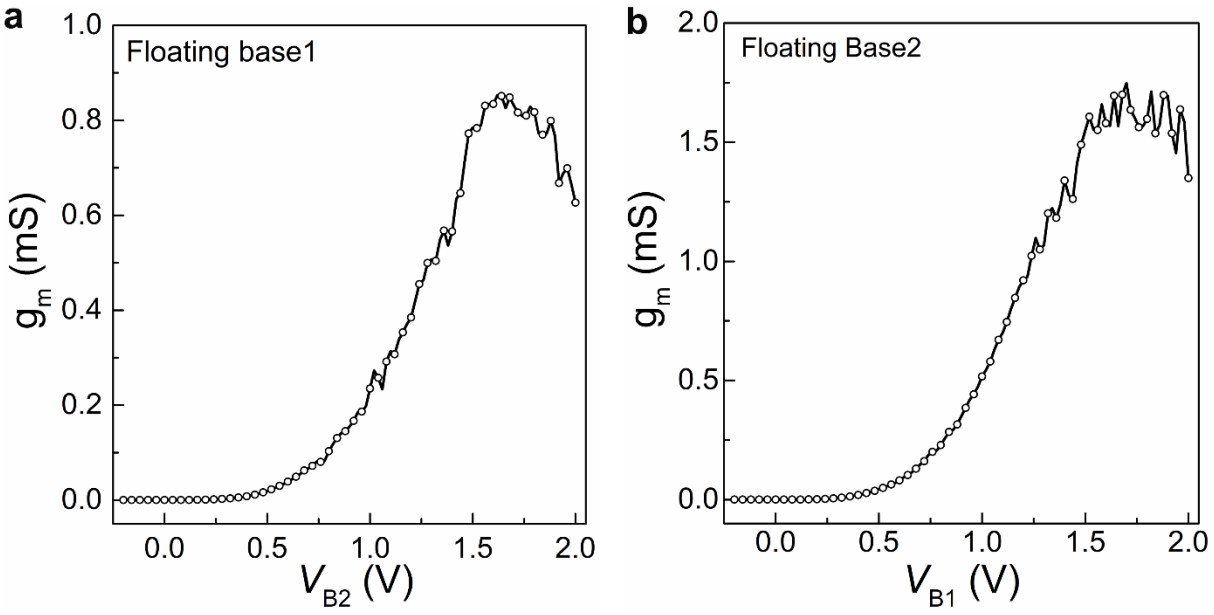


Supplementary Figure 1 | Current gain (β) of OPDBTs measured by floating one base. The maximum current gain of 7.7×10^5 and 1.4×10^5 when floating base1 and base2, respectively.



Supplementary Figure 2 | Transconductance (g_m) of OPDBTs measured by floating one base. a-b, Transconductance when floating base1 (**a**) and base2 (**b**) as a function of the base-emitter voltage. The maximum g_m value is 0.85 mS when floating base1 and 1.75 mS when floating base2.

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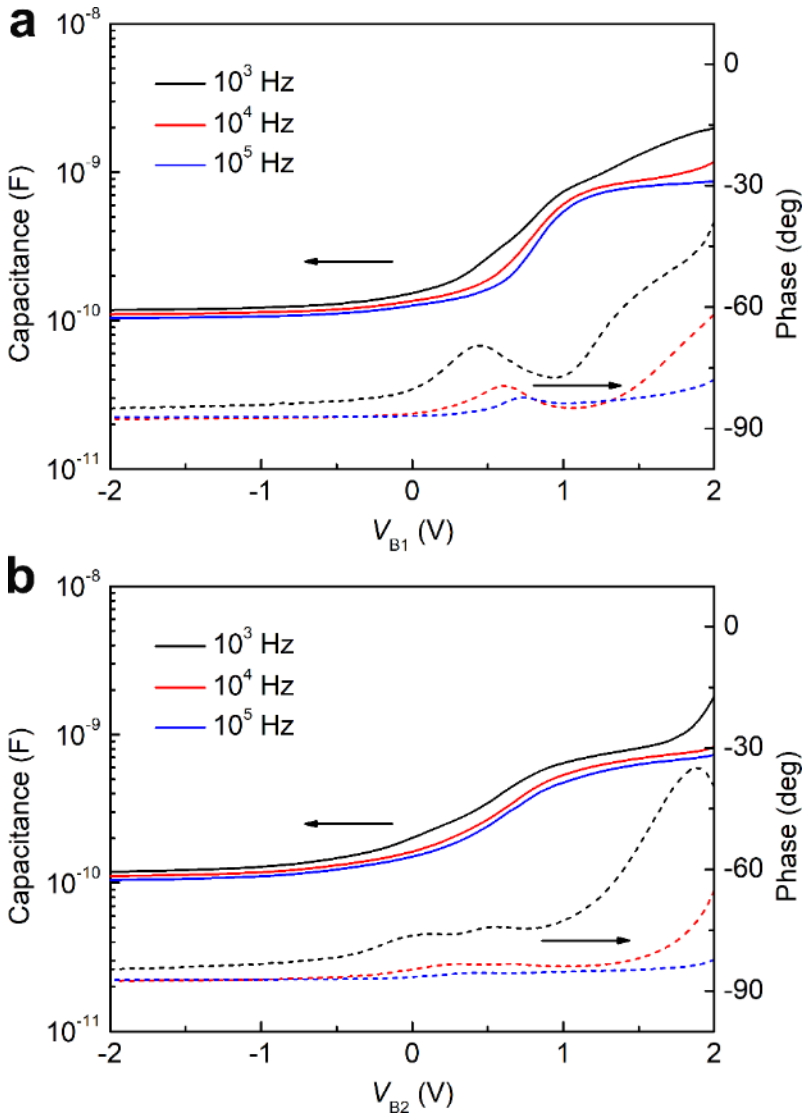

Supplementary Figure 3 | Capacitance and phase of OPBDTs. a, Capacitance and phase curves versus V_{B1} with different frequencies of 1 kHz, 10 kHz, and 100 kHz, respectively. **b**, Capacitance and phase curves versus V_{B1} with different frequencies of 1 kHz, 10 kHz, and 100 kHz, respectively. The phase stays close to -90°, indicating excellent insulating properties of the base oxide layer.

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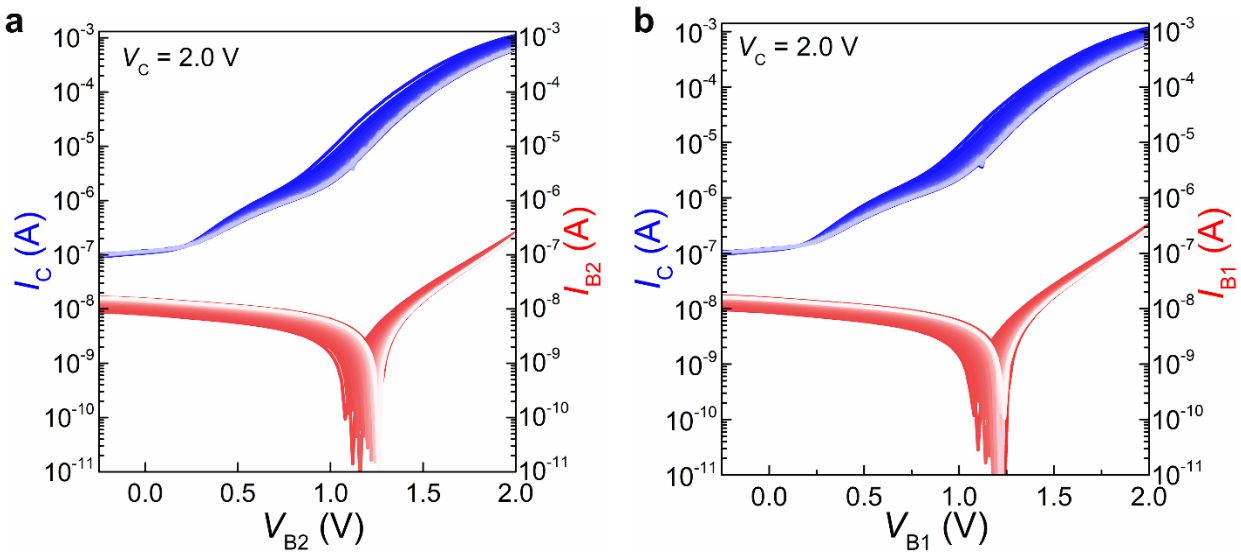
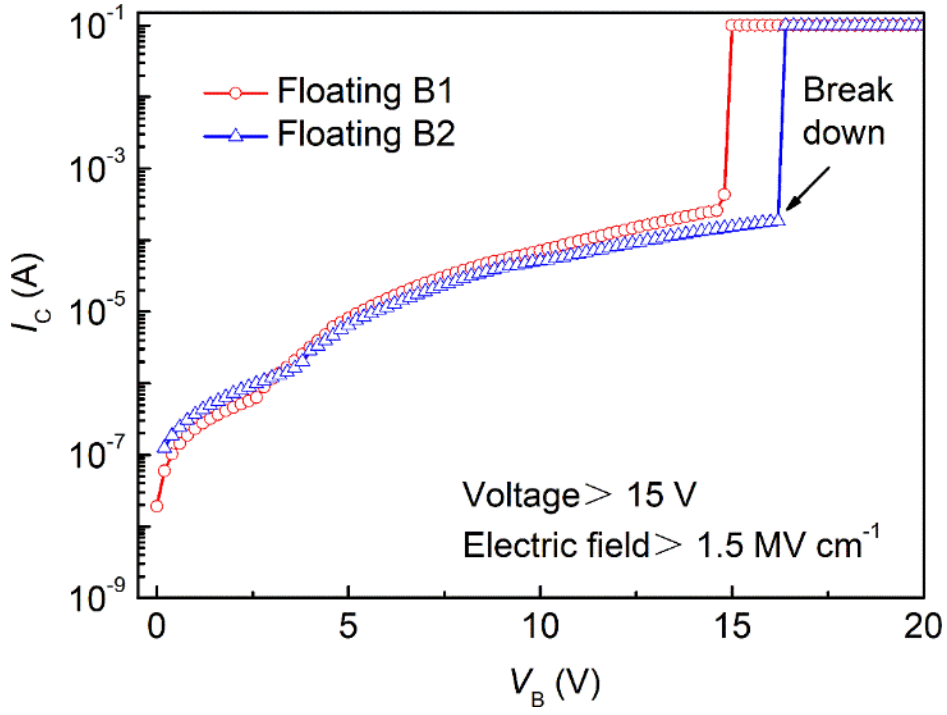


Supplementary Figure 4 | Operational stability. **a**-**b**, Semi-logarithmic *I*-*V* curves with 100 cycles of voltage sweeping for floating base1 (**a**) and for floating base2 (**b**).



Supplementary Figure 5 | Breakdown voltages. OPDBTs withstand electric field between base and collector greater than 1.5 MV cm^{-1} in off-state.

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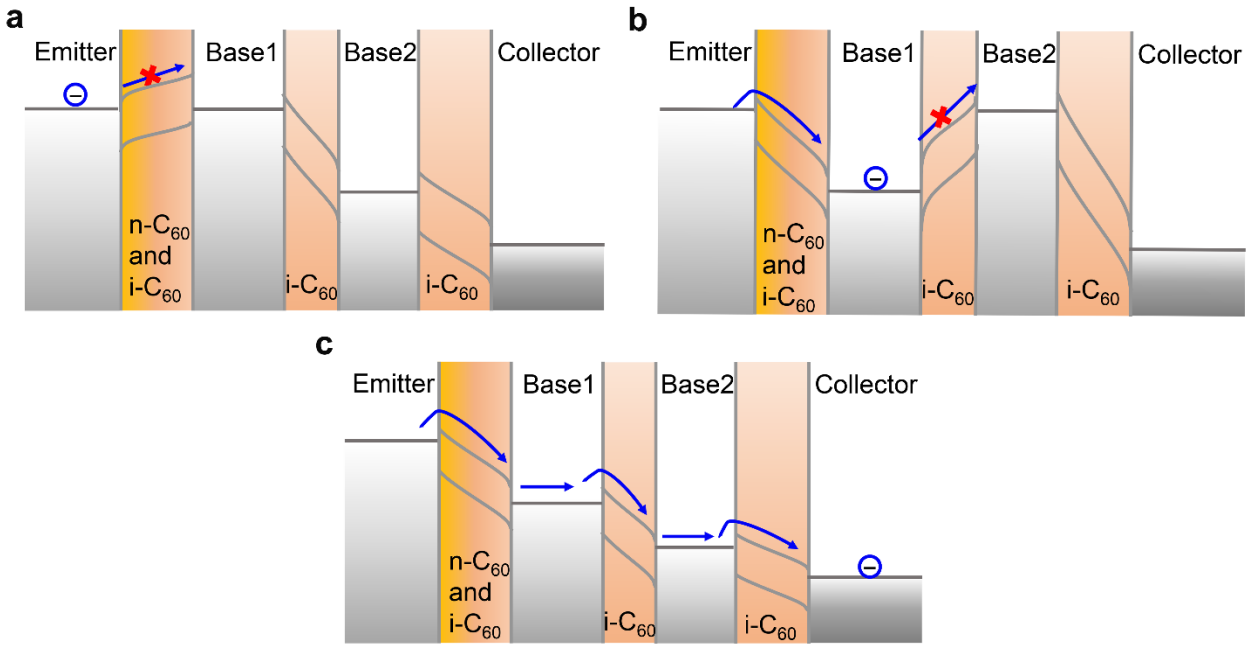
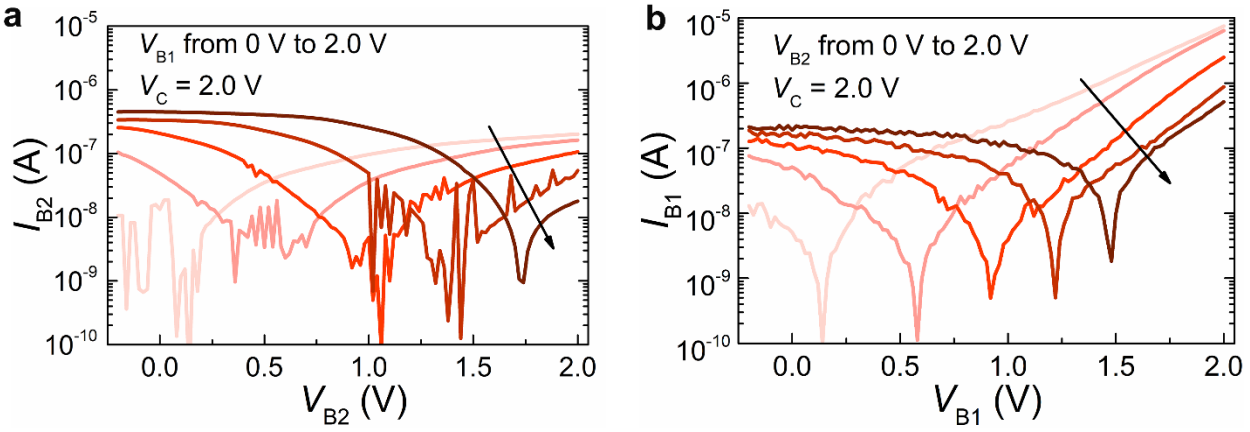


Supplementary Figure 6 | Energy band diagrams. a-c, Energy band diagrams of OPDBTs in off-state when base1 at low potential (**a**) and when base1 at high potential but base2 at low potential (**b**). **c,** Energy band diagram of OPDBTs in on-state (high base1 potential and higher base2 potential than base1), electrons can pass through the openings in both bases and reach the collector.



Supplementary Figure 7 | Base leakage currents. **a**, Base2 leakage current curves obtained during base2 sweep when V_C = 2.0 V and V_{B1E} = 0, 0.5, 1.0 and 2.0 V, respectively. **b**, Base2 leakage current curves obtained during base1 sweep when V_C = 2.0 V and V_{B2E} = 0, 0.5, 1.0 and 2.0 V, respectively.

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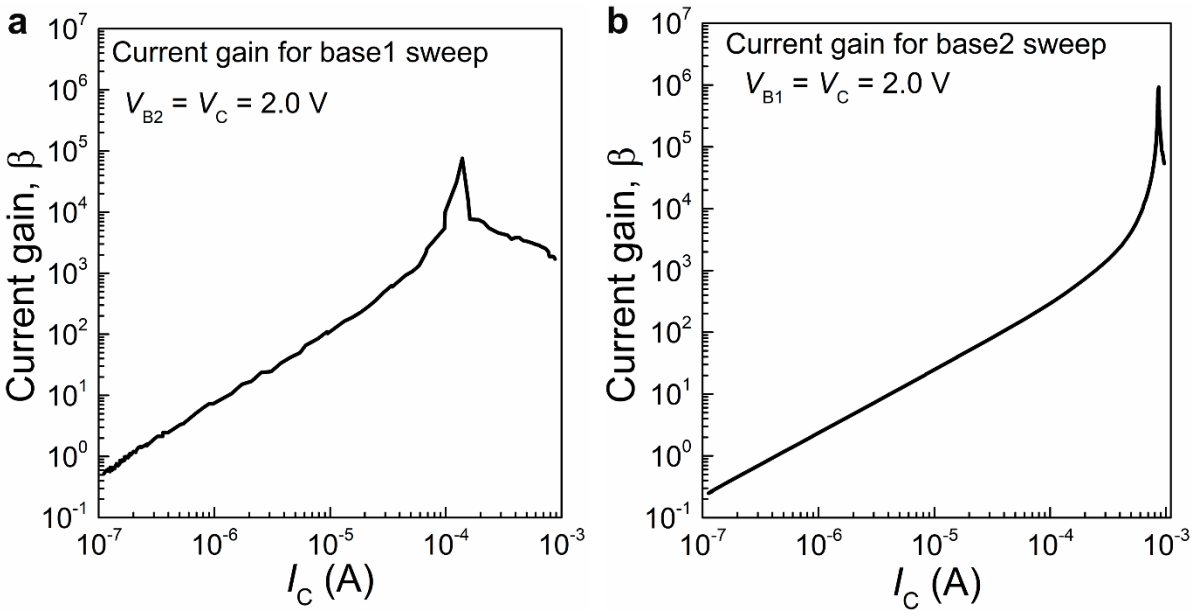
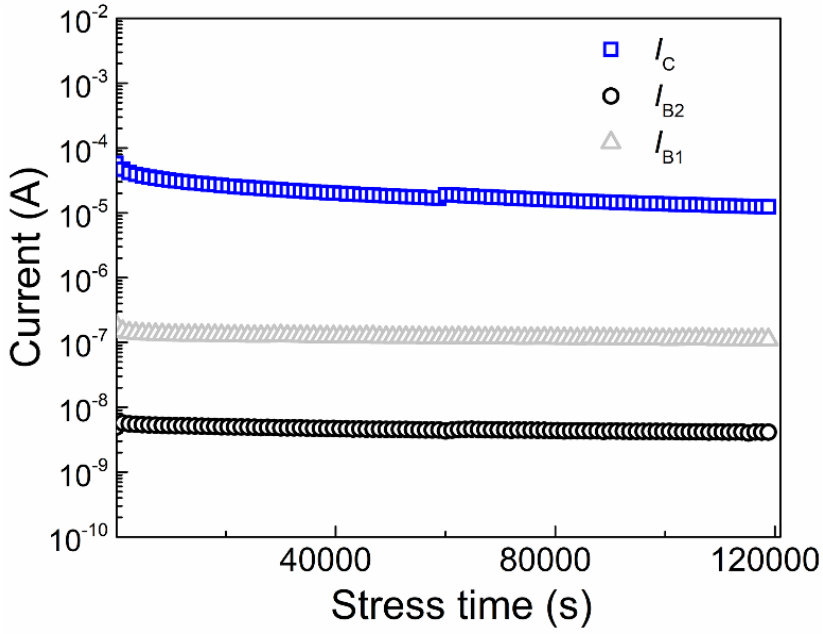


Supplementary Figure 8 | Current gain. **a**, Current gain of OPDBTs obtained during base1 sweep when V_{B2} = V_C = 2.0 V as a function of collector current. **b**, Current gain of OPDBTs obtained during base2 sweep when V_{B1} = V_C = 2.0 V as a function of collector current.



Supplementary Figure 9 | Bias stress stability. Bias stress measurement of OPDBTs when V_C = 2.0 V and V_{B2} = V_{B1} = 1.5 V.

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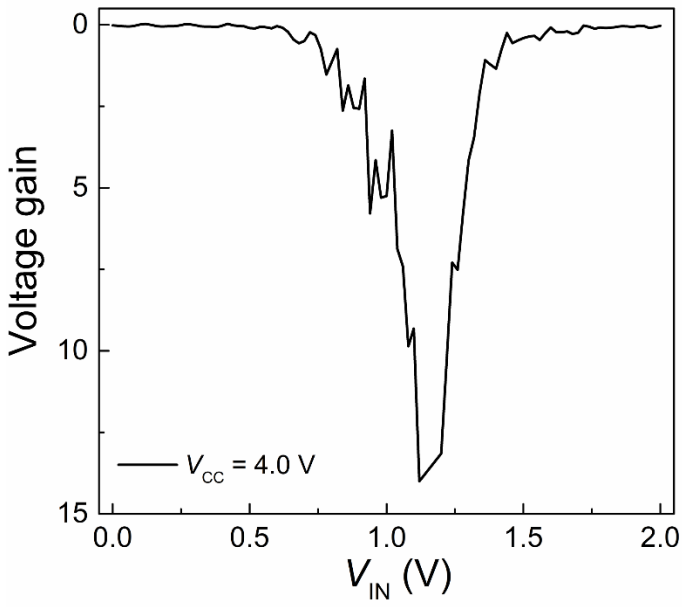
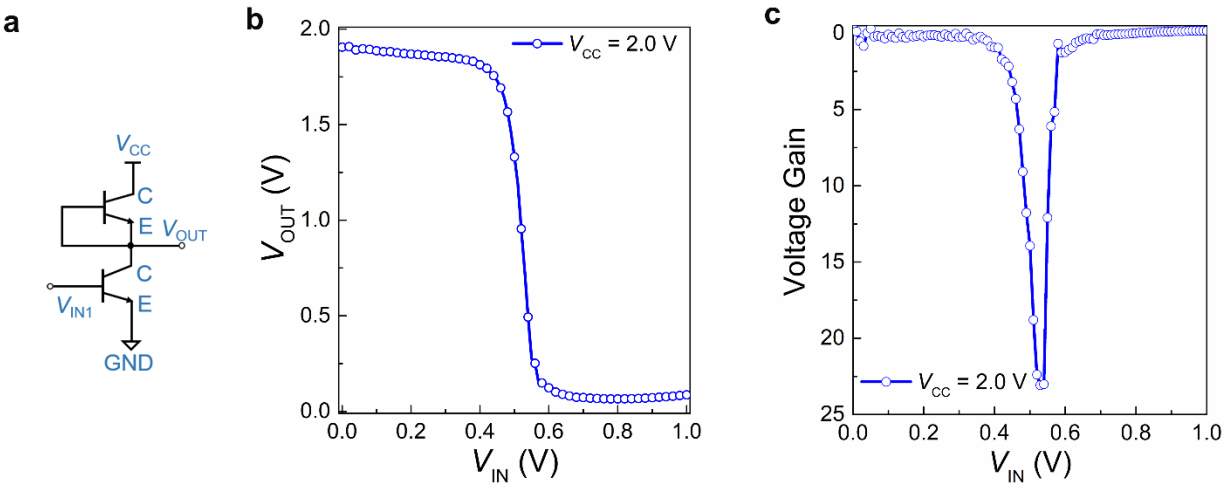


Supplementary Figure 10 | Voltage gain. Voltage gain of the resistive load inverter when supply voltage V_{CC} = 4.0 V.



Supplementary Figure 11 | Inverter with depletion load. **a**-**c**, Circuit diagram (**a**), experimental voltage transfer characteristics (**b**), and voltage gain (**c**) of an inverter realized by an OPDBT and a depletion load as swept by base1 bias when V_{CC} = 2.0 V.

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Supplementary Table 1. **Summary of OPDBTs measured by floating one base**. Transmission value, on-current density, on-off ratio, threshold voltage (V_{th}), transconductance ($g_{m.max.}$), subthreshold swing (SS) and current gain ($\beta_{max.}$) of OPDBTs measured by floating one base.

	Transmission	On-current density (A cm^{-2})	On/off ratio	V_{th} (V)	$g_{m.max.}$ (mS)	SS (mV dec^{-1})	$\beta_{max.}$
Floaing base2	99.965% V_C=V_{B1} =2.0 V	2.25 V_C=V_{B1} =2.0 V	1.6×10^4	0.4	1.75	200	1.4×10^5
Floating base1	99.996% V_C=V_{B2} =2.0 V	1.19 V_C=V_{B2} =2.0 V	6.6×10^3	0.4	0.85	263	7.7×10^5

Supplementary Table 2. **Summary of OPDBTs**. Transmission value, on-current density, on-off ratio, threshold voltage (V_{th}), transconductance ($g_{m.max.}$), subthreshold swing (SS) and current gain ($\beta_{max.}$) of OPDBTs.

	Transmission	On-current density (A cm^{-2})	On/off ratio	V_{th} (V)	$g_{m.max.}$ (mS)	SS (mV dec^{-1})	$\beta_{max.}$
Base2 sweep V_{B1} = 0.0 V	52.649% V_C=V_{B2} =2.0 V	3.59×10^{-4} V_C=V_{B2} =2.0 V	1.5	-	-	-	-
Base2 sweep V_{B1} = 0.5 V	99.895% V_C=V_{B2} =2.0 V	0.248 V_C=V_{B2} =2.0 V	7.5×10^2	0.04	0.14	130	-
Base2 sweep V_{B1} = 1.0 V	99.977% V_C=V_{B2} =2.0 V	0.749 V_C=V_{B2} =2.0 V	2.2×10^3	0.16	0.44	136	-
Base2 sweep V_{B1} = 1.5 V	99.993% V_C=V_{B2} =2.0 V	1.2 V_C=V_{B2} =2.0 V	4.0×10^3	0.30	0.72	126	-
Base2 sweep V_{B1} = 2.0V	99.998% V_C=V_{B2} =2.0 V	1.544 V_C=V_{B2} =2.0 V	8.0×10^3	0.52	0.95	152	9.2×10^5
Base1 sweep V_{B2} = 0.0 V	3.979% V_C=V_{B1} =2.0 V	4.98×10^{-4} V_C=V_{B1} =2.0 V	1.9	-	-	-	-
Base1 sweep V_{B2} = 0.5 V	68.159% V_C=V_{B1} =2.0 V	0.022 V_C=V_{B1} =2.0 V	1.1×10^2	0.68	0.02	304	-
Base1 sweep V_{B2} = 1.0 V	98.505% V_C=V_{B1} =2.0 V	0.260 V_C=V_{B1} =2.0 V	1.3×10^3	0.82	0.25	251	-
Base1 sweep V_{B2} = 1.5 V	99.826% V_C=V_{B1} =2.0 V	0.809 V_C=V_{B1} =2.0 V	4.2×10^3	0.90	0.95	238	-
Base1 sweep V_{B2} = 2.0 V	99.942% V_C=V_{B1} =2.0 V	1.411 V_C=V_{B1} =2.0 V	7.9×10^3	0.92	1.76	235	7.6×10^4

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Supplementary Table 3. TCAD Simulation Quantities. Parameters and units used for TCAD simulations.

Quantity	**Value/Unit**
Device Width W	1 µm
Device Length $L_E = L_C$	1 µm
OSC_{EB1} Thickness $T_{OSC(EB1)}$	100 nm
OSC_{B1B2} Thickness $T_{OSC(B1B2)}$	60 nm
OSC_{CB2} Thickness $T_{OSC(CB2)}$	100 nm
Oxide Thickness $T_{ox1} = L_{ox1}$	5 nm
Oxide Thickness $T_{ox2} = L_{ox2}$	5 nm
Pinhole Diameter L_{Pin1}	4 nm
Pinhole Diameter L_{Pin2}	4 nm
Number of Pinholes L_{Pin1}	50 μm^{-2}
Number of Pinholes L_{Pin2}	50 μm^{-2}
Base/Emitter/Collector Thickness $T_{B/E/C}$	10 nm
Zero-Field Mobility μ_0	3 $cm^2V^{-1}s^{-1}$
Effective Density of States N_C	$1x10^{21}$ cm^{-3}
Width of the DOS Distribution σ_{DOS}	0.081eV
Energy Center E_c	0.1eV
Temperature T	300 K
Poole Frenkel Coefficient β	3
Poole Frenkel Coefficient γ	0