Design and Implementation of A New CFAR Based on Weighted and Statistical Algorithms

Gufran M. Hatem[a], Thamir R. Saeed[b]—, Jafar W. Abdul Sadahc Hadi T. Ziboon[b]

[a]*Najaf Technical College Al-Najaf Al-Ashraf, Iraq*

[b]*Digital System Design and Pattern Recognition Research Group (DSDPRG),Electrical Eng. Dept -University of Technology, Iraq*

[c]*Communications Eng. Dept- University of Baghdad, Iraq*

Abstract

In the radar system, detection represents a basic and important stage in the receiver side. The detection process is based on the thresholding criteria; two philosophies of this criteria, constant and adaptive threshold. The constant threshold is simple in design, but it has a mis-detection and does not control the false alarm rate. As for the adaptive threshold, it is powerful in target detection, and better control of the false alarm rate, where it is called Constant False Alarm Rate (CFAR). Lots of research in the CFAR design, but the gap in the previous works is that there is no CFAR algorithm can be working with all or most environmental fields and all or most target situations.

In this paper, The CFAR, which can work with the most environment and most of the target situations, has been presented. The producing the design and implementation of the new practical CFAR processor is presented. Where, the new CFAR is a combination of the properties of three different CFAR algorithm (CA, OSGO, and OSSO), and from two different families; averaging and statistical. Where it has overperformed of it's P_D is 97.25% for simulation and 96.25% for the implementable version for different target situations. The simulation analysis is made by using Matlab 2015, while the implementation is done by using Xilinx Spartan 700 3a.

Keywords*: WS-CFAR, FPGA, Radar detection.*

1-Introduction

Radar detection suffers from many problems, especially; target detection in non-homogeneous environments such as environments of closed-multiple targets. Also, when the target lies at the edge which is separating the two different clutter environments. These situations cause increased in false detection or “false alarms”. Therefore, in order to manage or control this problem, special algorithm have been utilized to preserve the **F**alse **A**larm **R**ate (**FAR**) at a constant level, such algorithm is known as **C**onstant **F**alse **A**larm **R**ate (**CFAR**).

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

So as to save the false alarm constant, a threshold level is calculated, and target detection is performed depending on this level. If a target echo passes this level, a target declaration is made, if noise or clutter return or both pass this level false alarm is occurring.

The threshold level setting of the CFAR detector should follow the background noise power that is estimated by an algorithm depends on the detection environments. Targets should be detected in different detection environments. These environments are homogenous environment (single target or multi-targets) and non-homogeneous environment (closed multi-targets or clutter edge). Corresponding to these environments various CFAR detector had been developed, namely, Cell Averaging CFAR (**CA-CFAR**) [1], Greatest Of (**GO-CFAR**) [2], Smallest Of (**SO-CFAR**), Ordered Statistic (**OS-CFAR**)[3]. In addition, the combination of different CFAR algorithms were proposed such as Trimmed Mean CFAR (**TM-CFAR**)[4], Order Statistic Greatest Of (**OSGO-CFAR**)[5], Order Statistic Smallest Of (**OSSO-CFAR**), and Variability Index CFAR (**VI-CFAR**)), fusion of different CFAR detectors such as (AND-CFAR) and (OR-CFAR) detector [6]. Also, [7] present CA-clutter map (CM-CFAR), but it affected by interfering. Then solve this problem by order statistic clutter map CFAR (OSCM-CFAR). A mean of order statistics and cell averaging" (MOSCA) CFAR was presented by [8] for Swirling II target environmental. A Forward Automatic Order Selection Ordered Statistics Detector (FAOSOSD) for an estimate the interfering target was presented by [9]. A switching CFAR (S-CFAR), is presented in [10] to operate in a homogeneous environment and multiple targets with clutter transition situations. A 2D with optimize the computational time CFAR was proposed by [11]. A combination of cell-averaging and trimmed-mean a proposed CATM-CFAR was presented by [12] to detect targets in Weibull clutter. In order to mitigate the performance degradation in non-homogeneous Weibull clutter environment, a constant false alarm rate detector based on the skewness (SK) and mean ratio (MR) named SKMR-CFAR is proposed by [13]. [14], to guarantee the continuity of detector performance with different field environments and target situations based on a neural network (NN) proposed a Closed Loop CFAR (CL-CFAR) processor.

Therefore, to fill the gap in the previous works and with a simple and inexpensive detector, this paper presents a Statistical Weighted (SW) CFAR, which is designed and implemented, with FPGA to detect the targets with different environments, which is based on the properties of their CFARs not on CFARs itself.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

2 Proposed SW CFAR

As it is known, none of the elementary CFAR detectors are the best and suitable for all detection environments (***single target, multi-targets, closed multi-targets and clutter edge***). The idea of the proposed SW CFAR is to make a combination of these elements CFAR detectors to get a detector able to operate with high performance in most of the detection environments.

2.1 Architecture of the Proposed SW CFAR

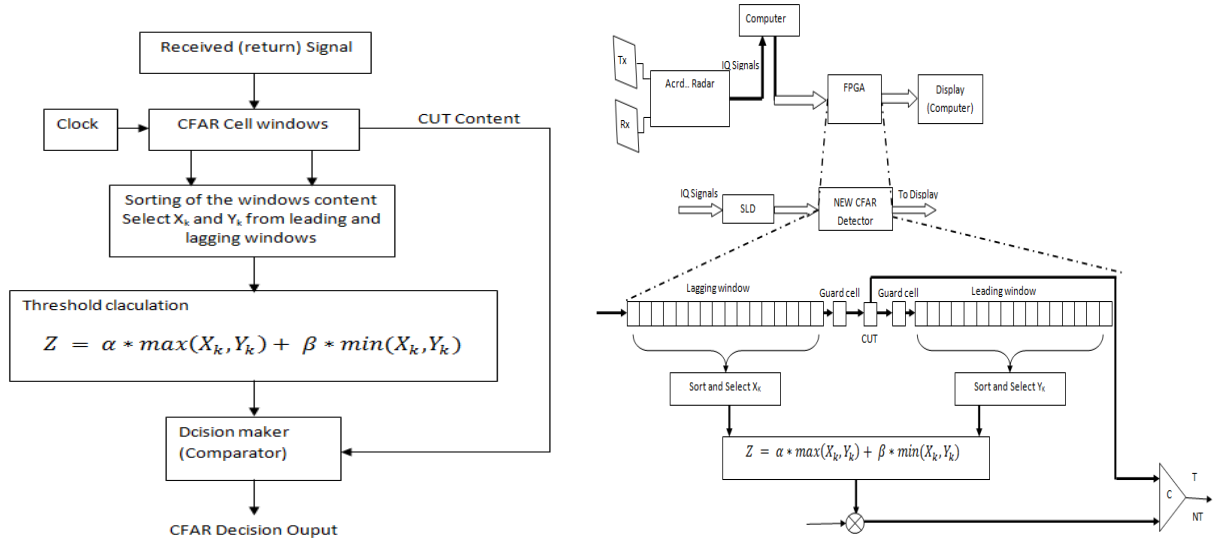
The architecture of the proposed CFAR is the combination of properties of the mean level and ordering families and as follows: the CA-CFAR and Weighted-CFAR are from mean family and OSSO-CFAR and OSGO-CFAR from statistical family.

The operation of the proposed CFAR is starting when the return signal reaches to the last cell in the leading window. Then sorting the content of the leading and the lagging windows ascending. After that, take 3/4 of the content of the windows, and apply the algorithm to the selected cells of leading and lagging windows. The threshold will be extracted after weighting it by α, β, and then the decision can be made as shown in the Fig. (**1**).

This means, that the clutter, power is estimated by applying the principle of OSGO to the leading and lagging window of SW CFAR, while, the OSSO principle was applied to the leading and lagging window over weighted them by the factor (α) and (β).

Therefore the main operations of the introduces CFAR are the sorting of windows contents and weighting of the sorting output. According to this procedure the CFAR is named **S**orting **W**eighting-CFAR (**SW-CFAR**).

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1



a- Flow chart of SW-CFAR b- Block diagram of the Proposed SW-CFAR

Fig. 1: Proposed SW-CFAR detector

2.2 Derivation of P_D and P_{fa} of SW-CFAR

The derivation is based on the consideration the received noise is distributed as Gaussian; while the envelope of detection signal is distributed as Rayleigh. Therefore, the Hypothesis testing model is derived as follows [15];

$$V = \begin{cases} f_{\circ}(v) = \frac{1}{\mu} e^{\left(-\frac{v}{\mu}\right)} & H_{\circ} \\ f_1(v) = \frac{1}{a\mu} e^{\left(-\frac{v}{a\mu}\right)} & H_1, \quad V > 0 \end{cases} \qquad 1$$

Where;

a= 1+ λ, and λ is SNR (dB).

The reference random variable x_i (i = l, . . . , n), y_j (j= 1, . . . , 2n) the reference cell is taken to be homogenous with general PDF;

$$f_x(x) = f_y(y) = \frac{1}{\mu} e^{-x/\mu} \qquad x > 0 \qquad 2$$

Their common cumulative distribution function (CDF) is evaluated as;

$$F_x(x) = F_y(y) = 1 - e^{-x/\mu} \qquad x > 0 \qquad 3$$

For CFAR detector applying the above decision rule, V and Z are independent random variables. Therefore, the detection probability of CFAR detector in homogenous background is Independent random variables V and Z are used for the CFAR detector to make decission. The probability of detection of CFAR detector in (IID) environment is;

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

$$P_d = d_z(u)|_{u=\tau/(a\mu)} \quad (4)$$

Where;

$d_z(u)$ - the moment generating function of Z. It's defined as

$$d_z(u) = \int_0^\infty \exp(-uz)\, f_z(z)\, dz \quad (5)$$

then the P_d is;

$$P_d = \int_0^\infty f_z(z)[\int_{T_z}^\infty \frac{1}{a\mu}\exp\left(-\frac{t}{a\mu}\right)dt]dz = \int_0^\infty f_z(z)\exp\left(-\frac{T_z}{a\mu}\right)dz = d_z(u)|_{u=\frac{T_z}{a\mu}} \quad (6)$$

The probability of false alarm is;

$$P_{fa} = d_z(u)|_{u=\tau/(\mu)}$$

$$P_{fa} = \int_0^\infty f_z(z)[\int_{T_z}^\infty \frac{1}{\mu}\exp\left(-\frac{t}{\mu}\right)dt]dz = \int_0^\infty f_z(z)\exp\left(-\frac{T_z}{\mu}\right)dz = d_z(u)|_{u=\frac{T_z}{\mu}} \quad (7)$$

the SW CFAR detector uses the following local estimators

$$Z1 = \alpha * max(X_k, Y_k) \quad (8)$$

$$Z2 = \beta * min(X_k, Y_k) \quad (9)$$

A general probability density function (PDF) of the SW CFAR detector is driven from the PDF of combinational CFAR detector that built from.

Therefore, to find the probability of detection and the probability of false alarm of the SW-CFAR detector we get

$$d_z(u) = [\alpha * d_{11}(u)] * [\beta * d_{22}(u)] \quad (10)$$

Where

$$d_{11}(u) = d_{osgo}(u) \quad (11)$$

$$d_{22}(u) = d_{osso}(u) \quad (12)$$

The probability of detection for SW-CFAR is;

$$P_d = \int_0^\infty f_z(z)[\int_{T_z}^\infty \frac{1}{a\mu}\exp\left(-\frac{t}{a\mu}\right)dt]dz \quad (13)$$

where;

$$f_z(z) = [\alpha * \left[M_X(u) + M_y(u)\right] * \beta[f_X(z) + f_X(z)f_y(z) - \left[M_X(u) + M_y(u)\right]]$$

$$f_z(z) = [\alpha * \left[[\frac{1}{\mu}k\binom{M}{k}(e^{-x})^{M-k+1}(1-e^{-x})^{k-1}]\,[\sum_{i=k}^{M}\binom{M}{i}[1-\exp(-y)]^i\,[\exp(-y)]^{M-1}] + [\frac{1}{\mu}\mathrm{k}\binom{\mathrm{N}}{\mathrm{k}}(\mathrm{e}^{-\mathrm{y}})^{\mathrm{N}-\mathrm{k}+1}(1-e^{-y})^{k-1}]\sum_{i=k}^{M}\binom{M}{i}[1-\exp(-x)]^i[\exp(-x)]^{M-1}\right] *$$

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

$$\beta[[\frac{1}{\mu}k(_{k}^{M})(e^{-x})^{M-k+1}(1-e^{-x})^{k-1}]+[[\frac{1}{\mu}k(_{k}^{M})(e^{-x})^{M-k+1}(1-e^{-x})^{k-1}][\frac{1}{\mu}\mathrm{k}(_{\mathrm{k}}^{\mathrm{N}})(\mathrm{e}^{-\mathrm{y}})^{\mathrm{N}-\mathrm{k}+1}(1-e^{-y})^{k-1}]]-\left[[\frac{1}{\mu}k(_{k}^{M})(e^{-x})^{M-k+1}(1-e^{-x})^{k-1}]\,[\sum_{i=k}^{M}(_{i}^{M})[1-\exp(-y)]^{i}\,[\exp(-y)]^{M-1}]+[\frac{1}{\mu}\mathrm{k}(_{\mathrm{k}}^{\mathrm{N}})(\mathrm{e}^{-\mathrm{y}})^{\mathrm{N}-\mathrm{k}+1}(1-e^{-y})^{k-1}]\sum_{i=k}^{M}(_{i}^{M})[1-\exp(-x)]^{i}[\exp(-x)]^{M-1}\right] \quad 15$$

while, the the probabilty of false alarm for SW-CFAR is;

$$P_{fa}=d_z(u)|_{u=\tau/(\mu)} \quad 16$$

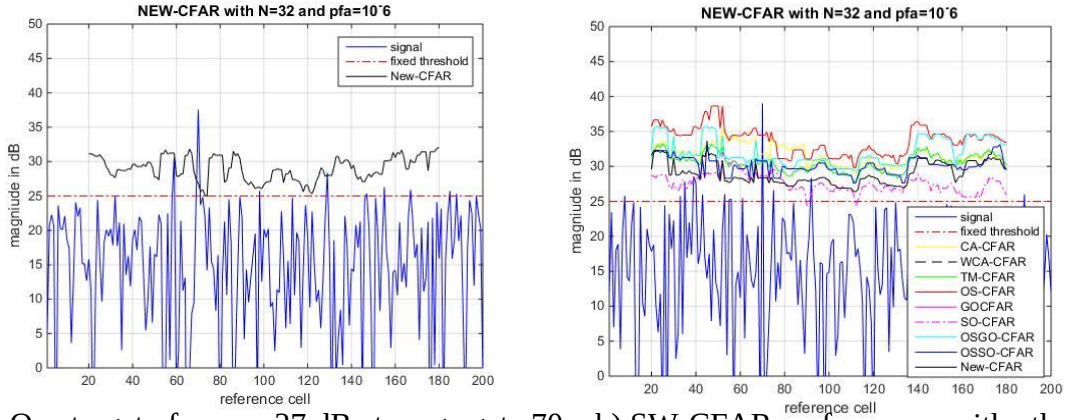
$$P_{fa}=\int_0^{\infty}f_z(z)[\int_{T_z}^{\infty}\frac{1}{\mu}\exp\left(-\frac{t}{\mu}\right)dt]dz=\int_0^{\infty}f_z(z)\exp\left(-\frac{T_z}{\mu}\right)d \quad 17$$

3-Simulation results of the Proposed SW-CFAR

The performance of the SW-CFAR processor is evaluated for the homogenous and non-homogenous environment in four target situations (single, multi-target, closed multi-target and clutter edge) separately and with other CFAR algorithms for comparison.

3.1 Single target detection

Fig.(**2**) illustrates the performance of the SW CFAR for single target detection and a comparison of its performance with other CFAR families.



a) One target of power 37 dB at range gate 70. b) SW-CFAR performance with other CFAR

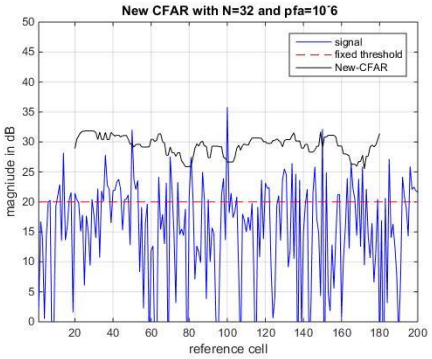
Fig. (2): SW-CFAR performance in Homogenous (single target) environment

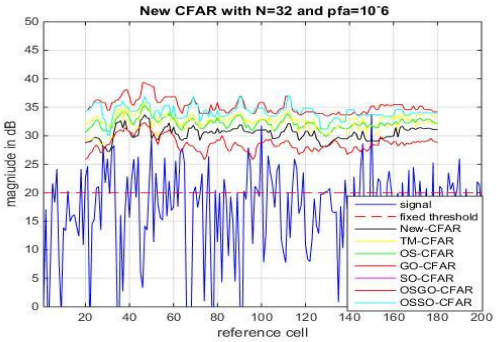
The performance of the SW CFAR is comparable to the performance of CA-CFAR and TM-CFAR. However, it is better than other CFAR families.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

3.2 Multi-targets detection

Fig.(**3**) illustrates the performance of the SW CFAR for multi- target detection and a comparison of its performance with other CFAR families.





a) Three targets of power (32, 36, and 30) dB at range gate (50, 100, and 150)

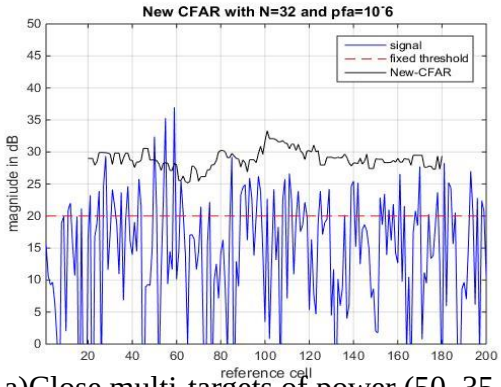
b) Multi-target environment with other CFAR

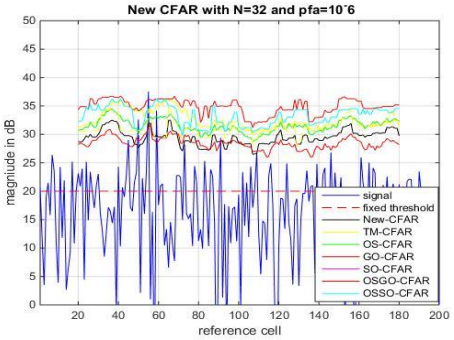
Fig. (3): SW-CFAR performance in Homogenous (multi-target) environment

As shown from Fig.(**3**), the performance of SW CFAR is very good as other family in the case of multi targets. Its performance is comparable to the performance of the OSGO-CFAR.

3.3 Closed multi-targets detection

Fig.(4) illustrates the performance of the SW CFAR for closed multi-targets detection and a comparison of its performance with other CFAR families.





a)Close multi-targets of power (50, 35, and 45) dB at range gate (50, 55, and 59)

b) closed multi target with other CFAR

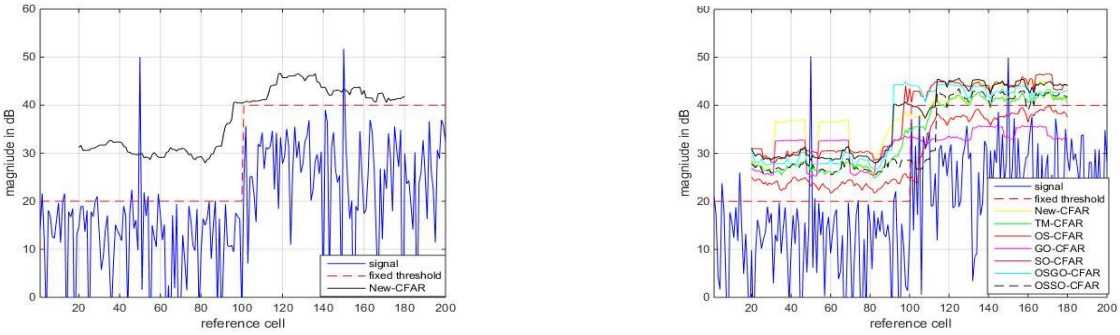
Fig. (4): SW-CFAR performance in Non-Homogenous (CMT) environment

From the previous works, it is shown that the OSSO-CFAR detector is the best for detection of closed multi-targets. However, the proposed SW CFAR has better performance for detection of closed multi-targets than OSSO-CFAR according to Fig. (**4)**

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

3.4 Target detection in clutter edge

Fig. (5) illustrates the performance of the SW CFAR for target detection in clutter edge closed and a comparison of its performance with other CFAR families.



a) CE environment two targets of power (50, 51) dB at range gate (50, and 150). b) Clutter edge with other CFAR family

Fig. (5): SW-CFAR performance in Non-Homogenous Clutter edge (CE) environment

Fig. (5) show that the SW-CFAR has a comparable performance to OSSO CFAR for target detection in clutter edge**.**

3.5 The probability of detection of SW-CFAR

Figure (**6**) illustrates the probability of detection of SW – CFAR detector and other CFAR detectors against signal to noise ratio for window size 32 and the probability of false alarm equal to 10^{-6}. The result indicated that the SW-CFAR has a highest P_d compared with other CFAR detectors.

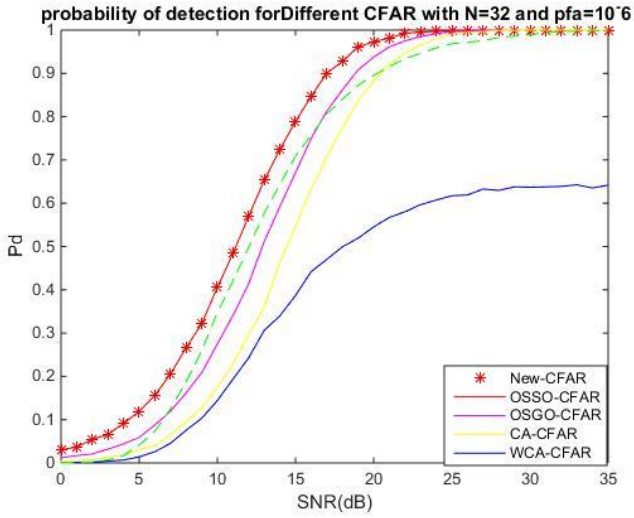
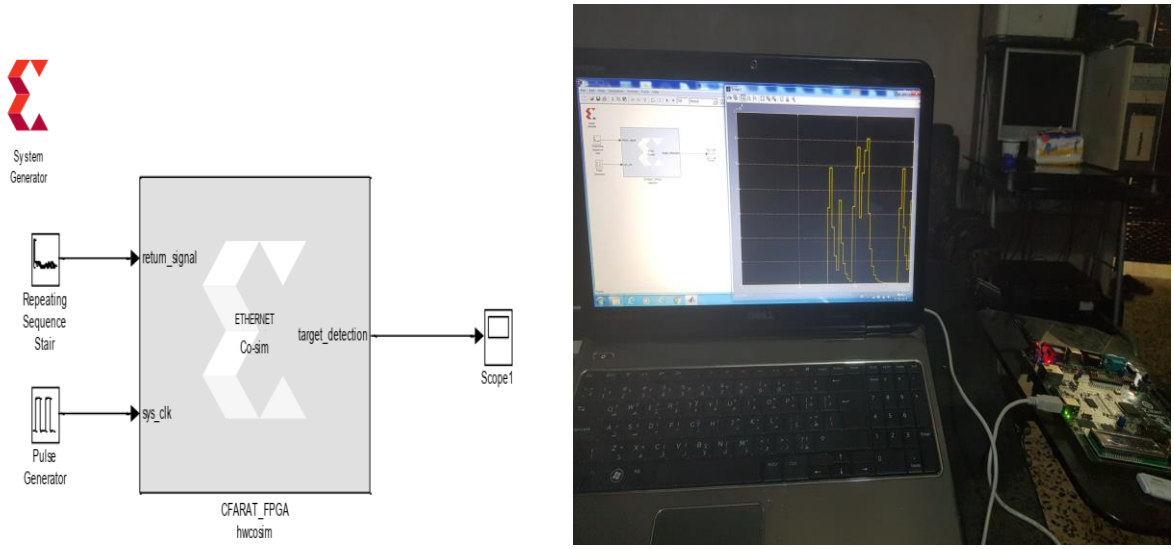


Fig.(6) Probability of detection (P_d) vs Signal to noise ratio (SNR) for different CFAR detectors

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

4-Hardware Implementation of the Proposed SW-CFAR

According to the suggested SW-CFAR results that has the best performance, the FPGA design of this CFAR is built as shown in Fig. (**7-a**) and the implements in Fig. (7-b).



a) FPGA system generator of proposed SW-CFAR

b) Proposed SW-CFAR in FPGA kit.

Fig.(7) Proposed New SW-CFAR

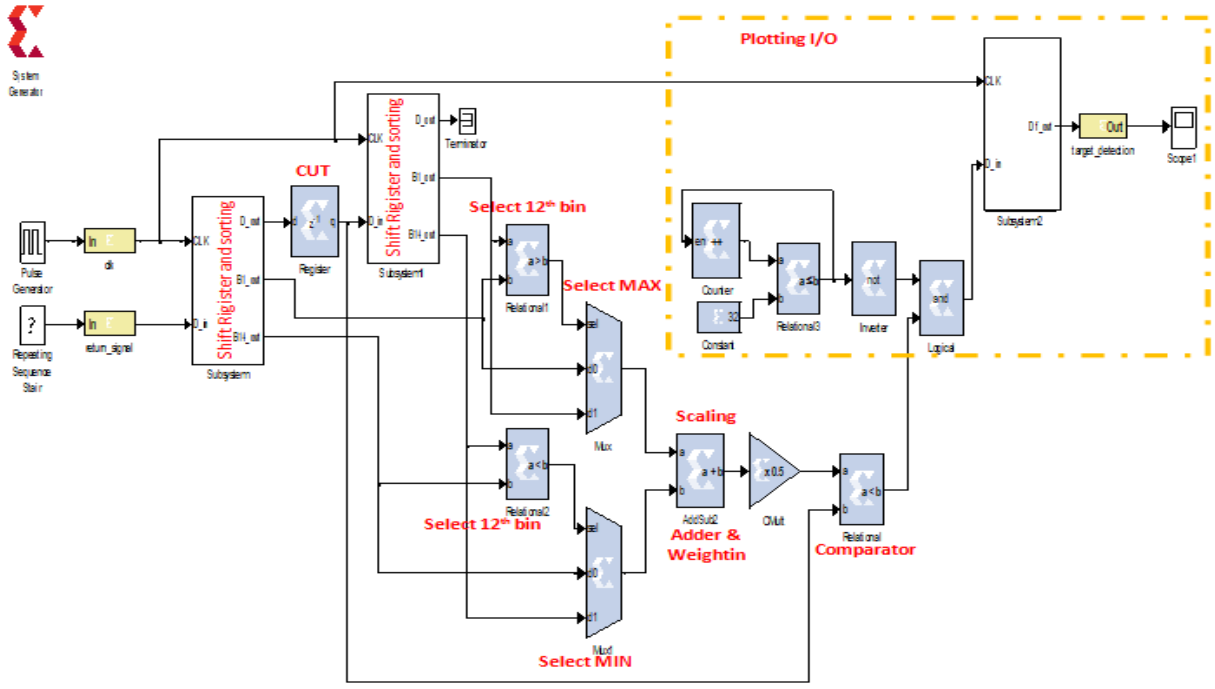


Fig. (8) FPGA block diagram of the Proposed New SW-CFAR

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

Related to Fig. (8) of the SW-CFAR FPGA block diagram, it has content subsystems can implement in FPGA. Each subsystem achieves a specific task. VHDL model creates the shift register and sorting subsystem using Xilinx ISE 14.6., while, the rest subsystems are occur as a function block in Xilinx System Generator block sets set up in MATLAB-Simulink. The file sources of The VHDL that generated in ISE are transferred via black box block to System Generator and the simulation is done by MATLAB-Simulink related with "XGS".

The hardware platform used to implement the proposed SW-CFAR is Spartan-3A DSP 3400A. Corresponding to available hardware characteristics, there are several limitations in FPGA design, these are;

1. The treatment received signals length at each clock is 33 symbols, where sixteen symbols for each window (leading and lagging) and one symbol for CUT.
2. The number of bits that represent the symbol is 8 bits. Also, a fixed-point precision of 8 bits.

4.1 FPGA implementation of subsystems

There are many subsystems implemented by FPGA, these are;

1- Shift register and sorting:

The received signal is generated in the computer by Matlab, and then entered to the FPGA. The first subsystem is the shift register and sorting. The signal will be shifted to the leading window through the CUT cell and lagging window. After that, the content of leading and lagging window will be sorted in ascending order individually. Fig. (9) shows this subsystem.

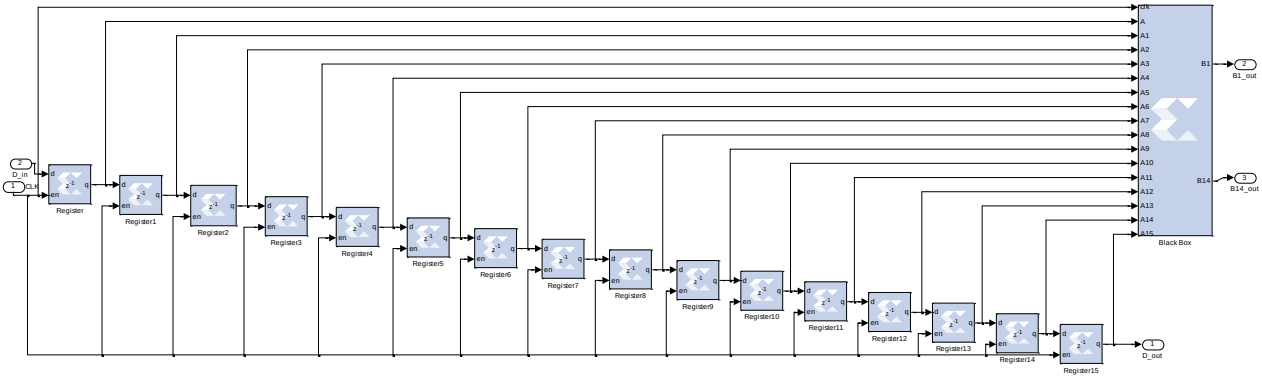


Fig. (9) Shift register and sorting subsystem

To sort the input signal by ascending rank without employing RAM, the online sorting method is suggested for implementing this procedure. This process is utilized to give a greater

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

12th bins that using to calculate maximum and minimum values. This proposed process relies based on comparison among the pre-saved sixteen points and SW point sequence. All pre-saved point values are initially zero. When the SW point appears, it is compared to the large value of pre-saved point, if the SW point is larger than the value of largest point, the largest value of per-saved point will be substituted by the SW point value with other whole pre-saved points with values smaller than the replacement point will be updated. Otherwise, if the SW point value is less than the greatest point value, the greatest point will become out of the comparison, and procedure of preceding comparison will occur with the next value of pre-saved point, etc.

2- Select the 12th bin subsystem.

The proposed design is based on select 3/4 of the windows, this means 12 bins. In the sorting ascending process means, the maximum is bin 12. Therefore, this subsystem selects the bin 12 from leading and lagging windows.

3- Select MAX and MIN subsystem.

These subsystems select the maximum and minimum values between the two maximum and minimum from the sorting, leading and lagging (bins 12th).

4- Adder and weighting subsystem

This subsystem is used for weighting by (0.5 and 0.75) which represented alpha and beta weighted factors respectively, then add the results of the above subsystems.

5- Scaling subsystem

0.5 (scaling factor) multiplies the weighting result.

6- Plotting I/O subsystem

This subsystem is content many blocks to plot the input and output of the proposed CFAR.

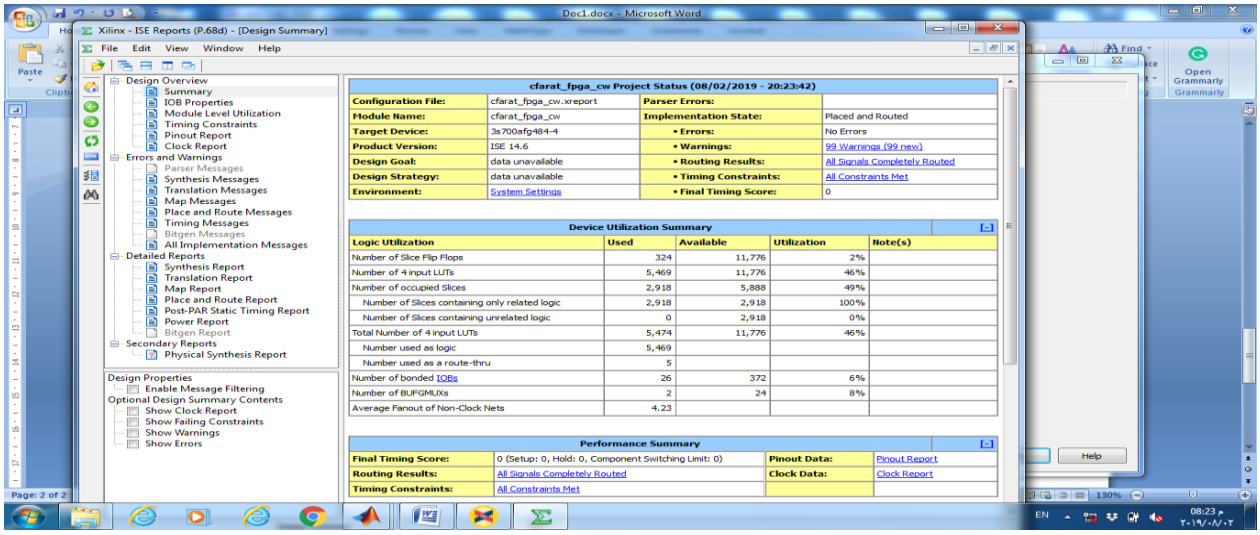
4.2 Hardware Implementation of the proposed SW-CFAR on Spartan-3A DSP 3400A Platform

There are four steps to complete the design flow of FPGA; 'design entry', 'design synthesis', 'design implementation', and 'Xilinx device programming'. The buildings of the suggested scheme, including the written of its VHDL files and use a block from the library are done in a first step. Code of VHDL and block are syntax checks and the design hierarchy study is done in a second step to enhance the proposed design scheme for FPGA architecture. The third step is accountable for linking input netlists and bonds within design file by 'Translate' process, fit the design system to FPGA hardware device’s resources through 'Map' process. Finally, place and route the design

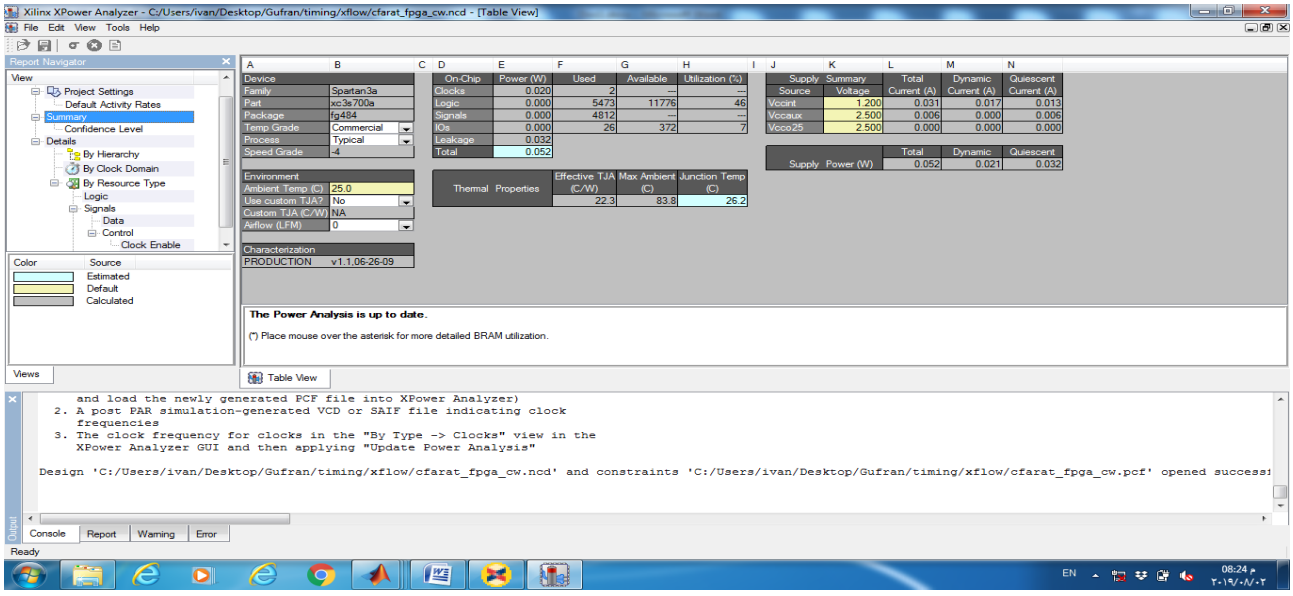
Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

system within the timing bonds by 'Place and Route' process. The final step creates the bitstream file to the design system so as in order to download to the FPGA platform.

More of the limitations of suggested design relate to the inadequate Xilinx device's presented resources that were checked and operated in the map process. The Map process of SW-CFAR and overview of the design of line are presented in Fig. (10).



a) The device utilization summary SW-CFAR system.



b) The power consumed in the FPGA kit

Fig. (10) The Map process of SW-CFAR and overview of the design.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

After the design system passes over the four FPGA design flow steps effectively, a bit stream file of a SW-CFAR can be generated in order to download into the hardware device in order to construct the this platform to suit the required design system. Numerous packages are used for downloading bit stream file through the FPGA platform; one of these packages is the Xilinx ISE 14.6 which utilizes ' Configure a Target Device' method to transmit this file to the FPGA device through Ethernet cable. Other packages such as MATLAB using the system generator hardware co-simulator to construct the hardware device and directly combine the suggested design running in the FPGA-HW to a simulation of MATLAB-Simulink. It is therefore very helpful in this thesis to use the hardware Co-Simulation, as it is essential to simulate the desired platform by transmitting the modulation signal to the device in relation to the bit stream file and collecting the results.

The hardware platform interface is either Ethernet cable or JTAG, this depends on the accessibility of those cables. In this paper, the Ethernet cable with point-to-point link is utilized to construct the SW-CFAR on FPGA platform. Fig. (7) shows this connection. An Ethernet cable provides a high throughput link with the FPGA platform and present best bandwidth when used in the applications of real life.

The host computer connects with the Spartan-3A DSP 3400A board in order to implement the SW-CFAR detector, figure (7) shows this action.

4.3 SW-CFAR Hardware Result

The similar conditions, which have processed in simulation for measuring the detection performance of SW-CFAR proposed, are processed to estimate the hardware implementation success rate. The return signal is generated by using MATLAB and it is sent by Ethernet cable to the FPGA device. Distinct levels from (5 dB to -5 dB) of AWGN were added to The generated signals . Each tested signal contains of 33 (32 for leading and lagging window and one for CUT) symbols generated randomly and repeated many times in the screen window for different target's situation and locations. Each figures from (11) to (15) consists of three parts ; the first part represents the received signal and adaptive threshold, while the second part shows the decision results and the third art appears the clock pulse, which the process begins and continues with it. For all the Figs of all target's situation, the first figure, it is clear the beginning of the process to create the threshold is not correct, because of the leading window of the CFAR is filled by zero

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

values and not real values. Therefore, the created adaptive threshold is not correct, then the decision is an error. For this reason, the decision process is beginning after the leading window is full by the received signal.

Single Target

Three cases for single target are considered, each one with different locations. One of these cases is shown in Fig. (11), which the target is located at bin 13. It is clear from the Fig. (11-a) of that the adaptive threshold follows the change in cells value. Also, from the Fig. (11-b) the decision is correctly at the location of the target at bin13.

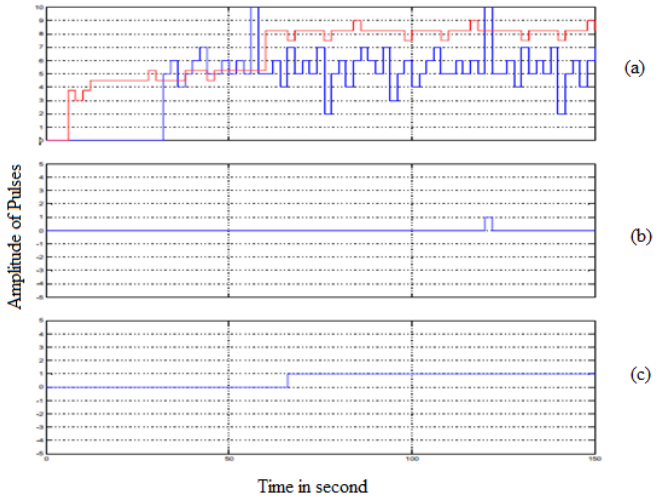


Fig.(11) detection and decision of SW-CFAR detector for ST at bin 13

(a) Signal with threshold (b) decision (c) clock pulse

In the second case, a single target is considered at bin 2. The target is detected at bin 2 and two false alarms at bin 3 & 4. In this context, in the third case, a single target is considered at bin 17 In all cases the detector is take a correct decision at the target locations.

Multi- targets

In the first experiment of multi-target detection, three targets are considered at bins 13, 23 & 32 as in Fig.(12). From the second part of the Fig. (12), it is clear the overperfom of the SW CFAR and the three targets are detected at cottect locations.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

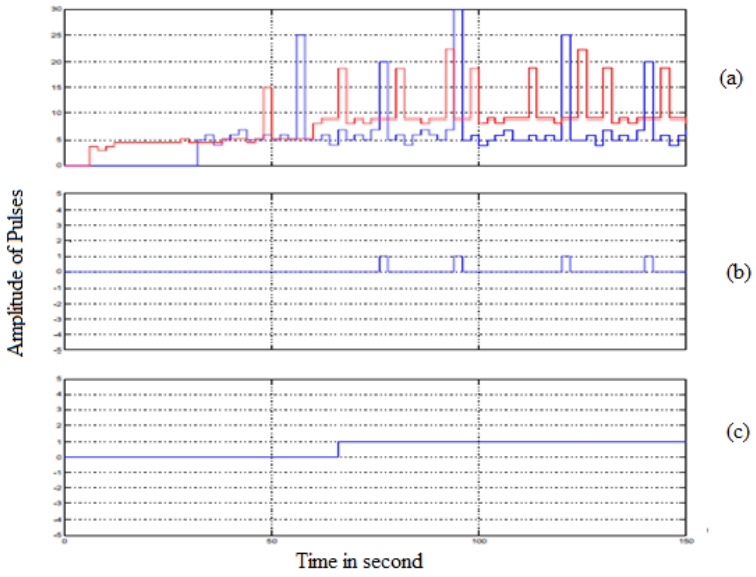


Fig. (12) detection and decision of SW-CFAR detector for Multi-target at bins 13, 23,32. (a) Signal with threshold (b) decision (c) clock pulse

A second experiment for multi-target detection, with other three targets at bins 2, 21 & 29. The correct decision is the proof of preference of the SW-CFAR algorithm. To make sure more, the other scenario of multi-targets are shown in Fig. (13). The importance of this scenario is coming from the values of these targets, there are many targets that have a low amplitude. In spite of that, the threshold creation process is good and the detection and decision processes appear clearly. The target location of this scenario is at, bins 3,9,22,31. The detection results are shown in Fig. (13) at bins 3, 9, 22 & 31. The importance of this experiment comes from the facts that the return signals from these targets are weak and they are four targets. Again, the four targets are detected in correct locations without any false alarm which indicates that the threshold process and the detection of the SW CFAR operate very well.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

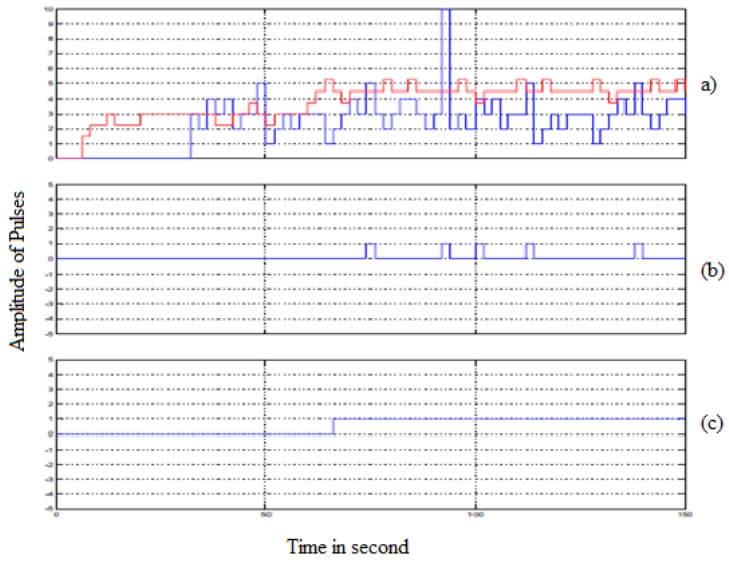


Fig. (13) detection and decision of SW-CFAR detector for Multi-target at bins 3,9,22,31. (a) Signal with threshold (b) decision (c) clock puls

Close Multi- Targets

The first experiment for closed multi-targets is shown in Fig.(14) where the targets at bins 3,6,8.The second part of Fig.(14) shows that these targets are detected in correct locations.

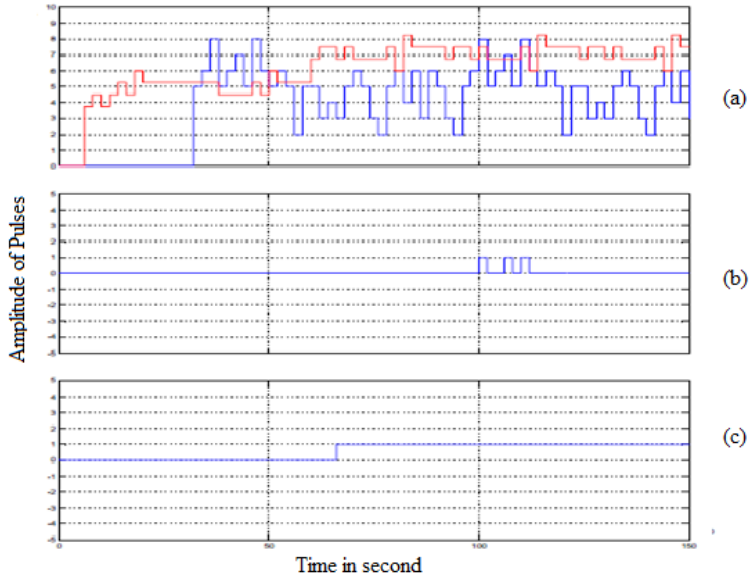


Fig. (14) detection and decision of SW-CFAR detector for Close Multi-target at bins 3,6,8. a) Signal with threshold (b) decision (c) clock pulse

The second experiment of closed multi-targets with target locations are at bins 10,12,15. The three closed targets are detected, however, a false alarm is appeared in bin 13. The third scenario in close

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

multi-targets considered the target location at the end of the stream, at the location bins 26,29,31. The decision Figure tells the accurate detection and decision, that means the overperform of the SW-CFAR.

Clutter edge

Target detection in clutter edge is one of the important situation of the real detection environment. Three experiments are done to examine the performance of the SW CFAR in the clutter edge environment. In the first experiment, the clutter is in bins 1,2,3,5,6, while the target at bin 4 as shown in Fig. (15).

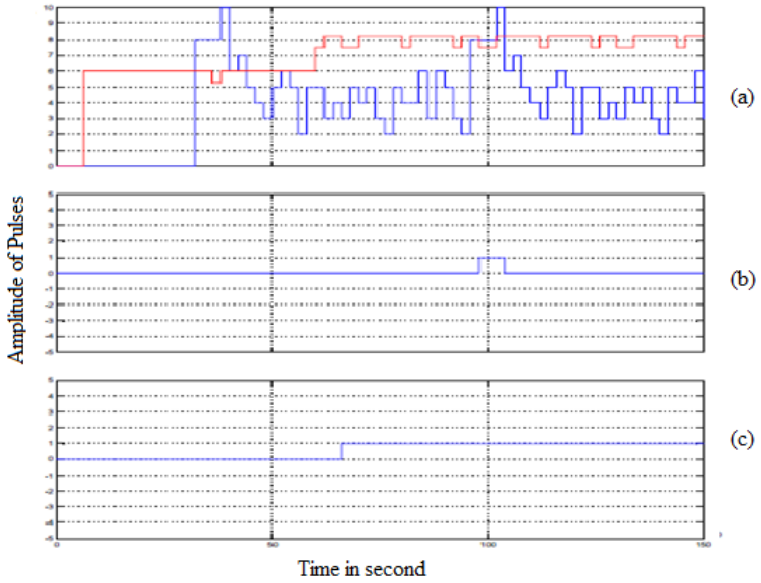


Fig. (15) detection and decision of SW-CFAR detector for Clutter edge target, clutter edge at bins 1,2,3,5,6, and target at bin 4. (a) Signal with threshold (b) decision (c) clock puls

The second experiment for clutter edge detection in which the clutter at the mid of the window at bins 10,11,12, 15,16,17 and the target at bin 14. The location of the clutter edge at the end of the window is tested in the third experiment for clutter edge detection. The clutter is at bins 25,26,29,30,31,32, and the target is in the bin 28. The results are showing a good detection process. From the clutter edge testing, there is an error appeared at the beginning and the end of the edge, where the CFAR detect it as a target while it is a false alarm. In this context can be negligent the edge of detection, and if the detection appears in the middle of the edge clutter this means a real target

The summarization of the results of the SW-CFAR are presented in Table (1), where this table appears the probability of detection of many algorithms and the SW-CFAR for comparison.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

Table (1) illustrates the probability of detection of the five CFAR techniques and the fixed threshold technique and the proposed SW-CFAR. Two important points can be illustrated from this table of the SW-CFAR, these are;

- The first point is that the advancement of the detection in simulation and implementation with an acceptable probability of detection.
- While the second point is that the SW-CFAR does not fluctuate in detection with different target situations. Conversely are the other CFAR algorithms.

Table (1) Probability of detection of SW-CFAR (simulation and Hardware) with other CFAR algorithms for 10^{-6} and N=32

Probability of detection for different Target Situations		Single Target %	Multi-Target %	Close Multi-Target %	Clutter Edge %	Average Detection %
CFAR Types						
CA		93	96	76	88	88.25
GO		91	98	83	90	90.5
OS		93	96	93	91	93.25
SO		92	100	92	87	92.75
OSGO		93	100	96	91	95
OSSO		92	96	96	92	94
TM		99	99	94	88	95
SW-CFAR	**Simulation**	100	96	99	94	97.25
	Hardware	95	100	95	95	96.25
Fix Threshold		Low	Low	Low	Low	Low

5- Conclusion

The CFAR is a technique being used in detection process stage to keep the false alarm at an acceptable level. There are many CFAR algorithms that can be used, each one is used with certain environment, while no CFAR can work in all environments. The received signal properties is changed according to the situations of the detected targets. There are four target situations;

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 26 March 2020 doi:10.20944/preprints202003.0397.v1

Single, multi-target, close multi-targets, and targets with clutter edge. There is a suitable CFAR algorithm with each target's situation, but, this CFAR is a degradation with other target's situations.

Therefore, the real problem is, the target needs to be detected is always in motion, then it's situation is changed. Therefore, the CFAR which can be operated with all target situations or with most of it must be built.

Accordingly, this paper presents a SW-CFAR algorithm; which enhance the detection of the radar system to solve the above problem.

From the evaluation and simulation the proposed new SW-CFAR many concluded points, where the combination of the CFAR properties outperforms the combination of the CFAR nether it is families as in the proposed CFAR processor. Where, this CFAR offers a good performance in all radar environments compared with other detectors, with less complexity in FPGA implementation and the highest probability of detection. In this context, the average $\boldsymbol{P_D}$ which has gained 97.25% with a range of (P_{fa}) from 10^{-4} to 10^{-6} for simulation and 96.25% with same range of (P_{fa}) for FPGA implementation. Also, the advantages of the NEW-CFAR over the other are the advancement of the probability of detection by 2.3% with the nearest one (TH) and it has no fluctuation in the probability of detection with different target situations. The probability of detection of the NEW-CFAR is less than the probability of detection of [H] by 0.75%. This reduction in probability of detection is considered acceptable against the reduction in complexity in the NEW-CFAR against it.

Based on the obtained results in this paper, several points have been noticed to be trying to satisfy the goal as a future work. These points; Other CFAR (properties) combination may give over performance in detection. Also, can Built the CFAR processor by using NN in optimal with all environments and all target situations. To enhance the detection performance, can design a CFAR based on frequency Doppler signature. Implement the proposed CFAR with another version of FPGA kits or TMS for improving their performance according to the speed and complexity.

References

1. P. Antonik, B. Bowies, G. Capraro, and L. Hennington. Intelligent Use of CFAR. Kaman Sciences Corporation, USA, 1991.
2. G.V. Hansen and J.H. Sawyers. Detectability loss due to greatestof selection in a cell averaging CFAR. IEEE Transactions on Aerospace & Electronic Systems, 16:115-118, 1980.
3. G.V. Trunk. Range resolution of targets using automatic detectors.IEEE Transactions on Aerospace & Electronic Systems, 14 (5): 750-755, September, 1978.
4. P.P. Gandhi and S.A. Kassam. Analysis of CFAR processors in non-homogeneous background. IEEE Transactions on Aerospace& Electronic Systems, 24(4):427-445, July, 1988
5. M.E. Smith and P.K. Varshney. Intelligent CFAR processor based on data variability. IEEE Transactions-on Aerospace & Electronic Systems, 36(3):837-847, July, 2000.
6. T. V. Cao, "A CFAR Thresholding Approach Based on Test Cell Statistics", Proc. IEEE Radar Conf., Philadelphia, USA, pp.349-354, April 2004.
7. Tao Shan, Ran Tao, Yue Wang, and Siyong Zhou, "Performance of order statistic clutter map CFAR", IEEE Conferences, 6th International Conference on Signal Processing, Pag.: 1572 - 1575 vol.2, 2002.
8. He You, Guan Jian, Peng Yingning, and Lu Dajin, "A new CFAR detector based on ordered statistics and cell averaging", IEEE Proceedings of International Radar Conference, Pag.: 106 - 108, 1996.
9. B. Magaz, A. Belouchrani, and M. Hamadouche, "AUTOMATIC THRESHOLD SELECTION IN OS-CFAR RADAR DETECTION USING INFORMATION THEORETIC CRITERIA", Progress In Electromagnetics Research B, Vol. 30, 157-175, 2011.
10. Tri-Tan Van Cao, "A CFAR Thresholding Approach Based on Test Cell Statistics", IEEE, 2004.
11. Gerardo G. Acosta, and Sebastián A. Villar, " Accumulated CA–CFAR Process in 2-D for Online Object Detection From Sidescan Sonar Data", IEEE JOURNAL OF OCEANIC ENGINEERING, VOL. 40, NO. 3, JULY 2015.
12. Dejan Ivković*, Milenko Andrić and Bojan Zrnić, "A New Model of CFAR Detector", Frequenz; 68(3 – 4): 125 – 136, 2014.
13. Xin Zhang ; Renli Zhang ; Weixing Sheng ; Xiaofeng Ma ; Yubing Han ; Jie Cui ; Fan Kong, "Intelligent CFAR detector for non-homogeneous weibull clutter environment based on skewness", IEEE Radar Conference (RadarConf18), Oklahoma City, OK, USA, Page s: 0322 - 0326, 23-27 April 2018.
14. G. M. Hatem, J. W. Abdul Sadah, J. Salman and T. R. Saeed, "Improve CFAR Algorithm Based on Closed Loop by Neural Network," 2019 4th Scientific International Conference Najaf (SICN), Al-Najef, Iraq, 2019, pp. 15-19.
15. J. Salo, H. M. El-Sallabi and P. Vainikainen, "The distribution of the product of independent Rayleigh random variables," in IEEE Transactions on Antennas and Propagation, vol. 54, no. 2, pp. 639-643, Feb. 2006.