Article

Electrical Characteristics and Reliability of Nitrogen-Stuffed Porous Low-*k* SiOCH/ Mn$_2$O$_{3-x}$N/Cu Integration

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Abstract: In our previous study, a novel barrier processing on a porous low-dielectric constant (low-*k*) film was developed: an ultrathin Mn oxide on a nitrogen-stuffed porous carbon-doped organosilica film (p-SiOCH(N)) as a barrier of the Cu film was fabricated. To form a better barrier Mn$_2$O$_{3-x}$N film, an additional annealing at 450°C was implemented. In this study, the electrical characteristics and reliability of this integrated Cu/Mn$_2$O$_{3-x}$N/p-SiOCH(N)/Si structure is investigated. The proposed Cu/Mn$_2$O$_{3-x}$N/p-SiOCH(N)/Si capacitors exhibited poor dielectric breakdown characteristics in the as-fabricted stage, although, less degradation was found after thermal stress. Moreover, its time-dependence-dielectric-breakdown electric-field acceleration factor slightly increased after thermal stress, leading to a larger dielectric lifetime in a low electric-field as compared to other MIS capacitors. Furthermore, its Cu barrier ability under electrical or thermal stress was improved. As a consequent, the proposed Cu/Mn$_2$O$_{3-x}$N/p-SiCOH(N) scheme is a promising integrity for back-end-of-line interconnects.

Keywords: Porous low-dielectric-constant; Barrier; MnO$_x$; Electrical characteristics; Reliability; Electric-field acceleration factor; TDDB.

1. Introduction

Copper (Cu) conductor and porous low-dielectric-constant (low-*k*) dielectric insulator have been used as back-end-of-line (BEOL) interconnect materials, accelerating the high-speed requirement for advanced microelectronic devices by the reduction of resistance-capacitance (RC) time delay [1-3]. However, due to the intrinsically structural and bonding weakness of porous dielectric materials, their integration with Cu is a challenging topic.

Poor adhesion and high diffusivity of Cu are the critical issues, causing integration difficulty of Cu and porous low-*k* dielectric materials [4,5]. Hence, a liner/barrier is interposed between Cu line and porous dielectric insulator. Currently, a dual layer of Ta/TaN liner/barrier is used by industry communities [6-8]. With the progress of advanced technological nodes, the dimensions of BEOL interconnects are continuously scaling down, and the associated thickness-thinning for Ta/TaN dual layer results in its failure to maintain effective barrier performance against Cu diffusion. Under such a scenario, Ta/TaN dual layer typically deposited by sputtering deposition, occupies a larger portion of Cu line volume, leading to a huge increase in overall resistivity of lines and vias, as well as a poor step coverage of trenches and vias [9].

Therefore, an alternative to replace the currently used Ta/TaN barrier materials and process for the aggressively scaled-down interconnects is required to overcome the above mentioned issues, among which self-forming barrier process, chemical vapor deposition (CVD), and atomic layer deposition (ALD) technologies have been proposed [10-12]. Moreover, manganese (Mn), ruthenium

(Ru), and cobalt (Co), along with their derivatives, are considered as potential alternative barrier materials to substitute Ta/TaN dual layer [13-15].

In light of the aforementioned studies of metal-based barriers, we have recently proposed a novel barrier process for Cu metallization [16] by firstly performing high-pressure nitrogen stuffing of a porous low-*k* SiOCH dielectric. Then, a 2-nm-thick Mn oxide film was deposited in a controlled (oxygen-containing) sputtering gas. Subsequently, an Ar/H_2 forming-gas treatment was performed on the MnO$_x$/porous SiOCH stacked layer to enhance its thermal stability. Such a thermal stabilization treatment results in the transformation of Mn_2O_3 and its reaction with stuffed gaseous, ultimately forming an effective ultrathin barrier denoted as $Mn_2O_{3-x}N$.

This proposed barrier process is an effective barrier against Cu diffusion under thermal stress. However, its impact on the electrical characteristics and reliability of the porous low-*k* SiOCH dielectric remains unclear. Therefore, the purpose of this study is to investigate this topic in details. The barrier capacities under thermal and electrical stresses for the proposed barrier process are also evaluated.

2. Experiments

The low dielectric-constant (*k*) material used in this study was porous SiOCH (abbreviated hereafter as p-SiOCH), which was deposited on a *p*-type (100) Si wafer by an Applied Materials plasma-enhanced chemical vapor deposition system using diethoxymethylsilane (DEMS), oxygen (O_2), and alpha-terpinene (ATRP) porogen as precursors [17]. The thickness and *k* value of p-SiOCH dielectric films were ~100 nm and 2.560, respectively.

First, a p-SiOCH sample was placed into a vacuum furnace evacuated by a scroll pump to background pressure of approximately 1 Pa. The p-SiOCH film was then stuffed at 450°C for 5 min under 4 atm of surrounding nitrogen, hereafter denoted as p-SiOCH(N). Subsequently, a 2-nm-thick layer of Mn_2O_3 was deposited onto p-SiOCH(N) through a shadow mask by sputtering a Mn target under a controlled Ar/O_2 oxidative atmosphere. The resultant sample, denoted as Mn_2O_3/p-SiOCH(N)/Si, was subjected to stabilization annealing at 450°C in an Ar/H_2 (5%) forming gas for 60 min, converting the Mn_2O_3 to $Mn_2O_{3-x}N$ [16]. Finally, a 50-nm-thick Cu film was thermally evaporated onto the stacked sample also through a shadow mask. The area of the formation Cu electrode was 9.0 x 10^{-4} cm^2. Based on this process flow, metal-insulator-silicon (MIS) capacitors with a Cu/$Mn_2O_{3-x}N$/p-SiOCH(N)/Si stacked structure were fabricated for electrical characteristics and reliability measurements. Other MIS capacitors with Cu/p-SiOCH/Si and Cu/Mn_2O_3/p-SiOCH/Si stacked structures were also fabricated for a reference.

C-V plots of dielectric films were measured by a semiconductor parameter analyzer (HP4280A), using applied voltages in the range from -40 V to 40 V and -40 V and an operation frequency of 1 MHz. The *k* value of each dielectric film was derived from the measured accumulation capacitance value (*C*) of the associated *C-V* plots, along with the values of Cu electrode area (A) and thickness (*d*) of the dielectric film, using the equation: $C=\varepsilon_0 k A/d$, where ε_0 is absolute capacitivity in vacuum (8.85 x 10^{-12} F/m). Furthermore, leakage currents of a dielectric film were measured versus applied voltages by a ramped-voltage-stress (RVS) method with a ramping rate of 0.1 V/s, from which a breakdown field was derived. Dielectric breakdown time was detected from time-dependent-dielectric-breakdown (TDDB) measurements by applying a constant electric voltage (field). RVS and TDDB tests were performed by an electrometer (Keithley, 6517A). All measurements were performed at room temperature (25°C). Electrical aspect of diffusion barrier properties for Cu/$Mn_2O_{3-x}N$/p-SiOCH(N)/Si structure was evaluated by thermal stress at 450°C for 2 h and electrical stress at 1.5-3.0 MV/cm

3. Results and Discussion

By recording the plots of relative changes of sheet resistance [$(R_T-R_0)/R_0$)] versus annealing temperatures (250-650°C) for three representative samples, as shown in Figure 1, the effectiveness of Mn_2O_3 and $Mn_2O_{3-x}N$ layers as barriers of Cu can be evaluated from comparing the values of temperature corresponding to the onsets of abrupt rise in relative resistance. Notably, R_0 is the sheet

96   resistance of a pristine stacked samples covered by a continuous Cu film, which is thus equalent to
97   the sheet resistance of the Cu conducting film,   while R_T is the sheet resistance of the same sample
98   after annealing. Thermal annealing tends to cause Cu to agglomerate and/or penetrate the manganese
99   oxide barrier into the underlying p-SiOCH films [18], leading to failure of the metallized layers.
100 Therefore, the values of $(R_T-R_0)/R_0$ reflect the integration of the Cu layers, and thus the magnitude of
101 threshold temperatures serves to provide capacity of barrier layers. According to Fig. 1, the threshold
102 temperatures for Cu/p-SiOCH (barrier-free) samples and identical samples interposed with a Mn_2O_3
103 or $Mn_2O_{3-x}N$ barriers are 450°C, 550°C, >550°C, respectively. Notably, the limit of temperature for
104 BEOL interconnect processing is around 400°C. Therefore, the slight increase in $(R_T-R_0)/R_0$ at the
105 threshold temperature (400 °C) for Cu/p-SiOCH indicates the necessity of a barrier. Comparing the
106 magnitudes of threshold temperature in Fig. 1 also suggests that $Mn_2O_{3-x}N$ outperforms Mn_2O_3; it
107 exhibits an outstanding barrier capacity with a significantly higher threshold temperature (650°C
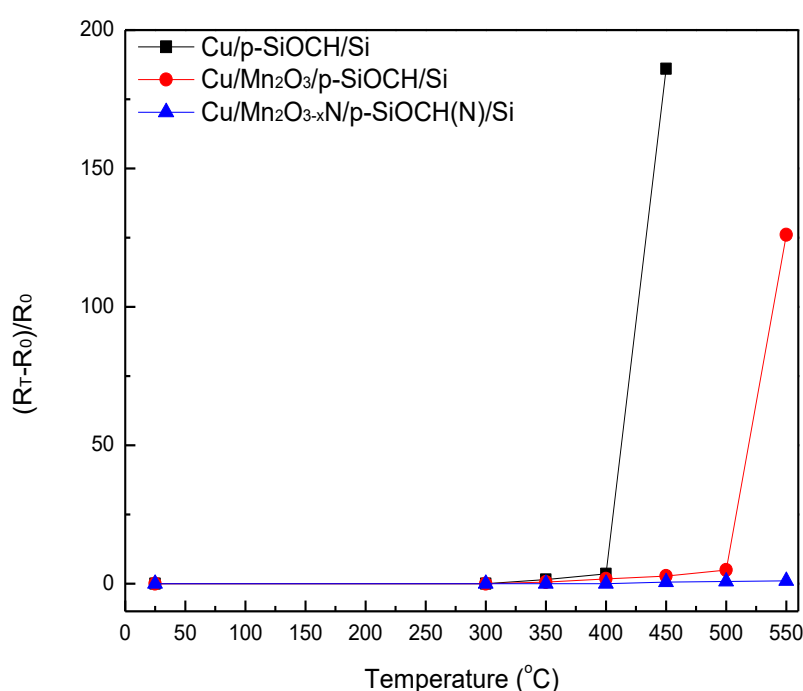108 versus 550 °C), even with a thickness of only 2 nm.

109

110 **Figure 1.** Variation of relative electrical resistivity as a function of annealing temperature for various
111 Cu-gate MIS capacitors.

112   Table 1 lists the results of tape testing of the as-deposited and annealed (450 °C for 2 h) samples,
113 including Cu/p-SiOCH/Si, Cu/Mn_2O_3/p-SiOCH(N)/Si, and Cu/$Mn2O_{3-x}N$/p-SiOCH(N)/Si. The size of
114 the tested sample films was 6 x 6 square regions. For the pristine and annealed (barrier-free) Cu/p-
115 SiOCH/Si samples, no square or only a few square regions were left after tape testing, indicating
116 delamination of Cu films due to poor adhesion. For the pristine Cu/Mn_2O_3/p-SiOCH(N)/Si samples,
117 about 20 % square regions were delaminated. After annealing, the delamination percentage was
118 slightly increased to approximately 35%, indicating that thermal annealing degrades the interfacial
119 adhesion. On the contrary, all the 36 square regions in the Cu/$Mn_2O_{3-x}N$/p-SiOCH(N)/Si samples
120 remained intact before and after annealing, indicating that, apart from acting as a barrier, the 2 nm-
121 thick $Mn_2O_{3-x}N$ layer serves as adhesion promoter, thus markedly increasing adhesion of Cu films.
122 The significant enhancement of interfacial adhesion by $Mn_2O_{3-x}N$ is attributed to a chemical
123 interaction between contacted layers and the resulting nitrogen-related bonding between Cu metal
124 electrode and p-SiOCH substrate. The obtained result is similar to the reported finding by Selvaraju

125   et al., indicating that a noticeable improvement in adhesion of Cu to the underlying SiO_2 was
126   observed by the use of Mn-nitride with a nitrogen content of just 5% [19].

127   **Table I: Tape test results of various MIS capacitors before and after annealing.**

	Cu/p-SiOCH/Si	Cu/Mn$_2$O$_3$/p-SiOCH/Si	Cu/Mn$_2$O$_{3-x}$N/p-SiOCH(N)/Si
As dep.	Fail	~ 20 % Fail	Pass
450°C/2 h	N/A	~ 35 % Fail	Pass

128

129   It is important for the underlying p-SiOCH layers to keep a low-*k* feature after completing the
130   fabrication of the Cu/Mn$_2$O$_{3-x}$N/p-SiOCH(N)/Si structure, involving nitrogen stuffing, Mn$_2$O$_3$
131   deposition, stabilization annealing [converting Mn$_2$O$_3$ to Mn$_2$O$_{3-x}$N], Cu deposition. Therefore, the
132   variations of the accumulation capacitances (*C*) and corresponding *k* values of the p-SiOCH layers
133   after the aforementioned treatment sequence were determined using *C-V* measurements, as plotted
134   in Figure 2. For the pristine p-SiOCH film, the accumulation capacitance per area was 2.266 X 10^{-4}
135   F/m^2, corresponding to a *k* value of 2.560. After a nitrogen-stuffing treatment at 450°C/4 atmosphere
136   for 5 min, the accumulation capacitance slightly increased to 2.317 X 10^{-4} F/m^2, leading to an increase
137   of *k* value to 2.618. Notably, the high-pressure nitrogen treatment results in the stuffing of the pores
138   within the p-SiOCH film [denoted as p-SiOCH(N)] with physisorbed nitrogen atoms (or molecules)
139   [16], thus rendering only a 2.26 % increase in *k* value. After sputter deposition of a 2-nm-thick Mn$_2$O$_3$
140   barrier, a large increase in accumulation capacitance of the p-SiOCH(N) film was measured,
141   associated with a marked   increase of *k* value to 2.914 (11.30 %). This increase is attributed to two
142   mechanisms: one is plasma-induced damage on the p-SiOCH(N) film during the deposition of Mn$_2$O$_3$
143   barrier [20]; another is the relative high *k* value of 5.10 of the coated Mn$_2$O$_3$ [21,22]. After annealing
144   with Ar/H$_2$ forming gas at 450°C for 1 h, Mn$_2$O$_3$ film became more stabilized. Moreover, the nitrogen
145   stuffed into the pores in the p-SiOCH(N) film was released and react with Mn$_2$O$_3$ film to form Mn$_2$O$_{3-}$
146    $_x$N layer. This transformation reduced the capacitance, resulting in a reduction of the *k* value to 2.845.
147   The capacitance and *k* value slightly decreased as Cu gate was formed. Further annealing (450°C/2 h)
148   of the Cu/Mn$_2$O$_{3-x}$N/p-SiOCH(N)/Si capacitor in an N$_2$ environment made the *k* value slightly
149   decrease to 2.757. In is worth mentioning that the *k* value of Cu/p-SiOCH/Si (without a barrier)
150   capacitors decreased upon annealing with a decreasing magnitude of 0.214, which could be caused
151   by Cu diffusion [23]. As a result, a lower decrease in the *k* value for Cu/Mn$_2$O$_{3-x}$N/p-SiOCH(N)/Si
152   capacitor upon annealing is indicative of greater Cu barrier capacity of the Mn$_2$O$_{3-x}$N layer.
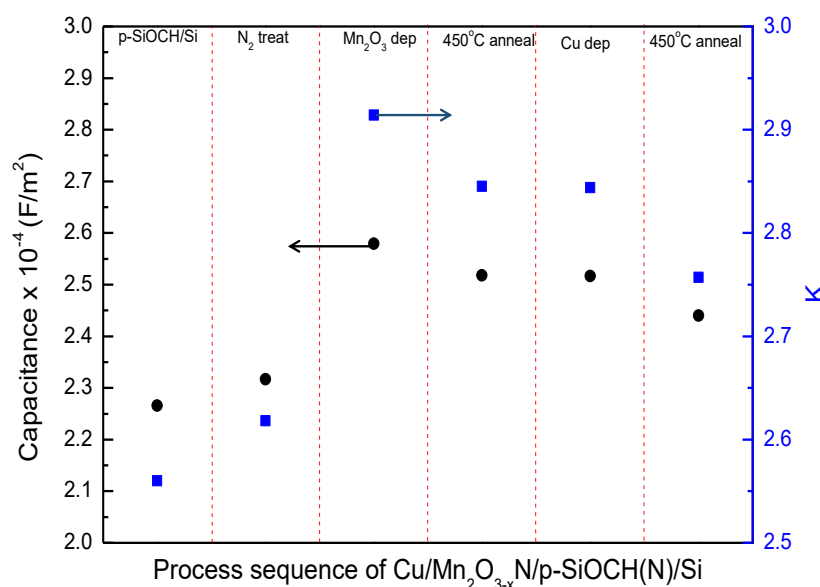
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Figure 2. Variations in capacitance and dielectric constant during Cu/Mn₂O₃₋ₓN/p-SiOCH(N)/Si integration.

Figure 3 plots the *I-E* curves of various Cu-gate capacitors before and after annealing. The negative-polarity voltage was applied and transformed to the electric field (E) by dividing it by the thickness of the p-SiOCH films. For all Cu-gate capacitors, the leakage currents increased with the electric fields, typically followed by a plateau, and then suddenly jumped. The applied field on the threshold of this jump is defined as a breakdown field of the p-SiOCH films. Prior to annealing and before breakdown of the p-SiOCH films, leakage currents of the capacitor samples without and with a Mn₂O₃ barrier layer were comparable, while those of the Cu/Mn₂O₃₋ₓN/p-SiOCH(N)/Si capacitors were substantially reduced by 1-2 orders. This finding indicates that the Mn₂O₃₋ₓN layer has a better barrier performance than the Mn₂O₃ layer, thus significantly improving electrical properties of p-SiOCH films. Furthermore, the conduction of leakage currents in dielectric materials is mainly through bulk transportation and surface migration of Cu atoms and ions. Therefore, leakage currents are ascribed to various factors, such as chemical structures of dielectrics, incorporated impurities, and metal-dielectric interfaces [24]. Since the Cu-gate capacitors studied here had the identical p-SiOCH film, the decrease in leakage current for the Cu-gate capacitor with a Mn₂O₃₋ₓN barrier layer is attributed to the improvement of metal-dielectric interfaces, thereby retarding surface migration of Cu atoms. After annealing, the leakage currents of all Cu-gate capacitors increased over the whole range of applied fields. The increase was most pronounced for the barrier-free samples, while the capacitor samples with a Mn₂O₃₋ₓN barrier layer exhibited the least increase in leakage currents. This implies that the conduction via metal-dielectric interface is the dominant mechanism for leakage current.
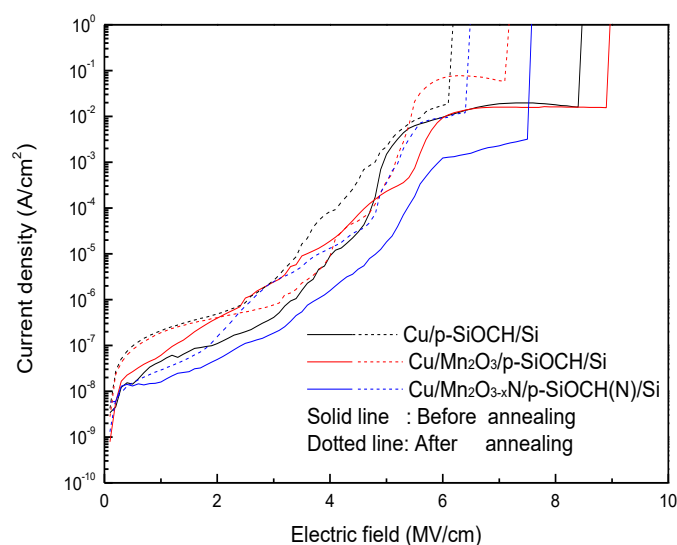
Figure 3. *J-E* plots of various Cu-gate MIS capacitors before and after annealing at 450°C for 2 h.

Figure 4 compares the breakdown fields of p-SiOCH films in various Cu-gate capacitors before and after annealing. Ten samples were measured for each condition. Before annealing, the magnitudes of breakdown fields follow the order of: Mn_2O_3 capped sample (8.74 MV/cm) > barrier-free sample (8.46 MV/cm) > $Mn_2O_{3-x}N$ capped sample (7.48 MV/cm). This trend is different from the result of leakage currents, suggesting that leakage current is not the necessary condition to trigger the breakdown of a dielectric film, which yields a reduced value of breakdown field as its molecular bonds are break up. For the p-SiOCH film in the Cu-gate capacitor with $Mn_2O_{3-x}N$ barrier layer, an additional annealing at 450°C for 1 h was performed on it before Cu gate deposition. The broken bonds were expected, thereby reducing the breakdown strength. Additionally, the barrier-free sample had a lower breakdown filed than the Mn_2O_3 capped sample due to the migration of Cu atoms/ions into the p-SiOCH film during Cu gate deposition. This suggests that a barrier is required for Cu/p-SiOCH integrity. After annealing, the breakdown fields of p-SiOCH films in all the capacitor samples were reduced. The largest magnitude of decreasing occurred in the barrier-free capacitor sample due to by bond breakage of p-SiOCH and Cu migration under thermal stress. With a Mn_2O_3 or $Mn_2O_{3-x}N$ barrier, Cu migration was inhibited. As a result, the reduction in the breakdown field was not as large as that obtained from the barrier-free sample. In the case of $Mn_2O_{3-x}N$ barrier, its magnitude of decreasing was the lowest, but the breakdown field variation was the smallest, suggesting that the $Mn_2O_{3-x}N$ layer is the best barrier against Cu thermal diffusion.
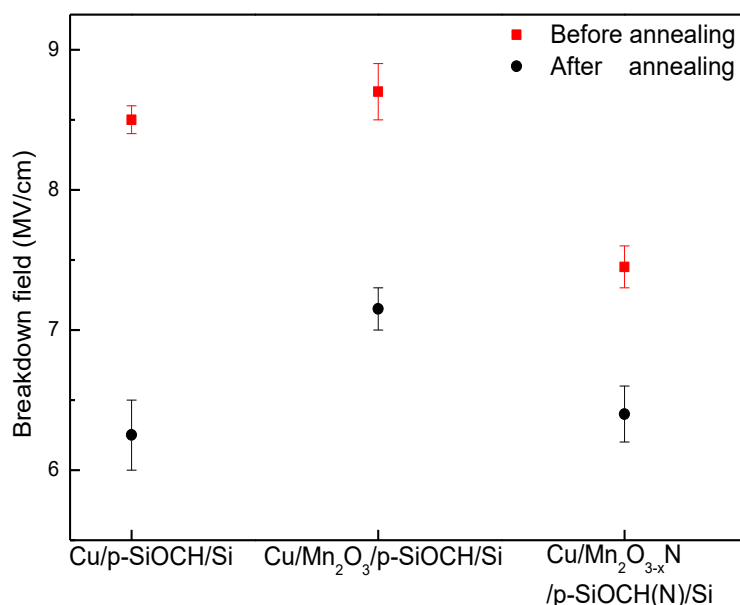
Figure 4. Comparison of breakdown fields of various Cu-gate MIS capacitors before and after annealing.

After thermal stress, *C-V* characteristics were measured again. Normalized *C-V* curves for the barrier-free and barrier capped capacitor samples before and after thermal stress (450°C/2 h) were compared and the shifts of their flat-band voltages (V_{fb}) were determined, as presented in Figure 5. The data presented here are the average values from 3 measurements for different capacitor samples. After thermal stress, the barrier-free capacitor sample exhibited a larger V_{fb} shift with negative direction. Additionally, its accumulation capacitance obviously decreased. These features represent the diffusion of Cu ions into the p-SiOCH film during thermal stressing [25]. For the Mn_2O_3 capped capacitor sample, V_{fb} still shifted toward negative voltage, but the shifting magnitude was obviously reduced. This result indicates that the diffusion of Cu ions into the p-SiOCH film is blocked by the Mn_2O_3 barrier, although, its blocking efficiency cannot reach 100 %. On the other hand, for the $Mn_2O_{3-x}N$ capped capacitor sample, a small V_{fb} shift was seen, but the direction was toward positive voltage. This positive shift of V_{fb} indicates the presence of negative charges, but not Cu diffusion into the p-SiOCH film, which in turn suggests that the retardation of Cu diffusion under thermal stress is ascribed to $Mn_2O_{3-x}N$ barrier and nitrogen-stuffed p-SiOCH film.
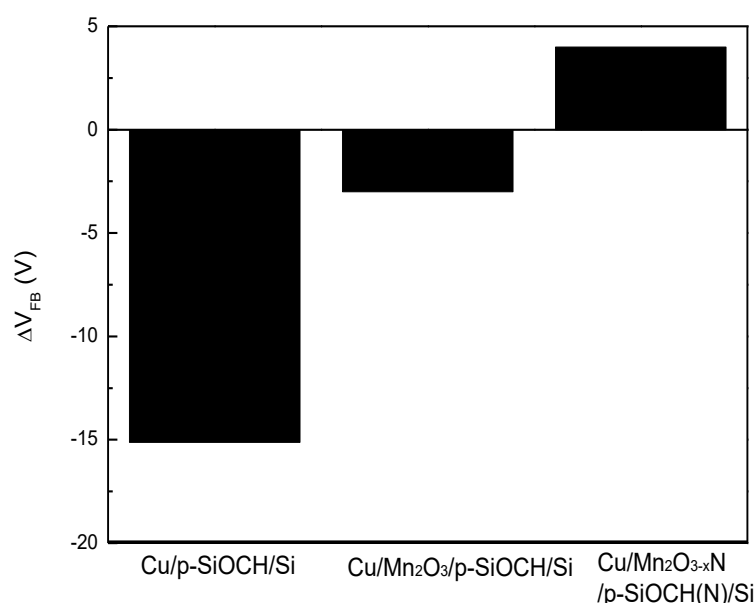
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Figure 5. Shift of flatband voltage (V_{FB}) of various Cu-gate MIS capacitors after being subjected to thermal stress.

In sum, Cu/Mn2O$_{3-x}$N/p-SiOCH(N) integration has been demonstrated to possess the best capacity against Cu thermal diffusion. However, under an electrical stress, Cu ions would drift into the p-SiOCH(N) (porous) dielectric film. Indeed, such phenomena is more pronounced for a porous film [26,27]. As Cu gate is stressed with a positive bias, Cu ions are generated and then drift into a dielectric film under the external electric field. After electrical stress, *I-V* characteristics with sweep at negative voltage were measured. The measured current is the response of both injection carriers and ionic currents.

Figure 6 (a) plots *I-V* curves of Mn$_2$O$_{3-x}$N capped capacitor samples before and after electrical stress (2.0 MV/cm) for various times. After electrical stress, the leakage current increased. Moreover, as the stressing time reached a certain value, a hump appeared at the voltage range from 0 to -20 V. The increase in the leakage currents is ascribed to the stress-induced trapping of within the p-SiOCH films. The appearing hump is mainly caused by ionic currents due to the migration of Cu ions. Under positive-polarity electrical stresses, Cu ions were generated, subsequently drifting into the p-SiOCH films following an assistance of the external electric fields. Then, during the application of negative-polarity voltages, the drifted Cu ions reversed back to the metal gate. Therefore, the presence of such a hump can be an indicator of Cu barrier capacity under an electrical stress. In this study, "Cu diffusion time" is defined as the stressing time of the positive-polarity stress required to produce this hump. A longer Cu diffusion time means a better Cu barrier capacity. Figure 6 (b) compares the Cu diffusion times of the three capacitor sample types as a function of electric field. The Cu diffusion times decrease with increases of the electric field for all the samples, indicating that a high electric field generates more Cu ions with faster drift rates. As expected, Cu-gate capacitors without a Mn$_2$O$_3$ barrier layer have the lowest Cu diffusion time. Cu-gate capacitors with Mn$_2$O$_3$ and Mn$_2$O$_{3-x}$N barrier layers have a longer and comparable Cu diffusion time, indicating that both barrier layers (Mn$_2$O$_3$ and Mn$_2$O$_{3-x}$N) have similar capacity in retarding Cu migration against electrical stress.
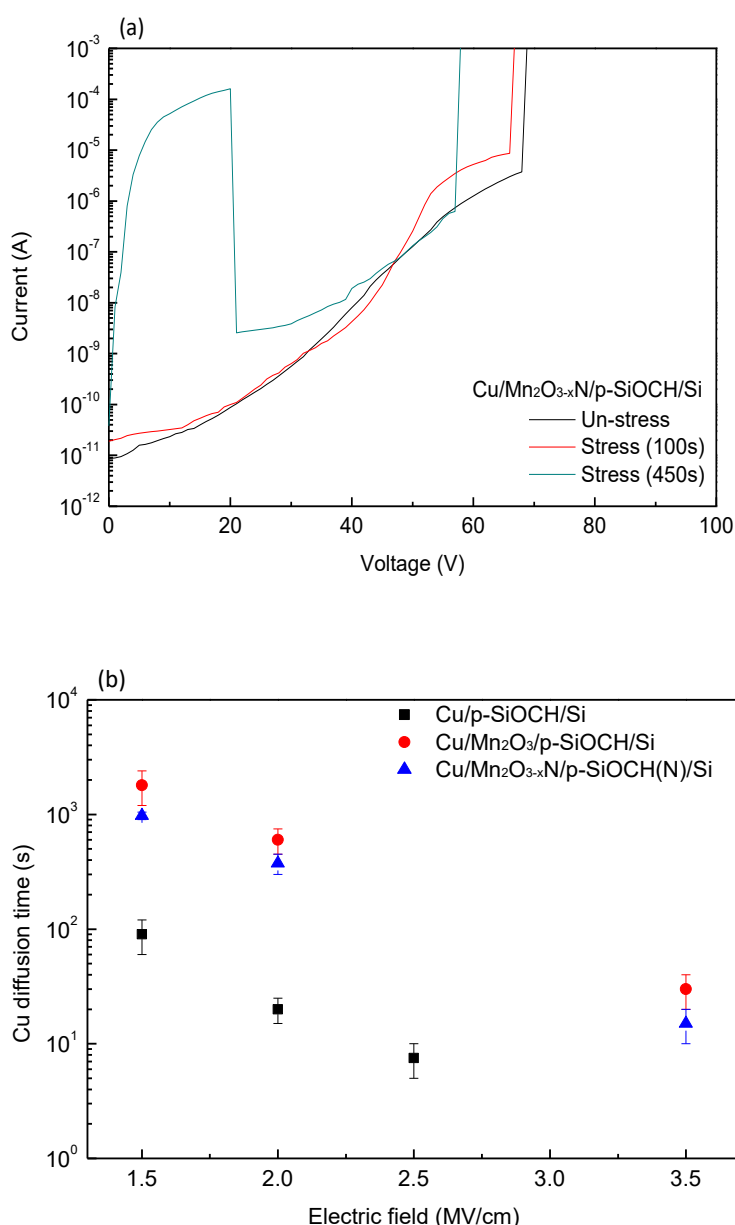
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Figure 6. (a) *I-V* curves of Cu-gate MIS capacitor with $Mn_2O_{3-x}N$ barrier before and after electrical stress (2.0 MV/cm) for various times; (b) Cu diffusion time of various Cu-gate MIS capacitors under electrical stress as function of electric-field.

245   The long-term reliability of p-SiOCH films in the Cu-gate MIS capacitors with various barriers
246   was evaluated by comparing the results of TDDB tests with those of barrier-free samples. During a
247   TDDB test (at 25°C), the samples were stressed by a constant electric field and the leakage current
248   was monitored until dielectric breakdown. The time-to-fail (TTF) was recorded as a leap in leakage
249   current by at least 3 orders of magnitude. Herein, At least three values of electric fields were used for
250   stressing and twelve MIS capacitors were measured for each condition, and the data of median TTFs
251   for various samples (before and after annealing) are presented in Figure 7. Similar to the results of
252   the breakdown fields measured from *I-V* measurements (Fig. 4), the measured TTFs display the same
253   order. That is, the p-SiOCH film in the Mn_2O_3 capped MIS capacitor exhibited the largest TTFs as
254   compared to those in other MIS capacitors. On the contrary, the $Cu/Mn_2O_{3-x}N/p$-SiOCH(N)/Si
255   capacitor had the shortest TTFs. After annealing, the TTFs of the p-SiOCH films in all the Cu-gate
256   MIS capacitors were reduced. Similarly, the p-SiOCH film in the Mn_2O_3 capped capacitor had the

257   largest TTFs. On the other hand, thermal annealing caused the lowest reduction in TTFs for the
258   Cu/Mn$_2$O$_{3-x}$N/p-SiOCH(N)/Si capacitor. As a result, its TTFs were slightly larger than those obtained
259   from the barrier-free samples. The result reveals that a barrier is required to ensure reliability for Cu
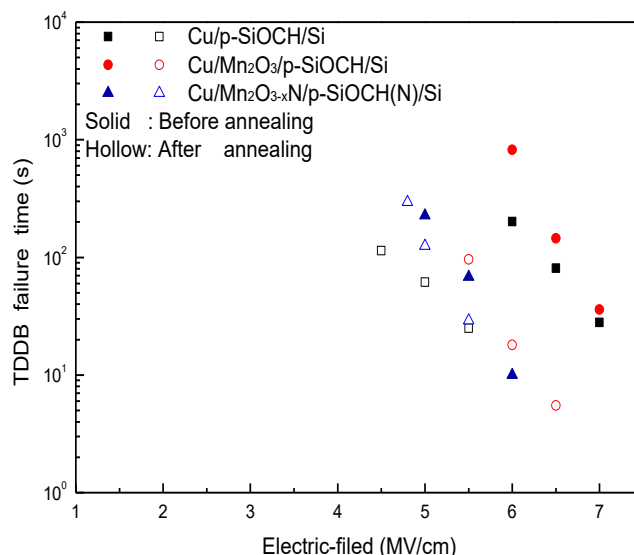260   and p-SiOCH integrity.

261

262   **Figure 7.** TTFs of p-SiOCH film in various Cu-gate MIS capacitors as function of applied electric-field
263   before and after annealing.

264   Annealing results in a reduction of TTFs; it also causes a change of slopes in the plots of TTF
265   versus the stressing filed, representing that the annealing causes an alteration of electric-field
266   acceleration factors. In this study, the *E* model [TTF = A exp (-γE)], which is the key to bond-breakage
267   mechanism, was used to describe the dielectric breakdown behavior [28,29]. In the equation, γ is the
268   electric-field acceleration factor, representing the extent to which TTF (derived from TDDB tests) is
269   affected by electric fields. A larger γ value means that TTF has a stronger dependence on electric fields.
270   Moreover, it provides a longer lifetime in lower operation fields. The γ values extracted from the plots
271   in Fig. 7 for the three different capacitor types before and after annealing are plotted in Figure 8. The
272   barrier-free capacitor sample before annealing had a lower γ value (2.42), which was significantly
273   reduced to 1.62 (the lowest). The decrease of γ value is believed to be caused by the drifting of Cu ions
274   [25]. Both capacitor samples with Mn$_2$O$_3$ and Mn$_2$O$_{3-x}$N barriers had the similar γ value of 3.12~3.13.
275   Upon annealing, a decrease in γ value to 2.86 was found in the Mn$_2$O$_3$ capped capacitor, whereas a
276   slight increase to 3.23 occurred for the Mn$_2$O$_{3-x}$N capped capacitor, indicating better Cu barrier
277   efficiency of the Mn$_2$O$_{3-x}$N layer. The large γ value for the Cu/Mn$_2$O$_{3-x}$N/p-SiOCH(N)/Si capacitor has
278   a dramatic benefit to promote a dielectric lifetime in a low operation field. As a result, the lifetimes
279   of the Cu-gate MIS capacitor with the Mn$_2$O$_{3-x}$N barrier layer surpass that obtained from the Cu MIS
280   capacitors with the MnO$_x$ barrier layer when the operation field is lower than 4.06 MV/cm.
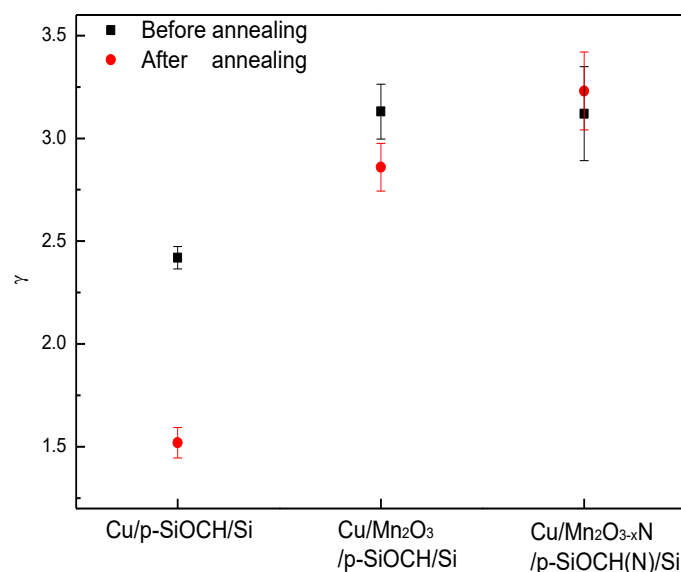
Figure 8. Electric-field acceleration factor of various Cu-gate MIS capacitors before and after annealing.

5. Conclusion

The electrical characteristics and reliability of the integrated Cu/Mn$_2$O$_{3-x}$N/p-SiOCH(N)/Si structure have been investigated in this study. In the as-fabricated stage, Cu/Mn$_2$O$_{3-x}$N/p-SiOCH(N)/Si structure exhibited poor dielectric breakdown characteristics, although, less degradation was observed after thermal stress. Moreover, its Cu barrier efficiency and TDDB electric-field acceleration factor were improved. Consequently, the proposed Cu/Mn$_2$O$_{3-x}$N/p-SiOCH(N) is a promising integration processing for Cu/porous low-*k* interconnects.

Conflicts of Interest: The authors declare no conflict of interest.

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