

Article

# Active Power Tracking Control Strategy to Suppress DC-Link Voltage Rising with Enhanced Fault Ride-Through Capability using Superconducting Fault Current Limiter

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**Abstract:** Building a new power plant to address the growing demand for power due to population concentration in the metropolitan area is one of the world's major concerns. However, since a large power plant can not be located around the city due to burden of economic cost, building power plant outside metropolitan and cities is necessary. Therefore, new power generation facilities are promoting policies to provide distributed generator(DG) with a small capacity relatively near the metropolitan. When the DG (photovoltaic, wind farm, etc.) is connected with the grid using medium voltage direct current (MVDC) system, voltage sourced converter(VSC) should supply reactive power to the grid, because of fault ride through(FRT) operation in grid fault. If the voltage drop is severe, the converter should be disconnected from the grid immediately without supplying the reactive power, resulting in a considerable economic loss. In general, superconducting fault current limiter(SFCL) is introduced as a measure to enhance FRT capability. In this paper, we use trigger type SFCL which protects superconducting element and reduces low voltage. On the other hand, the active power unbalance of the DC-link and the DC voltage rise due to the reactive power supply of the grid-side converter. The rise of the DC voltage causes the P (active power), Q (reactive power) control of the converter to deviate, causing malfunction and damage of the DC equipment. Therefore, the rise of the DC voltage must be prevented. In this paper, we consider the suppression the DC voltage rising caused by the FRT operation through the active power tracking control (APTC).

**Keywords:** distributed generator (DG); medium voltage direct current (MVDC) system; voltage sourced converter (VSC); fault ride-through (FRT); trigger type superconducting fault current limiter (SFCL); active power tracking control (APTC)

## 1. Introduction

Recently, global problems such as population concentration in the metropolitan, environmental pollution and global warming have led to the spread of renewable energy around the world. New and renewable energy sources are generally classified as distributed generator(DG) because they are small in capacity and distributed close to cities. When connecting the DGs to the grid, the grid code such as total harmonic distortion (THD) and reliability should be satisfied. Using the voltage sourced converter(VSC) DC system, the grid code can be effectively satisfied. Germany's grid code is renowned for its rigorous regulation about grid-connected DG systems. Among them, there is a fault ride-through (FRT) in which reactive power must be supplied when a system voltage drop [1]. Figure 1 shows that the reactive power can be controlled at the discretion of the operator when the voltage of the grid is between 0.9 and 1.1 [p.u.]. However, when the voltage deviates from the dead band, the

reactive power is supplied according to the grid voltage. With supply of reactive power, the grid AC voltage is recovered, but the DC voltage rises as the input / output power of the DC-link becomes unbalanced. When the DC-link voltage decreases, the input power decreases or the output power increases. On the other hand, when the DC-link voltage rises, the input power increases or the output power decreases [2-3].

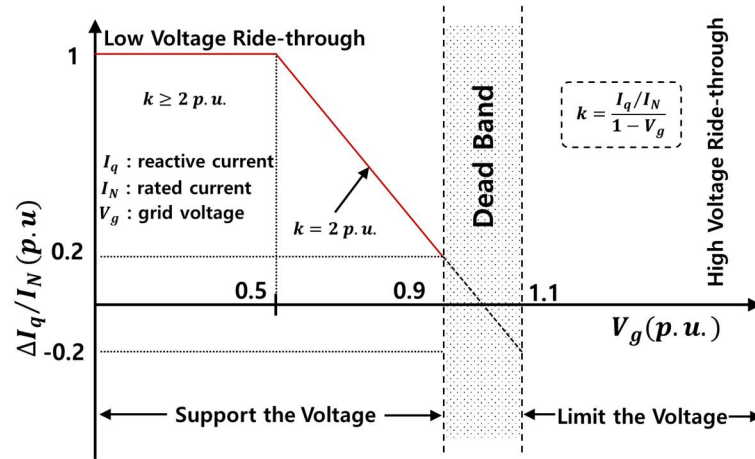


Figure 1. Reactive Current Supply Condition

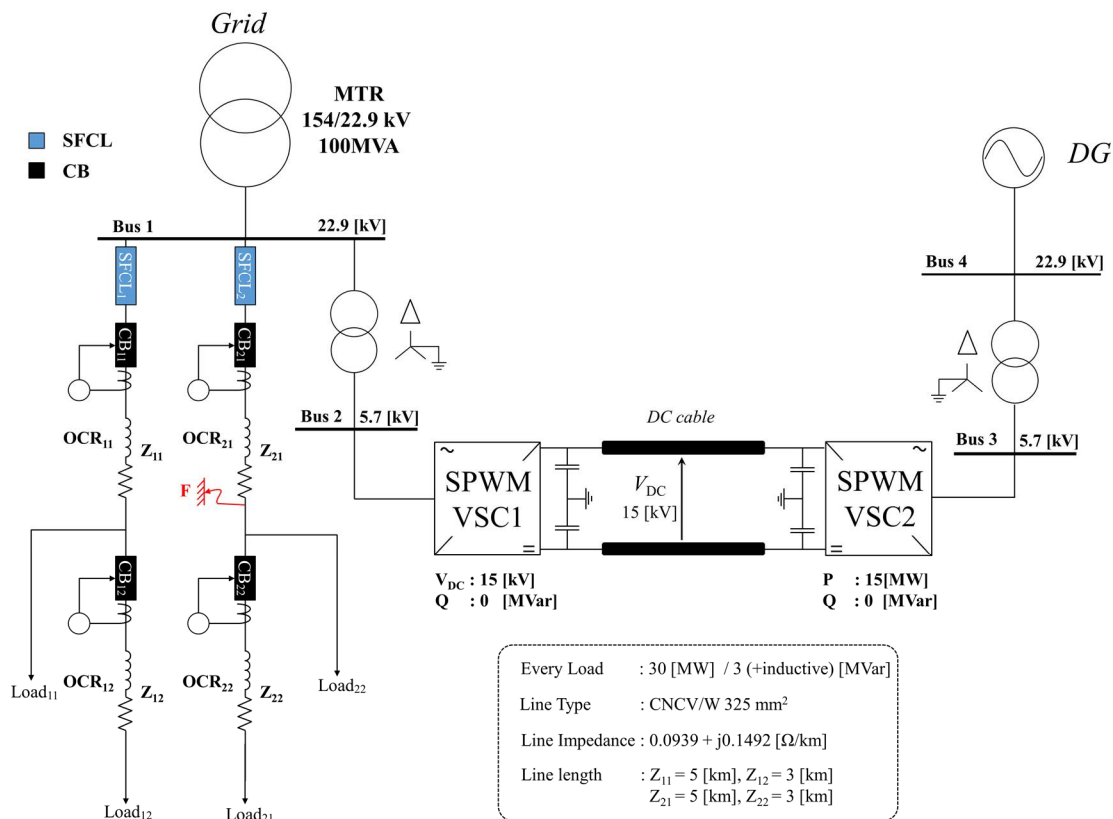


Figure 2. Configuration of the Grid with DC System for Distributed Generator(DG)

The Figure 2 above is a configuration of grid with DC system for DG to use in this paper. The grid is connected to two feeders via MTR, and a DC-link is connected to the same bus. The DC-link is a transmission line connecting the DG and the grid. Normally, active power is transmitted from DG to the grid along this DC-link. The voltage drop of Bus1 and Bus2 were simulated by three-phase ground fault at F (fault location). After the grid-side bus voltage drop, the VSC1 supplies reactive

power for FRT operation, which reduces the amount of active power transmission in the VSC1. The reason is that as the reactive power increases, the amount of active power already supplied decreases. Thus, although input power is constant in DC-link, output power is reduced. The power of DC-link becomes unbalanced, accumulating in capacitors and DC-link voltage rises. The way to suppress the DC-link voltage rise is decreasing the output of the DG [4-5]. Because controlling the output of the DG is not done immediately, it is not suitable in situations that must be dealt with in a short period of time, such as fault. On the other hand, there is another method of dissipating power within the DC-link [6-7]. However, in order to dissipate energy, a chopper resistor must be installed in the DC-link, which requires a lot of space around the converter station and installation and maintenance costs. This method is a reliable solution, but it is not economical. In this paper, we try to control the active power of the converter to solve these problems. Control the active power of VSC2 by inversely calculating the output to be adjusted based on the increased DC voltage. This is called as active power tracking control (APTC).

On the AC grid-side, using the trigger type superconducting fault current limiter (SFCL), we identify that the fault current in the feeder is reduced and the voltage drop of Bus1 and Bus2 is suppressed [8-10]. The SFCL used in the grid is usually resistive type SFCL. This is because the resistive type is more economical than other SFCLs, and has a high limiting impedance and a large capacity. However, resistive SFCLs are vulnerable to large fault current because the burden on superconducting elements is directly applied. The trigger type SFCL limits the fault current to the CLR by commutating the current to the parallel circuit of the superconducting element when the superconducting element is quenched and overloaded. Consequently, the trigger type SFCL suppresses the AC voltage drop through the CLR resistor, making it easy to change the impedance and thereby effectively enhance the FRT capacity [8-9].

## 2. Theoretical Investigation and Modeling

In order to construct a system in which DG is connected to a grid by DC-link, DG and VSC are primarily modeled. The VSC has different functions depending on the purpose of use. As shown in Figure 2, VSC1 controls the DC voltage and reactive power (Q), and VSC2 controls the active power (P) and Q. Since DG is not a model for control purposes, it is conceived to have a synchronous generator with a constant P output. The over-current relay (OCR), circuit breaker, and SFCL are modeled based on the system constructed as shown in Figure 2. Finally, a control block diagram for controlling P of VSC2 in condition during fault is modeled [10].

### 2.1. Theoretical investigation of voltage sourced converter (VSC)

Unlike CSC, which has been used in the past, each VSC stage in a DC serves as a constant voltage source. In other words, the DC voltage is kept constant even if the power direction changes or the size changes. The VSC model used in this paper can be configured as a CSC because of the structure in which two converters are connected in series. However, since the global trend is aimed at a multi terminal where multiple converters are connected to one another, there is a problem in operating it. In addition, since CSC uses SCR instead of IGBT or GTO, it has an inherent problem that independent control of reactive power and active power can not be done. These VSCs can selectively control DC voltage, active power, reactive power, and AC-side voltage, as mentioned briefly above. "Selectively" means that the DC voltage and the active power are physically related. It is. That is, since the active power is used to control the DC voltage, the two things can not be simultaneously controlled to a desired reference value. The reactive power and the AC voltage also have the principle of supplying reactive power to control the AC voltage, so that independent control is impossible.

Since the DC voltage and the active power control can not be simultaneously performed in one VSC, the role of each VSC differs. In the case of VSC1 in Figure 2, the DC voltage is controlled, so the active power won't be controlled. In this case, VSC1 receives only the active power supplied from VSC2, and sends power to the grid to maintain the DC voltage according to this power.

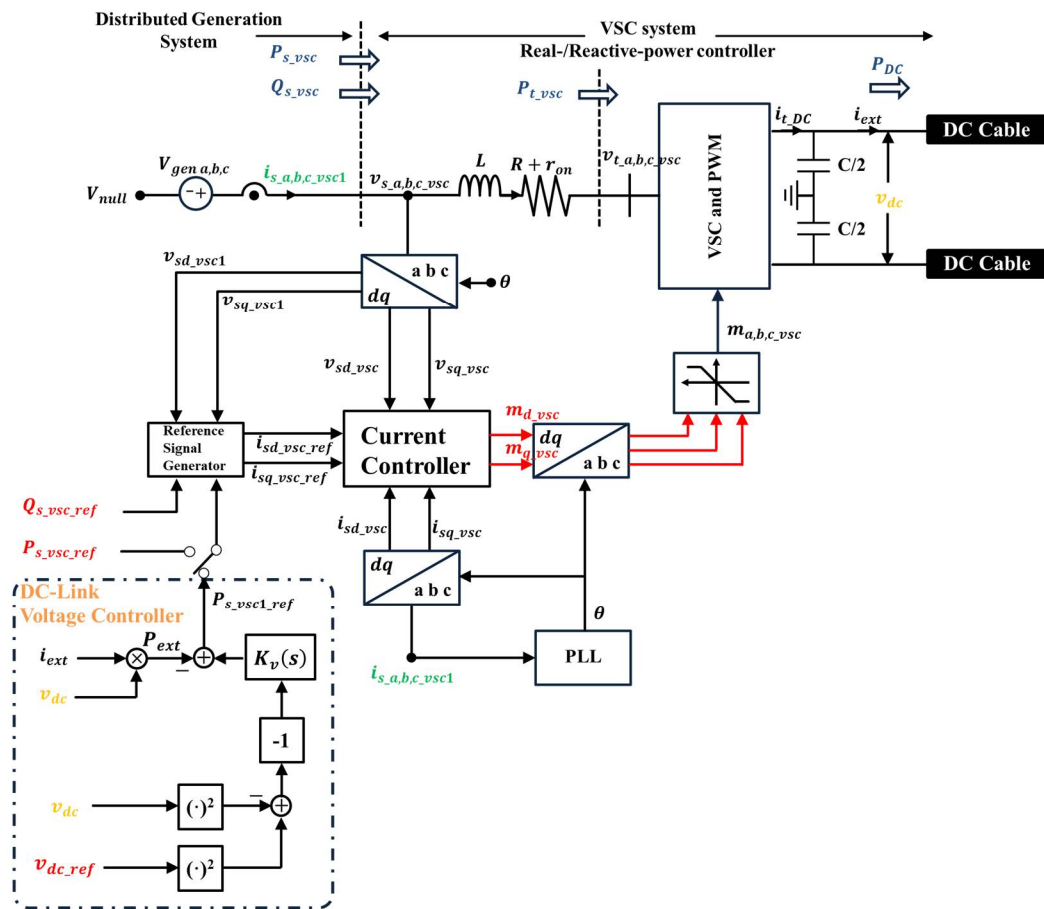


Figure 3. Control Block Diagram for Voltage Sourced Converter(VSC) and Pulse Width Modulation(PWM)

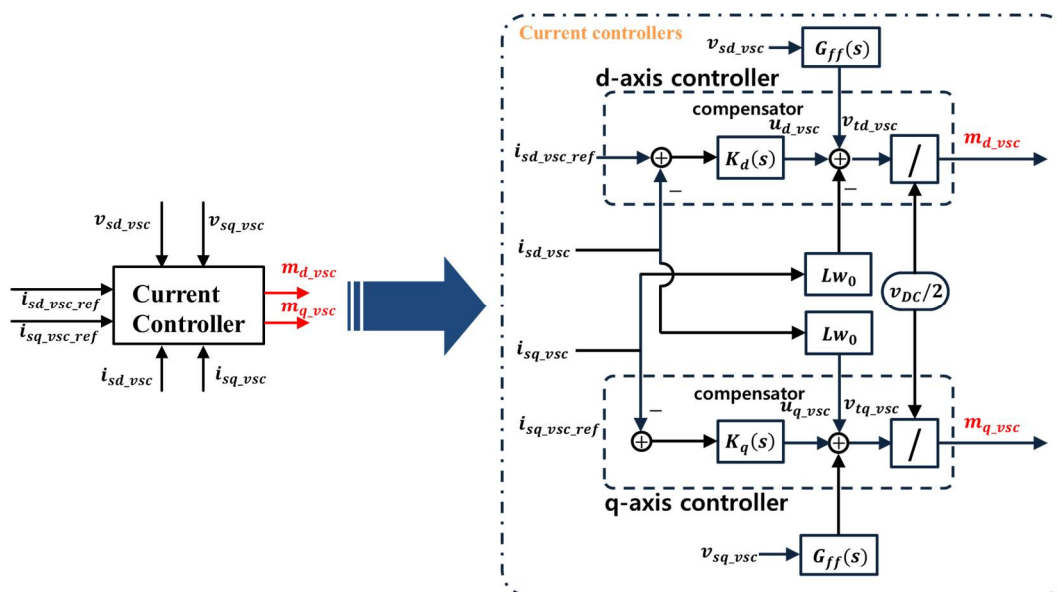


Figure 4. Control Block Diagram for DQ-Axis Current Controller

As shown in Figure 3 and 4, the VSC basically controls the d-q axis current through the current controller. Based on this, the current signal is converted into a modulating signal, which is used as a reference signal to modulate the PWM signal to control the gate operation of the IGBT. The following

equations (1) and (2) are the formula for generating the modulating signal. These equations can be derived from the AC side voltage equation from Figure 3 and represented by control block diagrams as shown in Figure 4.

$$m_{d\_vsc}(t) = \frac{2}{v_{dc}(t)} \{u_{d\_vsc}(t) - Lw_0 i_{sq\_vsc}(t) + v_{sd\_vsc}(t)\} \quad (1)$$

$$m_{q\_vsc}(t) = \frac{2}{v_{dc}(t)} \{u_{q\_vsc}(t) + Lw_0 i_{sd\_vsc}(t) + v_{sq\_vsc}(t)\} \quad (2)$$

When making the d-q axis current signal, it passes through the reference signal generator as shown in Figure 3 and its main input signal is active power and reactive power. The relationship between P, Q and each d-q axis current is expressed in the following equations (3) and (4). In particular, equation (4) shows the relationship between q-axis current and reactive power.

$$i_{sd\_vsc\_ref}(t) = \frac{2}{3} \frac{1}{v_{sd\_vsc}(t)} P_{s\_vsc\_ref}(t) \quad (3)$$

$$i_{sq\_vsc\_ref}(t) = -\frac{2}{3} \frac{1}{v_{sd\_vsc}(t)} Q_{s\_vsc\_ref}(t) \quad (4)$$

Equations (3), (4) can be expressed in terms of the d-q axis for P and Q, as in equation (5) and (6). Here, some of the terms can be eliminated because the q-axis voltage is synchronized to zero.

$$P_{s\_vsc}(t) = \frac{3}{2} [v_{sd\_vsc}(t) i_{sd\_vsc}(t) + v_{sq\_vsc}(t) i_{sq\_vsc}(t)] \quad (5)$$

$$Q_{s\_vsc}(t) = \frac{3}{2} [-v_{sd\_vsc}(t) i_{sq\_vsc}(t) + v_{sq\_vsc}(t) i_{sd\_vsc}(t)] \quad (6)$$

As mentioned in Section 2.0, P and Q values are dependent variables for controlling DC voltage and AC voltage, respectively. Therefore, transfer function for DC voltage  $v_{dc}^2(s)$  and active power  $P_{s\_vsc1}(s)$  should be obtained.

$$\frac{v_{dc}^2(s)}{P_{s\_vsc1}(s)} = -\frac{2}{C} \left[ \frac{1 + s\tau}{s} \right] = k_v(s) \quad (7)$$

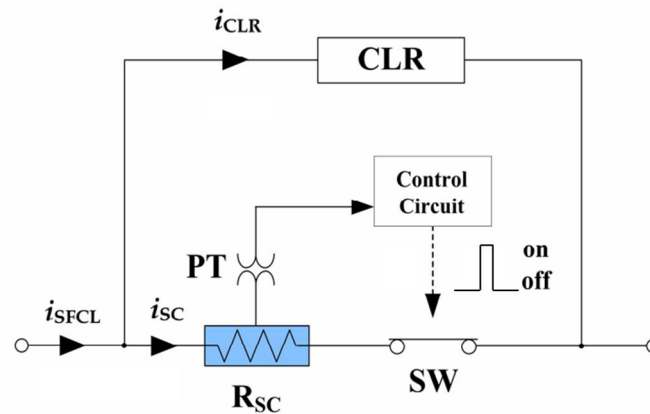
$$\tau = \frac{2LP_{s\_vsc1\_0}}{3\hat{v}_{s\_vsc1}^2} \quad (8)$$

Where subscripts 0 represents steady-state value of the  $P_{s\_vsc1\_0}$  when the small-signal perturbations are separated. The  $\hat{v}_{s\_vsc1}$  signifies a value that has only the angular frequency and magnitude of  $v_{s\_vsc1}$  and has no phase [10].

## 2.2. Modelling of trigger type superconducting fault current limiter (SFCL)

Superconducting fault current limiter (SFCL), which has been used worldwide, was a resistive type SFCL. The resistive type SFCL is a structure in which CLR and superconducting element (SCE) are connected in parallel. Therefore, there is a problem in protecting the superconducting element because the current continues to flow in the SCE. If the SCE resistance is high and the CLR resistance is designed low, the superconducting element can be protected, but the impedance that limits the current becomes lower. Current limiting and SCE protection are trade-offs.

Trigger type SFCL can take the voltage signal from the superconducting resistor through the PT and operate the SW, so that the SCE can be protected and the limiting impedance can be set high. The topology of the trigger type SFCL is shown in Figure 5.



**Figure 5.** Topology of Trigger Type Superconducting Fault Current Limiter(SFCL)

Before the fault, the resistance of SCE ( $R_{sc}$ ) is zero and the  $i_{CLR}$  is also zero. At this time, when a fault occurs and the  $i_{sc}$  exceeds the critical current of the SCE, the  $R_{sc}$  is quenched and becomes the normal state. As a result, the  $i_{sc}$  current is reduced and the  $i_{CLR}$  is increased. The voltage signal applied to the  $R_{sc}$  is received by the PT and sent to the control circuit. The control circuit calculates the voltage signal and converts an on / off signal to be sent to the SW. When SW is open, all current flows to CLR and the fault current is limited by the CLR impedance.

$$R_{sc}(t) = \begin{cases} 0 & (i_{sc} < \text{critical current}) \\ R_n \sqrt{-e^{-\frac{1}{\tau_0}(t)} + 1} & (i_{sc} \geq \text{critical current}) \end{cases} \quad (9)$$

Mathematical modeling of this superconducting resistance for the last century was one of the greatest interests for researchers and several prototypes have been developed and researched [11]. One of the studies is to model the superconducting phenomenon mathematically. Implementing this superconducting phenomena is essential for modeling the superconducting resistance. However, accurate modeling is very difficult because the quenching phenomena is affected by whole the magnitude field, current through it and the temperature [12]. Supposing that it is only excited by the current, the superconducting resistance can be expressed as the following equation (9) where  $R_n$  is the normal state resistance [11].

### 2.3. Modelling over current relay (OCR)

Generally, equation (10) is used for modeling of the OCR's characteristics. TD means time dial, A, B and p are constant value. The M is a variable depending on the feeder current ( $I_p$ ) through the OCR measured by CT. The definition of M is given in equation (11). The  $I_{pickup}$  is the presetting value that the OCR user desires the trip performance to start [13].

$$T_{trip} = TD \left( \frac{A}{M^p - 1} + B \right) \quad (10)$$

$$M = \frac{I_p}{I_{pickup}} \quad (11)$$

The definition of the integration signal (INT) is needed to create the actual trip signal to be input to the circuit breaker based on the trip. For OCR's trip operation, INT is calculated by integrating the reciprocal of the variable  $T_{trip}$  only when the M is bigger than the pre-setting values. When the accumulation of the INT reaches threshold value '1', the OCR output trip signal to circuit breaker for the interruption.



Through equations (10) and (11), it can be predicted that the operation of OCR is delayed by applying SFCL.  $T_{trip}$  will become larger when  $I_p$  which determines M value becomes smaller. To improve the delay rate, there is some researches to correct the variable M or the TD value of OCR. In this paper, however, general OCR is modeled without correction of variables and constant values.

### 3. Active Power Tracking Control (APTC) for Suppression of DC-link Voltage Rising

As discussed in the introduction above, according to the FRT, when an abnormal voltage in the grid occurs, the VSC must supply or consume reactive power. When reactive power is supplied, the amount of active power is reduced, resulting in a power imbalance of the DC-link and a rising in voltage. The solution to this problem is to use chopper resistance [14]. It is a method to solve the power imbalance by installing a resistor in parallel to the DC-link, but the problem can't be solved when the DC voltage drops. In addition, there are some inefficiencies in terms of site to install and economic feasibility. Another alternative is the de-loading method, which controls the torque output of the wind turbine under the assumption that DG is an offshore wind farm. At that time, the HVDC de-loading droop technique provides a multiplying factor to the converter's active power current controller. Thereby reducing the active power current of the converter and controlling the DC voltage [15]. This method requires fast communication with the DC-link VSC and all wind turbines in the wind farm.

In this paper, instead of controlling the multiplying factor to control the DC voltage, a new reference value is generated by adding the inverse calculated value of the DC voltage difference to the reference value of the existing active power. This method is called active power tracking control (APTC) and it is expressed in Figure 6.

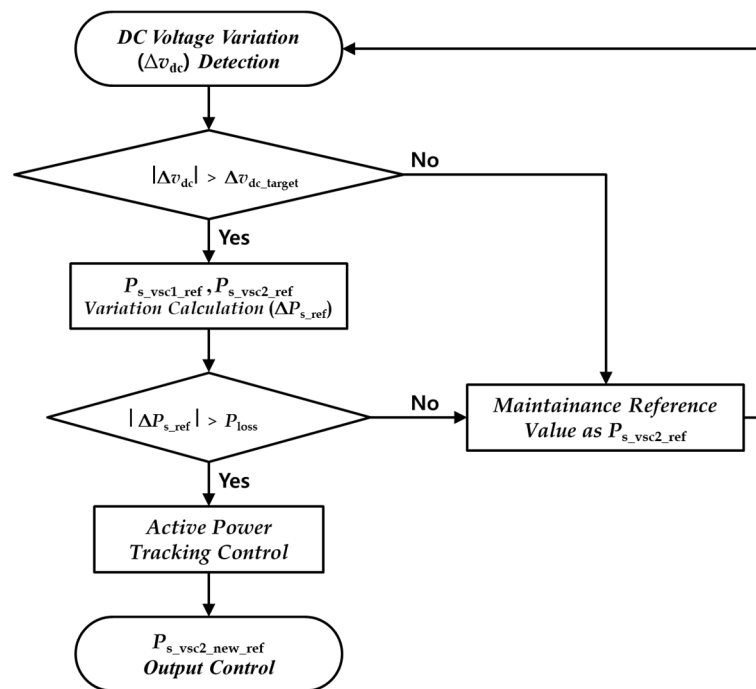


Figure 6. Operation Algorithm of Active Power Tracking Control(APTC)

When the DC-link voltage variation increases beyond its threshold value, APTC algorithm calculates the difference of DC-link power with input and output power in each VSC. If the variation of power in DC-link is bigger than the cable and conversion loss, the operation proceeds through APTC and otherwise maintain the active power reference value of the VSC2. When the new command value obtained from the APTC enters into the current controller, the input active power in VSC2 is reduced. In Figure 7, the variation of the DC-link voltage makes  $P_{s\_vsc2\_control}$  through the previously obtained transfer function  $K_v(s)$ . And adds  $P_{s\_vsc2\_control}$  to  $P_{s\_vsc2\_ref}$  to create a new command

value  $P_{s\_vsc2\_new\_ref}$ . The APTC on / off signal is output from APTC on-off signal generator according to the operation algorithm in Figure 6.

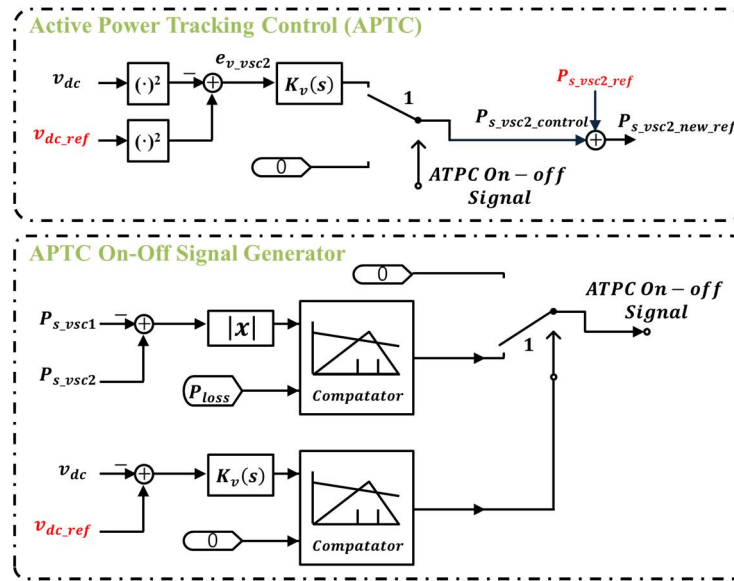


Figure 7. Control Block Diagram of Active Power Tracking Control(APTC)

If the active power of the VSC2 becomes smaller due to the new reference value of the active power, the power imbalance of the DC link is resolved and the rise of the voltage is also suppressed.

#### 4. Simulation Results and Discussion

As a method of verifying the operation of APTC, there is a simulation based on the theoretical modeling. It is more accurate to construct experiment with hardware and experimental grid and DG systems, but this is practically limited due to economic reasons.

In this study, a VSC2 that operate APTC connected to DG was considered. The VSC1 controls the DC voltage through the active power regardless of the fault, and the reactive power has the output of 0 [MVar] on normal state, but performs the FRT operation at the low voltage due to the fault. The VSC2 controls the active power to 15 [MW] without any reactive power at the normal state. However, when the voltage of the DC link rises due to the FRT operation of VSC1, the VSC2 performs the APTC operation. At the same time, the trigger type SFCL operates first in the fault location of the power distribution system. If the fault continues, the circuit breaker is tripped by the relay to stop the fault.

##### 4.1. Simulation setup

Figure 2 shows the grid connected with the distribution system and the DG linked by DC-link. A 300 [ms] three-phase short circuit fault was applied at the F (fault location) at 0.5 [s]. Simulation studies were carried out in EMTDC/PSCAD and the parameters for simulation in a whole system are given in the Appendix A. In the event of the fault, the voltage of the fault location (F) of the feeder drops to 0 [V] at 0.5 [s]. The current flowing through the feeder increases and the current through current transformer (CT) increases beyond pickup current of OCR. The modeling indexes required for SFCL and OCR operation in the simulation are also given in Appendix A.

##### 4.2. Protection of distribution system

In distribution system, the fault occurs on the middle of feeder. the voltage at the fault location becomes zero and the current increases greatly. Until this time,  $i_{CLR}$  is 0 and all current flows through the SCE ( $i_{SC}$ ). When the SCE current in the trigger type SFCL increases beyond its critical current, the SCE is quenched and the  $R_{SC}$  changes to a non-zero normal-state resistance. According to Figure 8,  $R_{SC}$  is 0 until the  $i_{SC}$  exceeds the critical current of 3 [kA] even after the fault occurs. However, after



237 quench, current flows to  $i_{CLR}$  because  $R_{SC}$  is no longer zero. When the SC voltage exceeds the SW  
 238 trip voltage, SW is tripped. Thereafter, the current is more limited because the  $R_{SFCL}$  increases to the  
 239  $R_{CLR}$  (0.5  $\Omega$ ).

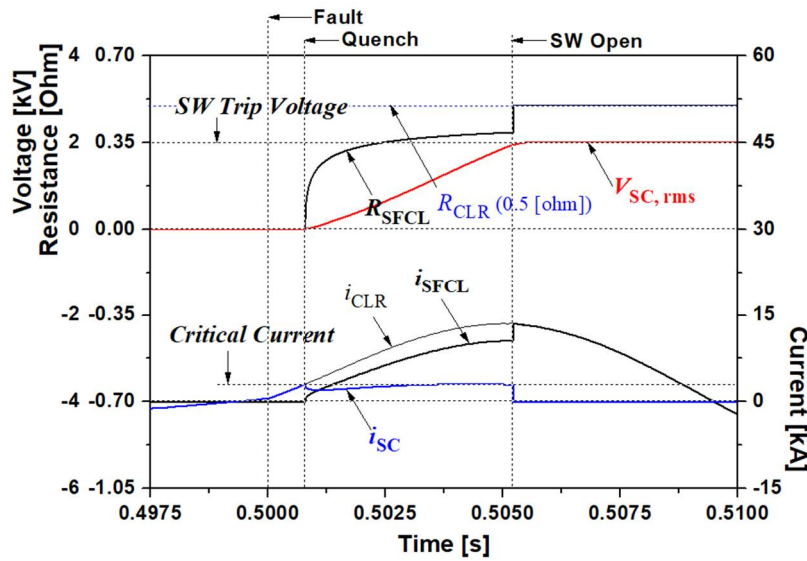


Figure 8. Voltage, Resistance and Current of SFCL with or without Active Power Tracking Control (APTC)

242 The positive current at the feeder's OCR ( $I_p$ ) increases to 3.5 [kA] over  $I_{pickup}$ , which causes the  
 243 OCR to proceed. Figure 9 shows the OCR operation with and without a trigger type SFCL under the  
 244 same fault conditions. The superscript 'with SFCL' and 'w/o SFCL' indicate result of simulation case  
 245 with or without SFCL. The subscript 'with APTC' and 'w/o APTC' are similar to superscript except  
 246 for APTC instead of SFCL.

247 As mentioned, OCR trip is implemented by using positive current ( $I_p$ ) of 3-phase current for M  
 248 of OCR variable without each phase current. Due to the fault, all three-phase currents increase  
 249 largely. The phase difference is 120 [degree] per phase, and the fault current magnitude varies with  
 250 fault phase, so the trip time of OCRs in each phase is different. In Figure 9 (a) and (b), when  $I_p$   
 251 exceeds 3.5, the variable M increases beyond 1, and the calculated  $T_{trip}$  (TCC) also has a certain  
 252 value.  
 253

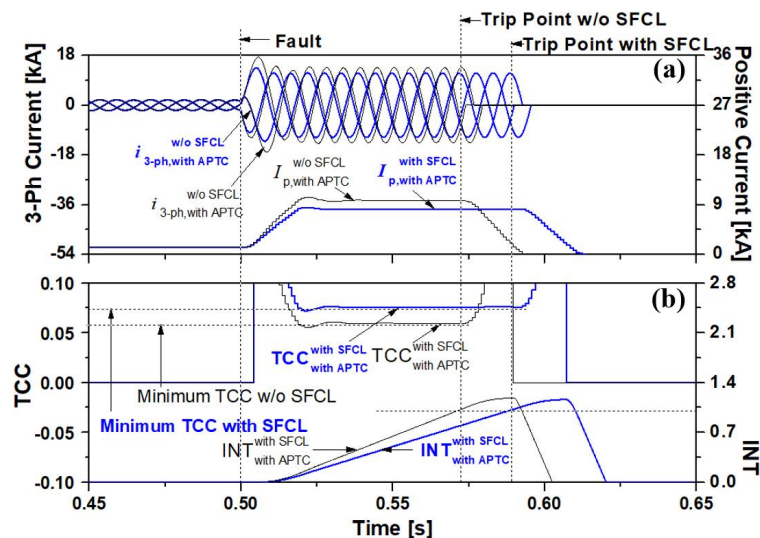


Figure 9. OCR Operation (a) 3-ph Current & Positive Current of Grid-side VSC1 Current  
(b) TCC & INT Signal

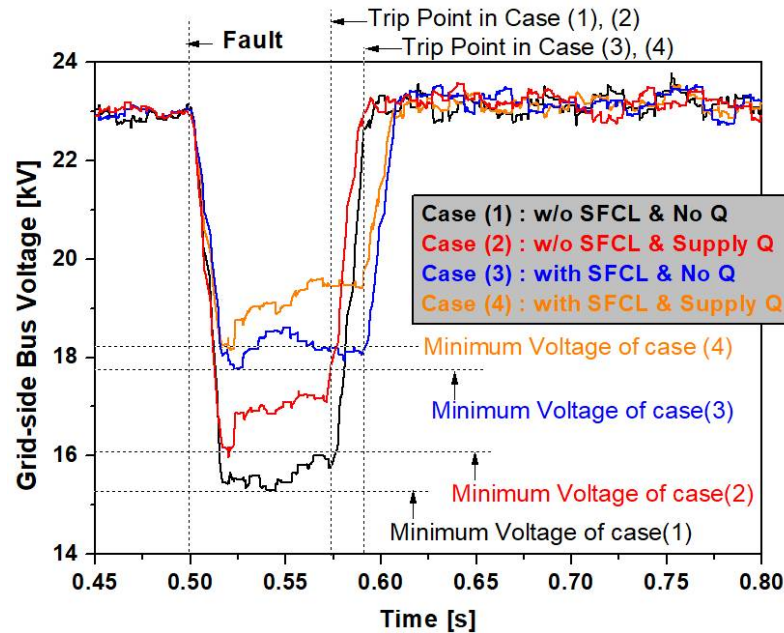


Figure 10. Grid-side Bus Voltage in Four Case

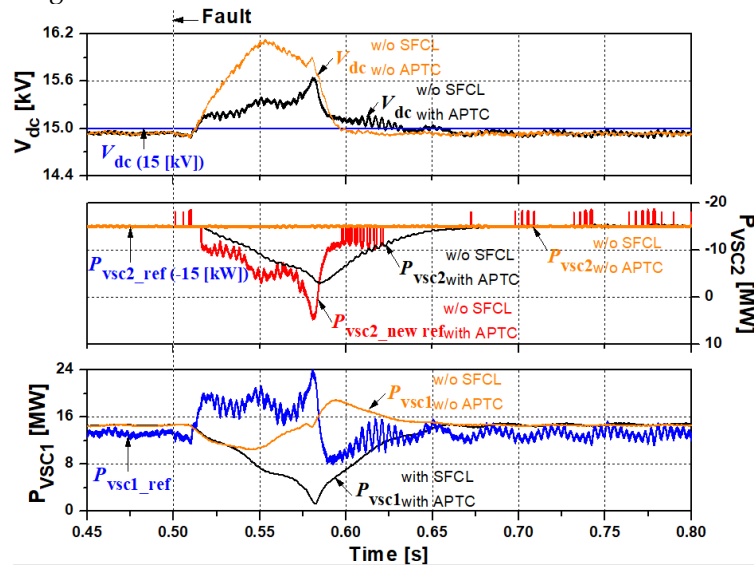
When the SFCL is applied, it can be seen in the Figure 9 (a) that the trip time is delayed as compared with when the SFCL is not applied. In the case of applying SFCL, the magnitude of the current ( $I_p$ ) is reduced, so that the value of the variable M becomes smaller, the TCC becomes larger, and the slope of the INT becomes smaller.

#### 4.3. FRT and APTC operation

In the distribution system, the system protection is progressed by SFCL and OCR due to the fault, and FRT operation is proceeded due to the bus voltage drop in the VSC1 terminal. Figure 11, the bus voltage is confirmed by dividing into four cases. In case (1) without FRT operation and applying SFCL, the bus voltage drops to 15.3 [kV]. In case (2), when the AC voltage drops to 0.9 [p.u.] as shown in Figure 1, the FRT operation is designed to supply reactive power to the grid. After reactive power is supplied, the lowest voltage rises to 16.2 [kV] and the voltage drop improves to 16.9 [kV] on average. In the case of FRT, it takes a long time to recover the voltage because there is a slight delay time that  $Q_{s\_vsc1}$  follows the  $Q_{s\_vsc1\_ref}$ , after giving the reactive power reference value ( $Q_{s\_vsc1\_ref}$ ), and it can be seen that there is not much recovery immediately after the occurrence of the voltage drop. In case (3) that the SFCL is applied among the protection schemes described in Section 4.2, the voltage drop is recovered to 17.8 [kV]. Also, when the trigger type SFCL is applied, the voltage drop immediately recovers. In final case, if the SFCL and the reactive power supply are combined, the trigger type SFCL operates instantaneously, recovering to 18.2 [kV] and gradually increasing to 19.5 [kV].

If the reactive power is supplied by the FRT, the DC voltage rises, but it can be suppressed by the active power tracking control APTC method. The APTC is a method of controlling the VSC2 active power on the DG side as discussed Section 3. As the  $Q_{vsc1}$  increases due to the FRT operation, the  $P_{vsc1}$  decreases and the DC voltage rises. To solve this, the power imbalance on the DC-link must be resolved. In the conventional method, a chopper resistor was applied to the DC-link to consume excess input power. Another method is to change the current controller multiplying factor of VSC2 to control  $P_{vsc2\_ref}$ . Since there are disadvantages to each method, this paper adopts a new method of calculating the additionally required  $P_{vsc2\_control}$  by subtracting the difference between the DC-

link voltage reference value and the practical voltage, and adding this  $P_{vsc2\_control}$  to the existing  $P_{vsc2\_ref}$  value. Figure 11 is a graph showing the result of controlling the active power to suppress the DC voltage rising.



**Figure 11. Active Power Tracking Control Operation**

(a) DC-Link Voltage and Reference Value for VSC1

(b) Active Power, Reference Value and New Reference Value of VSC2

(c) Active Power, Reference Value for VSC1

Figure 11 (c) shows that the practical  $P_{vsc1}$  drops to near zero from 15 [kW]. At this time, when APTC is not applied, it can be seen that  $P_{vsc2}$  outputs -15 [MW] constantly. Therefore, Figure 11 (a), the DC-link voltage rises by more than 1 [kV]. However, when APTC method is used,  $P_{vsc2\_ref}$  can be instantaneously changed to  $P_{vsc2\_new\_ref}$  to suppress DC voltage rise.

#### 4.4. Discussion

VSC has a limited amount of reactive power and active power that can be converted. This is why the amount of active power decreases with reactive power supply during FRT operation. When reactive power is supplied, if the amount of active power is not reduced, the VSC may be overloaded and the VSC may be damaged. Figure 12 shows the P-Q curve when SFCL and APTC are applied or not. If APTC is not applied, it can be seen that the active power decreases and then increases again before the reactive power reaches 15 [MVar]. However, when APTC is applied, it can be seen that the active power decreases rapidly inversely with the increase of the reactive power. In this case, it can protect against overload and overvoltage of VSC. If SFCL is not applied, a variation of 10 [MW] occurs when Q is 10 [MVar]. However, when the SFCL is operated, the variation of P is reduced to about 5 [MW]. That is, it means that the variation of active power is reduced due to the DC-link voltage-stabilization.

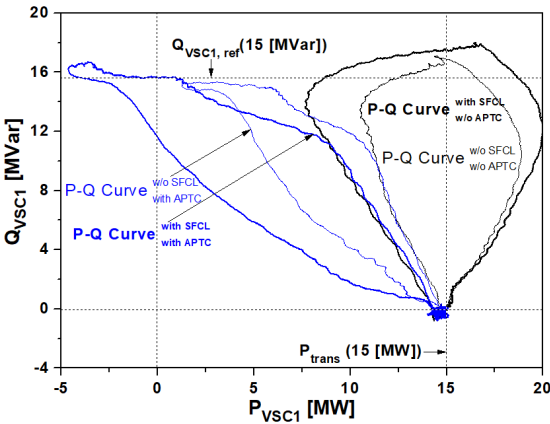


Figure 12. P-Q Curve about VSC1

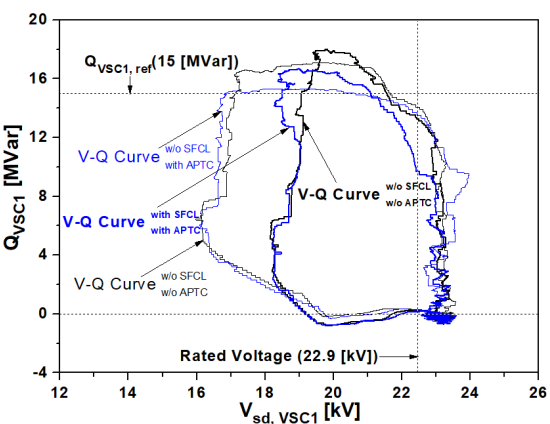


Figure 13. V-Q Curve about VSC1

Figure 13, the grid-side d-axis voltage on the x-axis and the reactive power on the y-axis are given. Normally, voltage is maintained at 21 [kV] and voltage drop occurs after the fault. When the voltage drops under 19 [kV], Q is supplied due to the FRT operation and the voltage drop is stopped. Since the operation of the SFCL has a direct effect on the voltage drop, the grid-side bus voltage drops less. Thus, the FRT capacity was enhanced and the VSC operation was stopped. APTC induces stabilization of the DC voltage, thereby preventing excessive supply of reactive power. The results indicate that the AC voltage changes little to the current.

5. Conclusions

In this paper, DC-link between grid and DG was implemented through voltage sourced converter modeling, and by newly proposing APTC and Trigger type SFCL, the FRT capacity was enhanced by suppression DC voltage rise and stabilization AC voltage drop. The APTC effectively and quickly suppresses the DC voltage rise than other solutions.

This paper confirms the following advantages

- When designing the SFCL, it is hard to protect the superconducting element. Therefore, adding SW to the superconducting element and connecting the CLR in parallel with these, the superconducting element could be protected and the limiting impedance can be increased. (Section 2.2, Section 4.2)
- The APTC is effective at suppressing DC voltage rise comparing to other methods; chopper resistor, de-loading method (Section 3)
- If the APTC does not operate, the reactive power and the active power may become large at the same time, causing the VSC to be overloaded and damaged. However, the APTC operation can prevent the overload of the VSC. (Section 4.4)
- FRT capacity could be greatly enhanced through applying trigger type SFCL, APTC operation was able to supply stable reactive power because DC voltage suppression and FRT capacity could be enhanced once more. (Section 4.2)

The application of the APTC the operation of the converter, making it economically more efficient than other methods and allowing for faster control than controlling the multiplying factor. In addition to the operation of the Trigger type SFCL, the capacity of the FRT greatly increased. On the other hand, the operation of the trigger type SFCL delayed the trip time of the overcurrent relay (OCR), and the OCR index correction is needed to solve this problem.

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**Appendix A**

**Table A1. Parameters for Simulation in whole System**

Item	Classification	Value	Unit
DC-link Constant	Rated Voltage	15	[kV]
	Cable Type	XLPE (ABB, July 2017)	
	Cable Impedance	0.022	[mΩ/km]
	Switching Frequency	1980	[Hz]
	VSC2 Control ( $P_{ref}/Q_{ref}$ )	15 / 0	[MW]/[MVar]
	VSC1 Control ( $V_{DC}/Q_{ref}$ )	15 / (0 or FRT)	[kV]/[MVar]
AC Grid Constant	Bus Voltage	154	[kV]
	MTR Ratio	154 / 22.9	-
	MTR Capacity	100	[MVA]
AC Distribution System Constant	Load	30 / 3(+inductive)	[MW]/[MVar]
	Line Type	CNCV/W 325	mm <sup>2</sup>
	Line Impedance	0.0939 + j0.1492	[Ω/km]
	Line length	$Z_{11} = 5, Z_{12} = 6$ $Z_{21} = 5, Z_{22} = 6$	[km]

**Table A2. Modeling Index of SFCL and OCR**

Item	Index	description	Value	Unit
OCR	$I_{pickup}$	pickup current of OCR	3.5	[kA]
	A	OCR Trip Index1	39.85	-
	B	OCR Trip Index2	1.084	-
	K	OCR Trip Index3	0	-
	Tr	OCR Reset Index	0.5	-
	p	Nonlinear Index for OCR trip	1.95	-
	q	Nonlinear Index for OCR reset	2	-
	TD	Time Dial	0.02	-
SFCL	$R_n$	Normal Voltage of SC	3	[Ω]
	$I_{critical}$	Critical Current of SC	3	[kA]
	$V_{SW}$	SW trip Voltage of SFCL	2	[kV]

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