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The Mixed Current Model of Nano-MOSFETs Considering the Effect of Horizontal and Vertical Electric Fields

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***Abstract*—A novel drive current model covering the effects of source/drain voltage (V_{DS}) and gate voltage (V_{GS}) and incorporating drift and diffusion current on the surface channel at the nano-node level, especially beyond 28nm node is presented. The effect of the diffusion current added is more satisfactory to describe the behavior of the drive current in nano-node MOSFETs, fabricated with the atomic-layer-deposition (ALD) technology. This breakthrough in model establishment can expose the long and short channel devices together. Introducing the variables of V_{DS} and V_{GS}, the mixed current model more effectively and meaningfully demonstrates the drive current of MOSFETs under the operation of horizontal, vertical, or mixed electrical field. In comparison between the simulation and experimental consequences, the electrical performance is impressive. The error between both is less than 1%, better than the empirical adjustment to issue a set of drive current models.**

***Index Terms*—drift current, diffusion current, mobility, nano-node, model, ALD technology.**

I. INTRODUCTION

In conventional device models for metal-oxide-semiconductor field-effect transistors (MOSFETs), the drive current [1,2] mainly considers the moving carriers with the drift effect. As the channel length of MOSFET keeps scaling down, the saturation current of MOSFETs raises up with the increase of the drain voltage or the decrease of the channel length. There are some published literatures to explain this phenomenon, such as channel length modulation [3-5] and velocity overshoot [6-9]. However, the proposed conduction mechanisms seem not fully to fit the physically measured current-voltage results well. To compensate this drawback, the device models in semiconductor foundries usually assist some empirical adjustment, but no physical meanings. Here, we propose a new concept incorporating the diffusion effect in each channel point due to the gradient of inversion charge density, especially near the pinch-off point. At this point, the inversion charge density traditionally approaches to zero, indicating the drift current zero, but the real drive current is not zero.

As a result, the drive current rises as the drain voltage increases for a nano-scale MOSFET. Adding the diffusion effect in drive-current model, the contribution of diffusion current in entire drive current is distinctly enhanced, especially in the current behavior of short channel devices [10]. In other words, a lager source/drain voltage V_{DS} will make a lager gradient of inversion charge density causing a larger surface diffusion current. However, the previous work only changing one parameter (V_{DS}) as V_{GS} fixed in long or short channel devices to fit the equivalent mobility μ_{eq} accurately was successfully finished. In this work, we furthermore propose a deeper consideration incorporating the modulation of all the parameters (V_{DS}, V_{GS} and L_{mask}) at one time to fit μ_{eq} correlated to V_{DS}, V_{GS} and channel length on drawn mask L_{mask}. Furthermore, consolidating the adjustment of V_{DS} and L_{mask} correlated to the horizontal electric field and V_{GS} influencing the vertical electric field, the drive current of MOSFETs is more meaningful and beneficial in providing a set of accurate nano-

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node device models, especially beyond 28nm node. The gate dielectric in this work was the sandwich stack of $HfO_x/ZrO_y/HfO_z$ deposited with the atomic layer deposition (ALD) technology. The physical thickness with ALD technology is about 24Å

II. II. Experimental and Fitting the Mobility

Based on the previous work [10], the carrier mobility μ(x) should be the function of the position x in the surface channel. But it seems not enough to describe the whole behavior of an equivalent mobility μ_{eq} correlated to V_{DS}, V_{GS}, and L_{mask}, independent of the position x. Incorporating the various conditions with V_{DS}, V_{GS} and L_{mask} is to reasonably describe the whole drive current and fit the μ_{eq} as shown in Eqs. (1)-(4):

$$I_{Drift} = Q_i(x) \times v_d(x) \times W \tag{1}$$

$$I_{Diff} = D_n \times \frac{dQ_i(x)}{dx} \times W \quad ; D_n = \mu_{eq} \times {kT}/{q} \tag{2}$$

$$\frac{I_{total}}{W} = I_{drift} + I_{diff} = -Q_i(x) \times v_d(x) + D_n \times \frac{dQ_i(x)}{dx} \tag{3}$$

$$\frac{I_{total}}{W} = -\frac{\mu_{eq} E_{sat} Q_i(x) \frac{dQ_i(x)}{dx}}{m C_{ox} E_{sat} + \frac{dQ_i(x)}{dx}} + D_n \times \frac{dQ_i(x)}{dx} \tag{4}$$

where q: unit charge, W: channel width, v_d: carrier drift velocity, D_n: diffusion coefficient of electron carrier, E_{sat}: horizontal electric field in saturation, k: Boltzmann constant, T: absolute temperature, and m: body factor.

Under the specific conditions such as fixing a channel length and tuning the gate voltages to sense the I_{DS}-V_{DS} characteristics, we can derive the relationship between the μ_{eq} and the drain bias, as shown in Fig. 1. Through changing the fixed channel length and the drain bias, the linear and saturation regions are obviously represented no matter what the tested channel device is. It is important to seek the accurate relationship between these three parameters and the μ_{eq}. In this work, there are four sections (a, b, c, d) illustrating long-short channel devices and linear-saturation regions split at L_{mask} = 120 nm due to the classification of electrical measurement, as shown in Table I.

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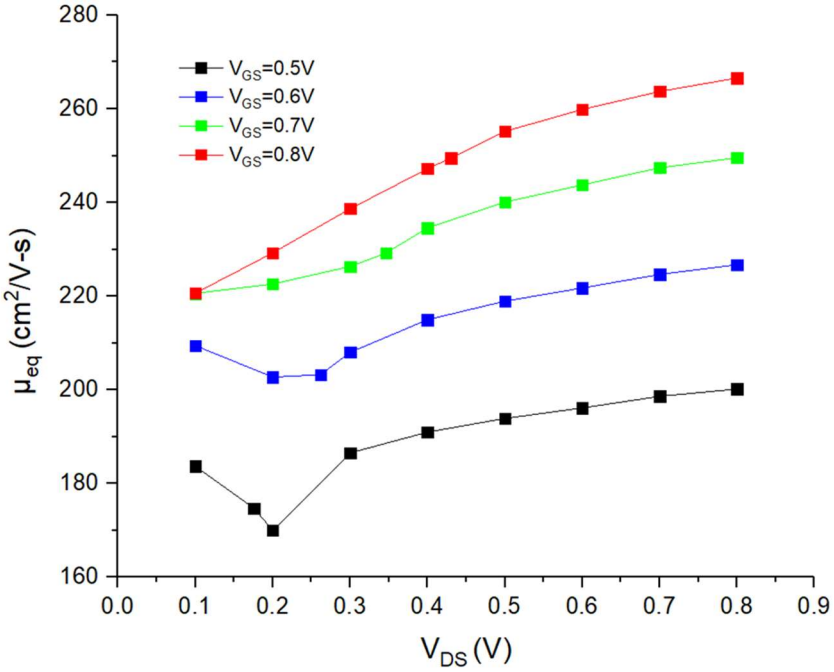

Fig. 1. μ_{eq} vs. V_{DS} under different V_{GS} at L_{mask} =500 nm in section a.

Table I. Four sections classified as long-short devices and linear-saturation regions.

Long channel (>120 nm), Linear region	*X*=a
Long channel (>120 nm), Saturation region	*X*=b
Short channel (< 120 nm), Linear region	*X*=c
Short channel (< 120 nm), Saturation region	*X*=d

First, the μ_{eq} can be written as a function of V_{DS} in different V_{GS} at fixed L_{mask}, which can be described by the Taylor expansion until the third-order polynomial, as shown in Eq.(5):

$$\mu_{eq}(V_{DS}) = \sum_{i=0}^{3} X_i \times (V_{DS})^i \quad (5)$$

where X_i is the coefficient of the i^{th} polynomial and i=0,1,2,3. *X* can be attributed as each section (a, b, c, or d).

Continuously, the X_i is strongly related to the gate voltages as L_{mask} fixed, which can be given as Eq.(6) with the Taylor expansion.

$$X_i(V_{GS}) = \sum_{j=0}^{3} X_{ij} \times (V_{GS})^j \quad (6)$$

where X_{ij} is the coefficient of V_{GS} polynomials with j=0,1,2,3.

Ultimately, the impact factor L_{mask} to the coefficient X_{ij} is entirely represented as Eq.(7):

$$X_{ij}(L_{mask}) = \sum_{k=0}^{2} X_{ijk} \times (L_{mask})^k \quad (7)$$

where X_{ijk} is the coefficient of L_{mask} variable with k=0,1,2.

The flow chart of *X*-coefficients and the μ_{eq} value in extraction is demonstrated in Fig.2 with section a as an example. The other sections in parameter extraction also follow the same procedures to achieve the accurate μ_{eq} value correlated to V_{DS}, V_{GS}, and L_{mask} variables. Table II demonstrates the full relationship of parameters and *X*-coefficients.

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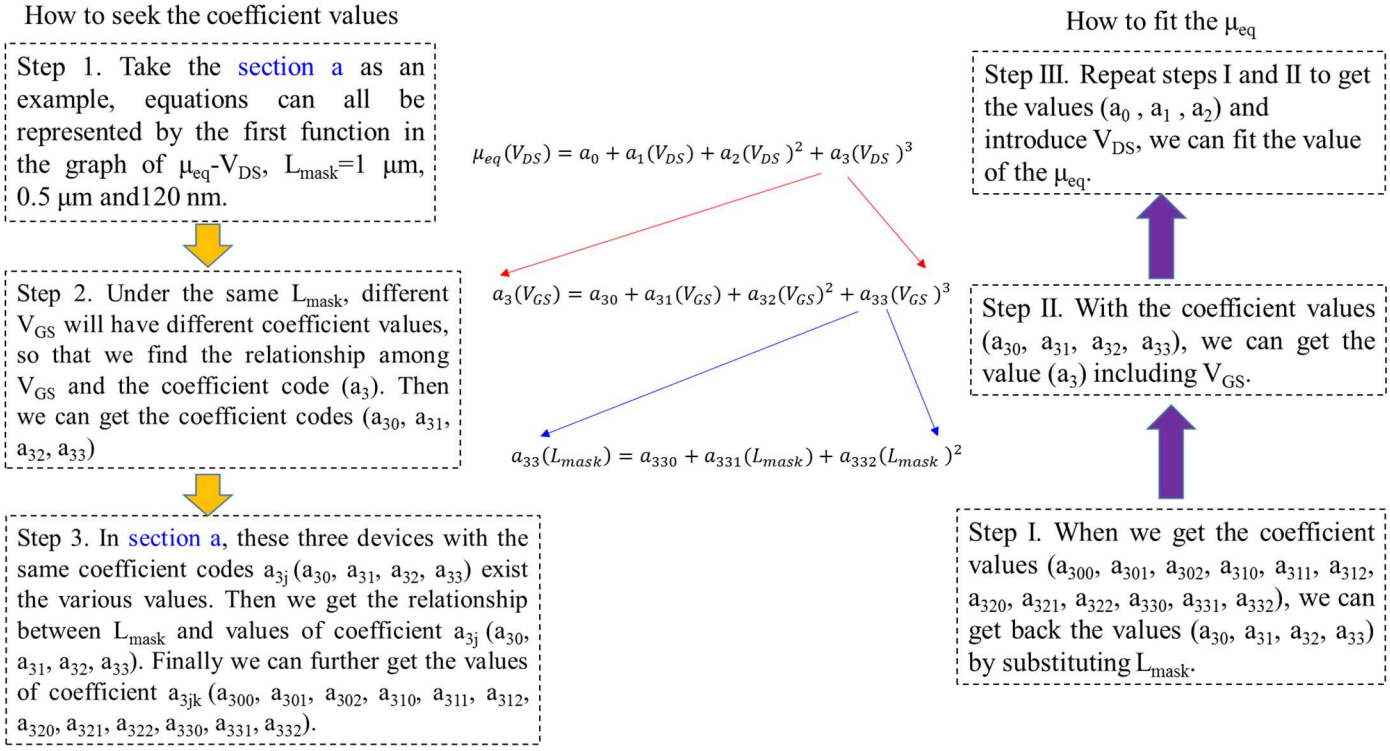

Fig. 2. The flow chart for extracting the coefficients and μ_{eq} values with section a as an example.

Table II. The relationship among each parameter and the coefficient in Taylor expansion.

The coefficient of μ_{eq} (V_{DS})	X_i : the functions of V_{GS} , i=0, 1, 2, 3
The coefficient of X_i (V_{GS})	X_{ij} : the functions of L_{mask}, j=0, 1, 2, 3
The coefficient of X_{ij} (L_{mask})	X_{ijk} : constant, k=0, 1, 2

III. III. RESULTS AND DISCUSSION

Following the last flow chart to obtain the coefficients (X_i, X_{ij}, X_{ijk}), the μ_{eq}(V_{DS}, V_{GS}, L_{mask}) at any condition can be effectively and meaningfully extracted. After that, the equivalent mobility will be immediately substituted into (4) to do the simulation of the corresponding drive current. The simulation and experimental results of I-V curves with long and short channel devices represented as four sections are shown in Fig. 3.

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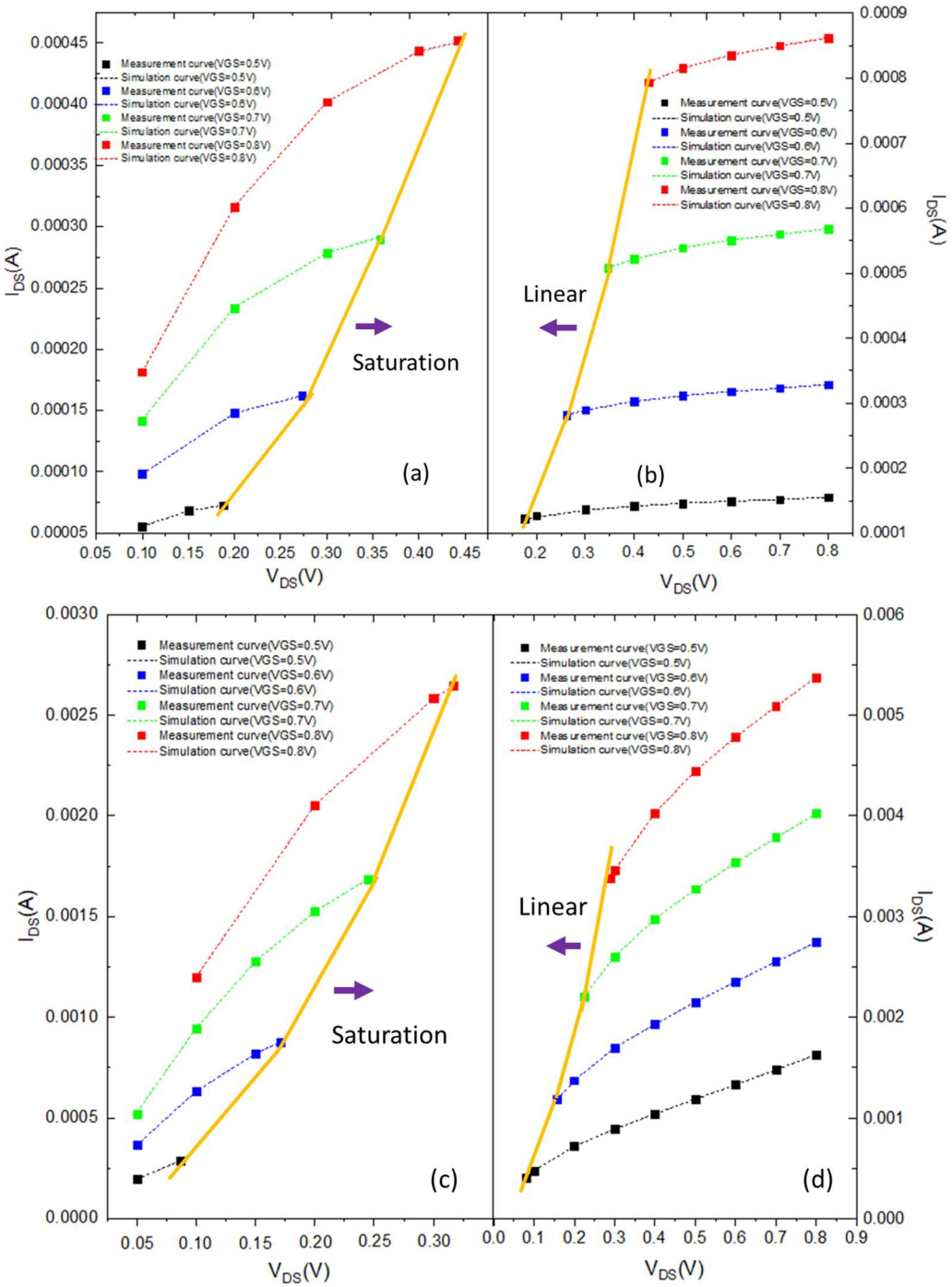

Fig. 3. I_{DS} vs. V_{DS} curves for long-channel devices: (a) at L_{mask}= 1 μm in section a and (b) at L_{mask}= 500 nm in section b; for short-channel devices: (c) at L_{mask}= 50 nm in section c and (d) at L_{mask}= 33 nm in section d.

For precise observation of the contribution of the μ_{eq} correlated to V_{DS}, V_{GS}, and L_{mask}, one 3-D plot is established and shown in Fig. 4, combining all of these extracted data linked as lines and extended these lines as a continuous plane.

In this study, the tested channel-length devices contain 33, 50, 90, 120, 500 nm and 1 μm. As the channel length L is greater than 120 nm, the section is defined as the long-channel section. Thus, the plot in Fig.4 with L= 500 nm is represented as long-channel section and with L= 33 nm as short-channel one. Furthermore, the V_{DS} and V_{GS} sensed are 0.1, 0.2…, 0.8 V and 0.5, 0.6, 0.7, 0.8 V, respectively. The error between simulation and real measurement data is less than 1% no matter what the channel-length devices and the

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operation mode at linear or saturation region are. Table III is an example to extract the coefficients in section a under V_{GS}= 0.8 V and L_{mask}= 500 nm.

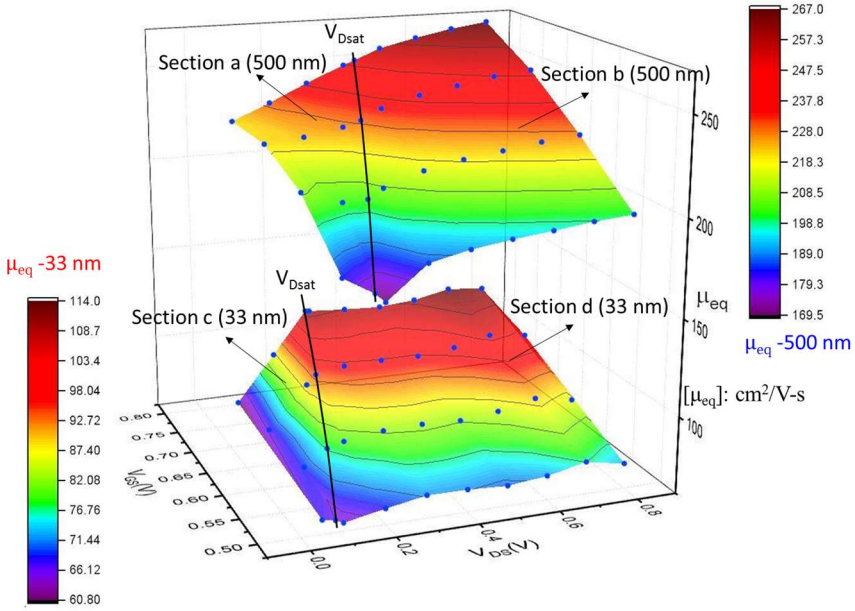

Fig. 4. Three dimensions of μ_{eq} versus V_{DS} and V_{GS} at L_{mask} =500 nm (long-channel) and 33 nm (short-channel).

Table III. The values of coefficients in section a under V_{GS}= 0.8 V and L_{mask} = 500 nm.

The value of a_3	a_3= -247.999
The values of a_{3j}	a_{33}= 19833.33 a_{32}= -5150 a_{31}= -29383.3 a_{30}= 16400
The values of a_{3jk}	a332= -3283858.592 a331= 5452922.151 a330= -1885663.094 a322= 6422679 a321= -10725100.45 a320= 3751730.477 a312= -4094362.073 a311= 6889789.134 a310= -2450687.382 a302= 840872.7189 a301= -1430708.191 a300= 521535.9158

IV. IV. CONCLUSION

Without considering the effect of channel length modulation and drift velocity overshoot, the mixed current model, including surface drift and diffusion current, has been announced to describe the electrical behavior of drive current of nano-node MOSFETs. The existence of diffusion current addresses why the drive current enters the saturation region, but not zero at the pinch-off point. The diffusion contribution in drive current becomes more apparent, especially for short-channel MOSFETs. For devices in normal operation, the

parameters (V_{DS}, V_{GS}, and L_{mask}) independent of channel poistion are strongly correlated to the μ_{eq} value. Investigating the mutual interaction among them is indeed necessary. This work successfully provides the physical and meaningful consequences for nano-node MOSFET devices, fabricated with the ALD technology. The error between simulation and experimental results is less than 1%, which is more suitable to the 28nm devices or beyond to build up a more accurate set of device model in circuit design consideration.

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