Back-end-of-the-line MEMS switches for power management, ESD and security

Nusrat Tazin, Daniel G. Saab, and Massood Tabib-Azar

***Abstract*— This paper discusses a MEMS switch that can be fabricated using low temperature (<100ºC) deposition and patterning techniques suitable for the back-end-of-the-line integration with CMOS. The resulting cross-bar switches can be used for electrostatic discharge protection, FPGA implementation, chip security assessment and lock-down, and circuit block power management. We discuss platinum and iron switch with turn-on voltages of ~ 1.8 V. In the case of the iron switches, we also show that they can be magnetized to have "memory" and stay on when turned on. Platinum switch cycling of up to 1000 times did not show any changes in their turn-on voltage and their contact resistance was unchanged. The 10-100 nm switch airgaps were formed using low temperature sputtered sacrificial polysilicon and XeF_2 etching. XeF_2 does not attack any of the metals used in CMOS enabling fabrication of cross-bar switches with any of these metals. Once activated, it takes ∼ 6 µs to mechanically turn on the switch that can be decreased to ~1 ns by optimizing the device structure. Interestingly, the nm-scale gaps can be used as spark gap as a fast plasma switch to discharge first followed by the activation of the MEMS switch.**

***Index Terms*—Microelectromechanical systems (MEMS), Electrostatic Discharge (ESD), Back-end-of-line (BEOL), Memory Switch**

I. Introduction

Scaling of electronics has resulted in integrated circuits with enhanced sensitivity to the electrostatic discharge (ESD) and larger leakage power. The migration of the manufacturing of these circuits to other countries has resulted in concerns regarding chip security. Many solutions to address these concerns exist and constantly are being developed; each with its own strengths and shortcomings. Here, we explore the feasibility of microelectromechanical (MEMS) switches to address ESD and discuss its possible applications in chip security, field-programmable gate arrays (FPGA), and chip power management. The most important advantages of MEMS switches are [1][2][3][4] : 1) they can be fabricated using very low temperature deposition and patterning steps, 2) their turn-on voltage can be easily adjusted by adjusting their structure and 1 V, 1 GHz switches are demonstrated in [4], 3) they can have very low (<1 mΩ) "on" resistance and very low leakage current (<10^{-12} A), 4) they can have built-in memory as we show in this work, 5) they can be designed to have many contacts in the same device resulting in unique functionalities in a single device [1], and 6) their parasitic capacitance, resistance and inductance can be an order of magnitude smaller than the silicon devices. On the other hand, a) owing to their moving parts they are not as reliable as silicon electronic devices, b) they tend to be slower, and c) their structures may require air gaps and mechanical structures reducing their fabrication yield.

In electrostatic discharge events the amount of damage experienced by an integrated circuit is due to excessive gradient of voltage and current densities inside the device and circuit [5][6][7][8]. Schottky diode-based silicon-controlled rectifier is used in most electronics to mitigate ESD. When ESD voltage exceeds the actuation voltage of the Schottky diode, it shunts the transient current to the ground. Its actuation voltage can be as low as 0.6 V [5] with switching time reported in [9] as ∼ 7.8 ns . The problems associated with these devices are their low reverse voltage rating and high reverse leakage current that increases at higher temperatures. Higher forward bias voltage increases the reverse voltage rating [5]. Schottky diode-based SCR has high tolerance characteristics and the circuit design has been modified several times to improve its performance [10][11]. However, for application specific voltage requirement, the design parameters are needed to be adjusted which increases the size of the ESD device and circuit [12]. The interactions between the core IC circuit and the protection circuit for such devices are complex and the characterization and inclusion of parasitic effect in designing the IC is a requirement [12].

Simple MEMS on/off switches have been reported since 60's [13]. MEMS switches have virtually zero leakage current, no sub-threshold conduction [14][15][1], possibility to integrate in the same chip with CMOS circuits, scalability and ability to perform reliably in harsh environments like high temperatures and in high ionizing radiation (I-R). It also provides advantage on power management for very large scale integrated circuits (VLSI) [1], programming interconnect in FPGAs [2], [16] and biomedical applications where reduction of leakage power is desirable for prolong battery life [17]. MEMS switches can also be used for ESD protection. Changing the geometry and the material of the MEMS switch one can modify their speed and turn-on voltage. Whereas, for SCR devices, changing its turn-on voltage requires alteration of design parameters [8]. MEMS FPGAs also have simpler architecture [18]. It is also shown that MEMS can be used for power gating to VLSI chip [19].

In this paper a very simple vertical MEMS switch is discussed that is composed of a cross bar structure with two metal plates with a gap between them. The bottom electrode is fixed, and the top bridge deforms when actuated by an applied voltage. The 3D and 2D structure of the proposed switch is presented in Fig. 1 along with an optical image of

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microfabricated switch. The cross-bar device was fabricated using a Back end of the line (BEOL) compatible VLSI process because of the advantage it provides compared to the conventional process [20]. With this process, devices can be fabricated at low temperature to avoid degrading the underlying VLSI performance [21].

Section II describes the geometrical modelling of the switch including design specifications and design parameters. Section III presents the design of the switch, pull-in voltage analysis, characteristics of the memory switch and temperature dependence of pull-in voltage. Section IV explains the experimental results including the fabrication process, I-V and switching characteristics of the memory switch. Section V includes the characteristics of MEMS switch for reducing power in FPGA and improving its speed. Section VI represents the modelling of MEMS switch for power management and power gating. The MEMS switch can also be used to for security purposes as discussed in Section VII. Conclusions are presented in Section VIII.

II. GEOMETRICAL MODELLING

A. Design Specifications

COMSOL Multiphysics analysis was used to simulate the electro-mechanical properties of the cross-bar switch. The length, width and the thickness of the beam were varied to optimize switch voltage and speed. The bottom stationary electrode can be any thickness down to 0.3 nm graphene. The gap between the beam and the bottom electrode ranged from 10 nm to 200 nm. The structure is similar to a fixed-fixed bridge shunt switch discussed in the literature [22] . We used different metals including platinum and iron that were also fabricated. The important properties of the platinum and iron are given in Table I.

B. Design Parameters

The fixed electrode and the top movable bridge create parallel plate capacitance which results in electrostatic actuation. The electrostatic force developed in the beam is given by [22]:

$$F = \frac{\varepsilon_0 \varepsilon_r A V^2}{2{g_0}^2} \quad (1)$$

where V is the actuation voltage, g_0 is the gap between two electrodes and A is the area of the plate. ε_0 *is* permittivity of vacuum and ε_r is relative permittivity of the material. The pull-in voltage is

$$V_{pull-in} = \sqrt{\frac{8k{g_0}^3}{27A\varepsilon_0}}, \quad (1)$$

where, "k" is the spring constant of the beam given by:

$$k = {2Ewt^3}/{3l^3}, \quad (2)$$

where, E= Young's modulus in Pa, l is the length of the beam, w is the width of the cantilever, and t is the thickness of the beam.

Switching time of such switch can be derived as [23]

$$t_s \approx 3.67 \frac{V_{pull-in}}{V_{supply}\omega_0} \quad (3)$$

Here, t_s= switching time, V_{supply}= supply voltage and ω_0= resonant frequency.

TABLE I
PROPERTIES OF MATERIALS OF BOTH ELECTRODE.

Material	Platinum	Iron
Poisson ratio	0.38	0.29
Young's modulus	168GPa	200 GPa
Density	21450 Kg/m^3	7870 Kg/m^3

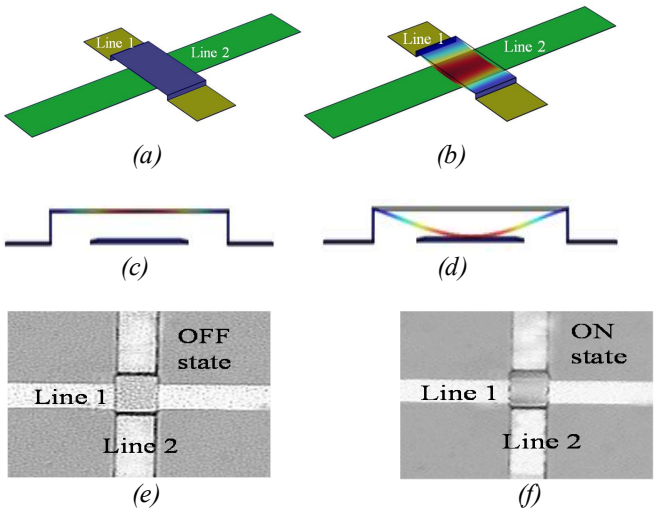

Fig. 1: a) 3D rendering of the OFF state of the cross-bar switch, b) its ON state; c) and d) their corresponding 2D renderings. e) and f) Optical images of a microfabricated platinum cross-bar switch in "off" and "on" states with switching areas of 10μm x 10μm

C. Pull-In voltage analysis

The pull-in voltage analysis of the switch structure with different lengths, widths and thickness is shown in Fig. *2*.

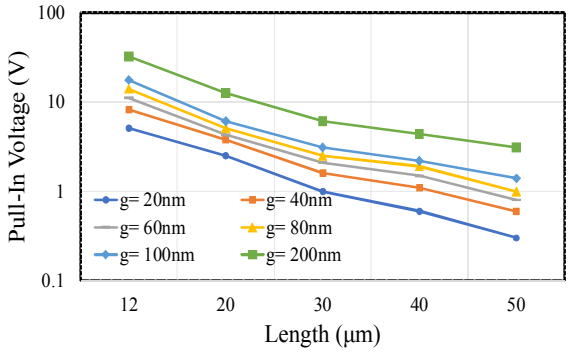

Fig. 2: Design calculations on pull in voltage and length of the beam based on COMSOL simulations on for gap height from 20nm to 200nm.

The data in fig. 2 indicate that with the increase of the length of the beam, the pull-in voltage decreases. For 12 μm length and 200 nm gap, the pull-in voltage was 32.3 V whereas for 50 μm and 200 nm gap the pull-in voltage was reduced to 3.1 V.

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For 50 µm long, 0.1 µm thick top electrode or bridge, we calculated the pull-in voltages for different widths: 10 μm , 15 μm and 20 µm as shown in Fig. 3. The pull-in voltage increases with the increase of the beam width as expected. For 10 μm width and gap of 200 nm, the pull-in voltage was 3.1 V, whereas for 20 μm width and 200 nm gap, the pull-in voltage increased to 3.7 V. Similar situations can be observed for the thickness of the beam as shown in Fig. 4 where analysis was performed for fixed width of 10 μm and length of 50 μm and by varying the thickness from 0.1 μm to 0.7 μm. The pull-in voltage increased with thickness of the beam. For 0.1 μm thickness and 200 nm gap, the pull-in voltage was 3.1 V and for 0.7 µm thickness and 200 nm gap, the pull in voltage was increased up to 131.8 V.

Similar analysis can be performed considering other materials: tungsten, aluminum, iron and copper. As these materials exhibits different properties like Young's modulus and material density, they provide different pull in performances shown in Fig. 5. For 200 nm gap, tungsten pull-in voltage was 3.8 V, whereas, other materials such as aluminum, copper, iron and platinum, had pull-in voltages of 1.6 V, 2.3 V, 2.6 V and 3.1 V, respectively. The upper mentioned analysis is performed using COMSOL Multiphysics.

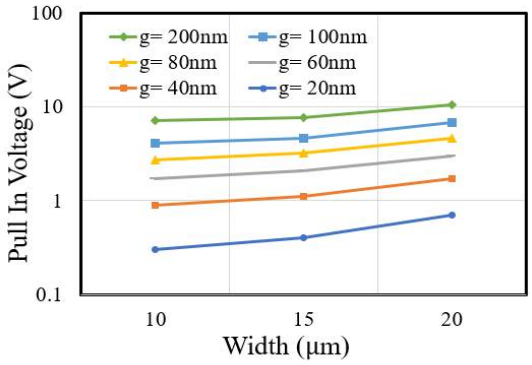

Fig. 3: Simulated pull-in voltages versus the width of the platinum switch bridge.

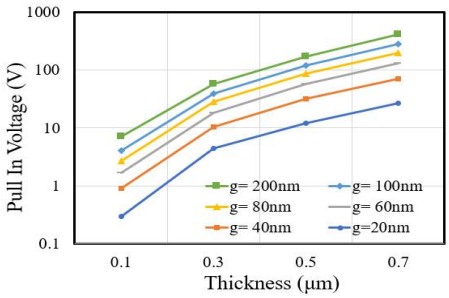

Fig. 4: Simulated pull-in voltages versus the thickness of the platinum switch bridge.

The turn-on time is also very important in ESD protection which can be found by Equation (3). Fig. 6 shows switching time for the platinum 10 µm long and 0.1 µm thick cross-bar switch calculated using COMSOL Multiphysics. For 50 μm long bridge, the switching time was 5.89 μs, whereas for 12 μm long bridge, the time is reduced to 0.17 μs. Tungsten switch with electrode dimensions of 10 μm × 1 μm × 0.1 μm and the bridge dimensions of 2 μm × 3 μm × 0.1 μm, has a switching time of 7.62 ns calculated using COMSOL Multiphysics which is comparable to the ESD protection device presented in [9].

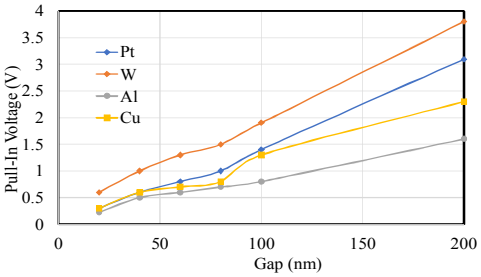

Fig. 5: Simulated pull-in voltage for Pt, W, Al, Fe and Cu bridges as a function of gap.

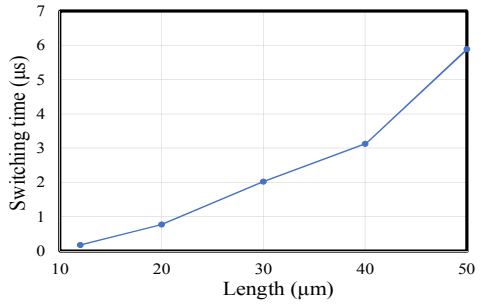

Fig. 6: Simulated switching time vs platinum bridge length.

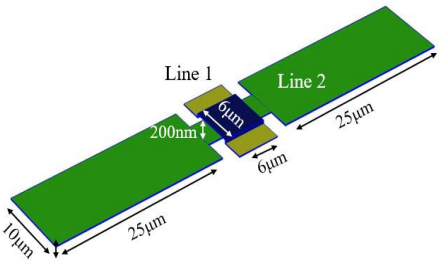

Fig. 7: Proposed switch structure with rescaled dimensions to improve speed and reduce the turn-on voltage.

Materials with lower Young's moduli can reduce the actuation voltage. Aluminum switch with 2 μm × 3 μm × 0.05 μm bridge dimensions and 20 nm gap has pull-in voltage of 18 V and switching time of 9.98 ns. The performance can be further improved by taking the dimension of the bottom electrode as 10 µm × 1 µm × 0.03 µm and bridge dimensions to be 2 µm × 1 µm × 0.03 µm. The pull-in voltage in this case was reduced to 4 V and switching time became 17 ns. Therefore, changing the material and scaling the structure one can simultaneously reach the switching time and actuation voltage for ESD protection. With reducing bridge dimensions, the structure of the switch can be considered like Fig. 7 where the contact area is reduced.

D. Characteristics of the Memory Switch

Ferromagnetic materials such iron can be used to fabricate memory switches. When the top and bottom electrode of the

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iron switch are magnetized, the following forces are generated at equilibrium.

$$F_E = F_{ES} + F_M \quad (4)$$

where F_{ES} is the electrostatic force that generated due to the electrostatic actuation voltage and presented in (1) and F_M is the magnetic force experienced by the top electrode. When both the top and bottom electrodes are magnetized with remnant magnetic fields of B_{r1} ($=\frac{2\mu_0 m_1}{3V}$, where μ_0 is the permeability of the free space and V is the volume of the magnetized bridge) and B_{r2} (bottom electrode), the force between them is given by [24]:

$$\boldsymbol{F_M = \nabla(m.B_{r1}) = (\frac{3V}{2\mu_0})\,\nabla(B_{r2}.B_{r1})} \quad (5)$$

The force between two magnetized surfaces separated by a small gap "g_0" (much smaller than the length and the width of the plates) and assuming that there are no fringing fields, is given by:

$$F_M = \frac{B_{r1}B_{r2}A}{2\mu_0} \quad (6)$$

For this case the F_m does not depend on the gap distance. However, the COMSOL simulation shows that at small gaps approaching 40-20 nm, the fringing fields increase the magnetic force as shown in Fig. 8. In this simulation the remnant magnetization of the top and bottom electrodes were 1 mT. The electrostatic actuation brings the top bridge close to the bottom electrode and the existing magnetic field causes them to stick. When $F_M \geq F_E$ at g_0, the top bridge will stick to the bottom electrode. To un-stuck them, one can either demagnetize them or apply an opposing magnetic pulse or use a see-saw structure discussed later in this manuscript.

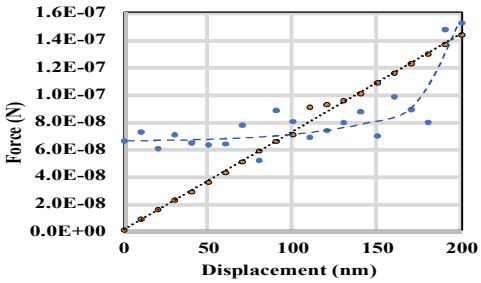

Fig. 8: Elastic and magnetostatic components of the force vs displacement for the magnetized switch. At 200 nm displacement, the bridge can stick to the ground electrode because of the magnetic force.

For small displacements, F_E is simply given by: $F_E = -k\,(g_0 - g)$, where, k is the spring constant and $g_0 - g$ is the displacement due to the acting electrostatic force: g_0 is the gap at zero applied voltage and "g" is the gap at applied voltage V (i.e., g=g_0 when V=0). For small displacements, the spring constant is a constant related to the Young's modulus of the bridge material, its dimensions, and its built-in residual stress. As the gap becomes smaller, it can be shown that the "effective" spring constant (k_e) is given by: $k_e = k\left(1 - \frac{\varepsilon_0 A V^2}{g^3}\right)$. Thus, F_E becomes: $F_E = -k_e\,x$.

In the constant voltage actuation scheme, it is important to note that at g=2g_0/3 the bridge becomes unstable and collapses and contacts the bottom electrode. Similar spring softening also occurs for magnetic actuation with coils excited with constant voltage source. However, in the above example we do not increase the magnetic field to actuate the bridge. We use the existing magnetization in the bridge and bottom electrode to cause stiction between them when they are brought together by the electrostatic actuation. Thus, when $F_{ES} + F_M > F_E$, the top electrode collapses and touches the bottom electrode. For the switch to act as a memory switch, the condition $F_M \geq F_E$ must be maintained for which the switch will stay "ON" even after removing the electrostatic force.

E. Effect of Temperature on the Turn-On Voltage

Thermal effects [25] are particularly important in ESD and other security and power management applications. Unlike semiconductor devices where thermal run-away can cause device melt-down, MEMS switches do not experience thermal run-away but their turn-on voltage and speed can change as a function of temperature as discussed here. Fig. 9 shows the effect of temperature on stresses and dimensional changes of the al the parts of the bridge switch. Stresses for the bridge and its supports can be summarized as:

$$\sigma_{L_1} = \alpha\Delta T E \quad (7)$$

$$\sigma_{L_2} = tan^{-1}\left(\frac{\alpha\Delta T L_1/_2}{L_2(1+\alpha\Delta T)}\right)\frac{E}{2(1+\vartheta)} + \alpha\Delta T E \quad (8)$$

$$\sigma_{L_2} = tan^{-1}\left(\frac{\alpha\Delta T L_1/_2}{L_3(1+\alpha\Delta T)}\right)\frac{E}{2(1+\vartheta)} + \alpha\Delta T E \quad (9)$$

where, ϑ is the Poisson ratio, α is the coefficient of thermal expansion, ΔT is the change in temperature and E is the Young's modulus. L_1 is the length of the top electrode. L_2 and L_3 are the length of the support beams or side beams.

We then solve for the Young moduli:

$$E = \frac{\sigma_{L_1}}{\alpha\Delta T} \quad (10)$$

$$E = \frac{\sigma_{L_2}}{tan^{-1}\left(\frac{\alpha\Delta T L_1/_2}{L_2(1+\alpha\Delta T)}\right)\frac{1}{2(1+\vartheta)} + \alpha\Delta T} \quad (11)$$

$$E = \frac{\sigma_{L_2}}{tan^{-1}\left(\frac{\alpha\Delta T L_1/_2}{L_3(1+\alpha\Delta T)}\right)\frac{1}{2(1+\vartheta)} + \alpha\Delta T} \quad (12)$$

Equations (10)-(12) show that the Young's modulus of the beam is proportional to the tangent of 1/ΔT. The relation between temperature and strain can be simulated using MATLAB and the results are shown in Fig.10.

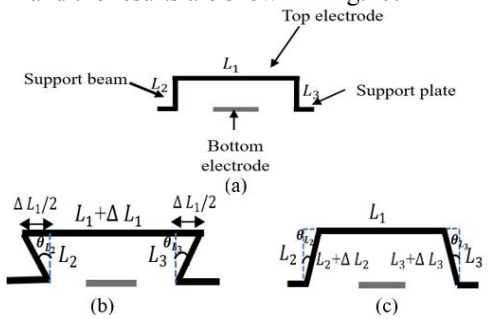

Fig. 9: Shape of the beam due to temperature change (a) the original structure, (b) the length of the top electrode increases, and (c) the length of the support beam increases.

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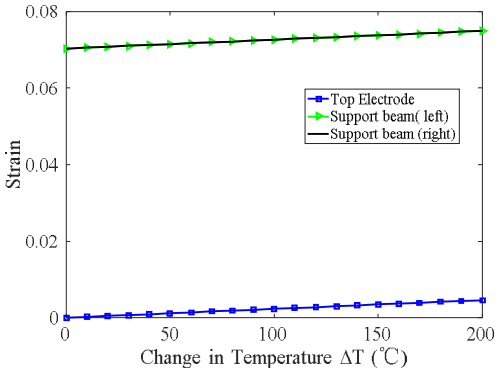

Fig. 10: Strain vs temperature for aluminum beam.

Here, for the simulation presented in Fig. 10 and Fig. 11, we used aluminum with Length of the top electrode=L_1=50μm , Width of the top electrode=W=10 μm and thickness=t=100 nm for the switch and the temperature was varied from 0℃-200℃. The length of the side beams are considered as L_2=L_3= 0.3 μm It can be observed from Fig. 10, that with the increase of the temperature the strain on the electrodes increases. Moreover, the relation between temperature and the pull-in voltage was also simulated using COMSOL in Fig. 11 where the pull-in voltage decreased with temperature. Variation of the pull-in voltage from 0 ℃ to 100 ℃ was less than 0.1% which provides better thermal stability compared to Schottky diode [26].

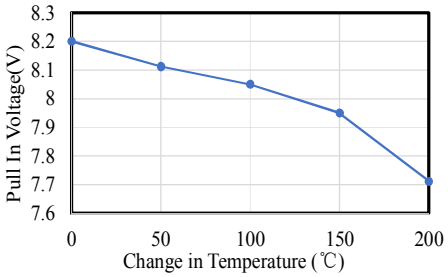

Fig. 11: Pull-in voltage vs temperature for the aluminum beam.

III. Experimental Results

A. Fabrication Process

The above devices were fabricated using a simple 2-mask process using sputtered platinum at 50 W at < 2 µTorr pressures. The first step of fabrication involved deposition of silicon nitride passivation layer for the protection of the substrate. Then, using the sputtering technique, platinum was deposited and patterned as the bottom electrode. Then, a sacrificial polysilicon layer was added. Next, the second metal was sputtered and patterned to form the bridge. Upon $XeFe_2$ etching of the sacrificial layer, the top metal was freed to form the bridge. Important steps of the fabrication process are shown in Fig. 12.

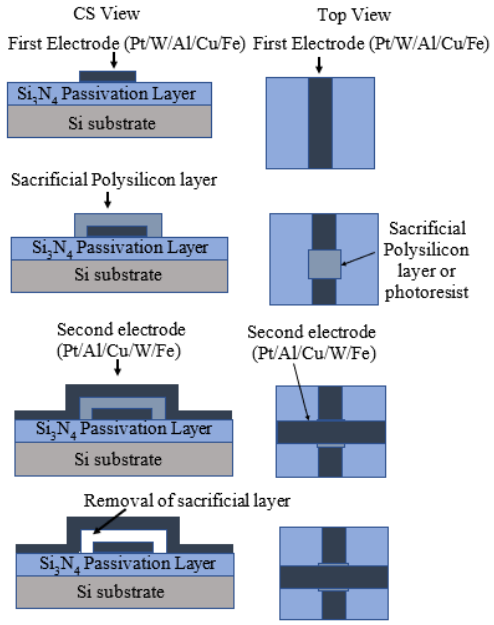

Fig. 12: Fabrication process outline.

B. I-V curve and contact resistance

Fig. 13 shows the I-Vs of the 100 nm gap device. The evolution of the contact resistance in the thin film for platinum has been studied in [27] and the results are summarized in Fig. 13. **Error! Reference source not found.** The measured contact resistance in the "on" state was on the order of 4 mΩ for up to 1000 cycles.

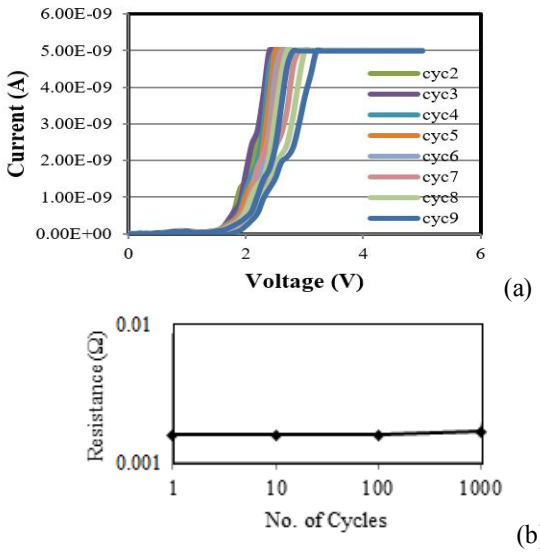

Fig. 13: a) I-V Cycling measurements on 100 nm gap devices. V_{PI} ~ 2 V. b) Contact resistance evolution of Pt over 1000 I-V cycles. Contact area was ~ 25 nm^2.

The above switch can be used for ESD and can be designed to have almost any turn-on voltage in the range of ~ 0.1 V up to 100's of volts. Its speed is currently at 1 µs and can be improved by optimizing its structure [4]. We also note that its gap can be used as a spark gap [28] and discharge electrostatic voltages in excess of a few thousand volts over very short time without

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degradation. This property of the switch can be advantageously used to circumvent the slow speed of its mechanical part.

C. Switching Characteristics of Magnetic Switch

I-V characteristics of the magnetic memory switch is presented in Fig.14. When the switch is magnetized the top and bottom electrode latch on to each other and form a non-volatile switch. To turn-off the device, one can use a current pulse to heat-up or to apply an opposite field.

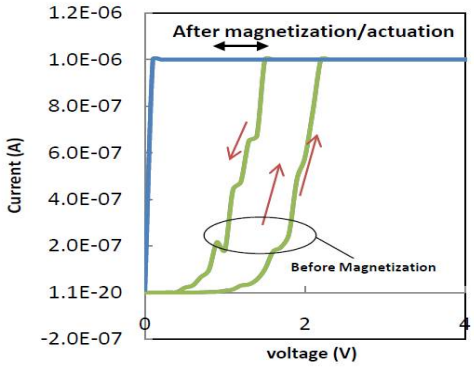

Fig. 14: Switching and latching characteristics of magnetic memory switch.

IV. FPGA WITH CROSS-BAR SWITCHES

FPGAs are in-the field programmable devices which can implement any complex digital circuit providing efficient and real time computing. However, it has disadvantages like requirement of large static RAM (SRAM) for configuration of data. Scaling down of nodes creates single-event upset (SEU) or soft error problem and large current leakage which shows high temperature dependence. A nanobridge-based FPGA is presented in [18] to address the problem of high temperature environment which is nonvolatile, SEU-free and have the structure of complementary atom switch (CAS) exhibiting reliable OFF state and low voltage.

We have constructed an island style FPGA framework containing logic blocks, switch boxes, connection boxes, routing tracks and configuration registers made up of SRAM cells presented in Fig. 15 [29] in order to perform accurate comparative evaluation of Hybrid N architectures with CMOS architectures at spice level. Routing tracks are the individual vertical and horizontal line segments that run throughout the FPGA architecture. These routing tracks are grouped together in channels and number of routing tracks present in each channel is determined by the channel width (Wc) which remains identical in X and Y directions in uniform FPGAs. Connection blocks connect the logic blocks to Fc number of tracks in the channel. Switch blocks connect the logic elements by connecting appropriate horizontal and vertical tracks. Fs specify max number of other tracks that each track can connect to. A logic block (as in Fig. 16 (a)) is made up of interconnection switch matrix and N number of basic logic elements (BLEs). Interconnection matrix performs connections between BLEs during logic implementation. A BLE whose size is given by K is constructed out of a K-input LUT and a DFF to generate a registered and unregistered output. The interconnection matrix can be implemented using cross-bar switches.

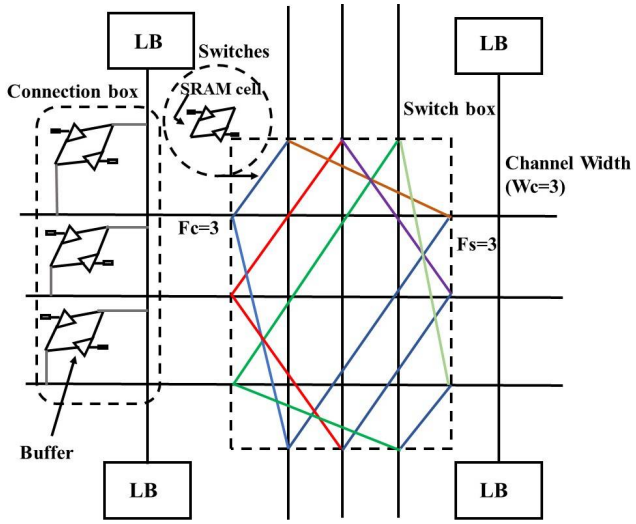

Fig. 15: Uniform, Bi-directional and island style FPGA [27].

Design Architect of Mentor Graphics has been used to draw the schematics of FPGA components and ELDO spice simulator is used for simulations. Fig. 17 illustrates a 4 input LUT design used in BLE which consists of a decoder, 16X1 SRAM cells and a multiplexer network. Inputs to LUT are decoded to select an SRAM cell in to which data is written during WRITE operation. During READ operation, WRITE port of SRAM cell (W) is logic '0' and data from READ port (R) of corresponding memory cell, determined by decoded multiplexer control signals is driven on to LUTs 'OUT' port.

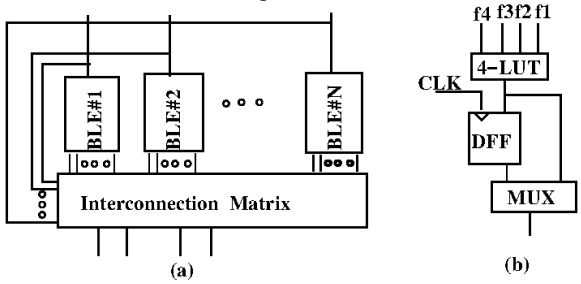

Fig.16: a) Logic block design and b) BLE design.

FPGA MEM/CMOS architectures containing switch and LUT blocks offers several advantages including: 1) reduced routing leakage power consumption, 2) improved critical path delay since MEM device "ON" resistance is x100 less than CMOS device. This enables MEM/CMOS FPGA to operate at extremely low power. MEMS in the switch block are used only during configuration and remain in the same state during FPGA operation improving the FPGA speed. MEMS FPGA switch blocks do not need SRAM where keeps the the switch configuration. Therefore, switch modules in reconfigurable architecture can be developed using MEMS significantly higher integration density, lower power and faster speed. MEMS switch block once configured can retain its state permanently. Configuration of MEM (T_{config}) is around 1 ms found from simulation and which is faster than the time achievable with CMOS(5-6ms)[30] and if $T_{config} > T_{write}$ (SRAM loading time),

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usage of MEM can increase configuration time proportional to the difference of T_{write} (as observed with baseline CMOS FPGAs) and T_{config}.

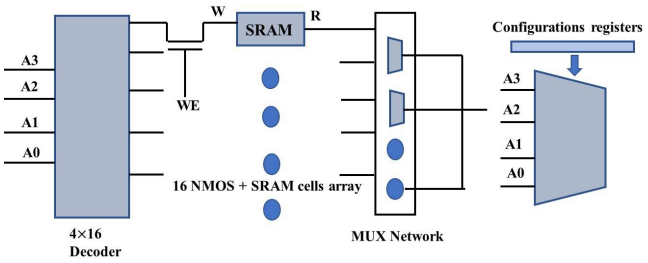

Fig. 17: (a) Modeling of 4 input LUT and (b) LUT block diagram.

A. *Fast Energy Efficient MEM/CMOS FPGAs*

The proposed energy efficient MEM/CMOS FPGA contains MEM based switch blocks and CMOS CLB's design identical to baseline CMOS FPGAs. Bi-directional FPGAs which employ tristate buffers as routing switches are used in our experiments.

We performed comparative study of baseline CMOS FPGAs and hybrid MEM/CMOS FPGAs at spice level (low level) and architectural level (high level) in two phases. First, we performed low level analysis using spice and compares power and delay results obtained with high level analysis performed using VPR5.0 framework. Spice simulations provide base framework to evaluate hybrid FPGA vis-a-vis CMOS FPGA and establishes the accuracy of results obtained using VPR. Next, we evaluated the FPGAs using VPR 5.0 framework [31].

We first developed a spice model of CMOS FPGA framework using above mentioned components with K (LUT size) = 4, N (Number of logic blocks in a CLB). Power and delay analysis is carried out in each instance for varying number of logic blocks in FPGA using ELDO spice and 180nm technology. For the hybrid MEM/CMOS architectures, equivalent spice level description netlist is generated. Results obtained from Hybrid MEM/CMOS simulator are integrated with CMOS observations to analyze power and delay measurements.

We next used the VPR 5.0 [31] framework which has integrated power, area and delay model is used in our analysis. This power model uses transition density and static probability information of a signal to compute the dynamic power. Short circuit power is calculated as a percentage of dynamic power which is one of the parameters in architecture file. Input signal probability is assumed to be 0.5 and transition probability of 0.5. VPR analysis is based on values supplied through architecture files which make it flexible for usage across FPGAs with varying LUT sizes (K) and CLB sizes (N), switch block and connection block designs. Parameters concerning propagation delay through LUTs, IOBs, switch blocks and connection blocks, present in architecture file are updated with values derived from ELDO spice. VPR 5.0 [31] takes in architecture file describing FPGA framework, a netlist describing digital circuit implementation using CLBs, activity information of each net in the circuit and a function generator.

VPR was developed for evaluation of CMOS FPGAs and to account for MEM characteristics in the MEM/CMOS FPGAs, modules concerning leakage power and switch block power are modified accordingly in the power model. MEM switch block parameters mentioned in Table II are introduced in architecture files to take the effect of usage of MEM.

TABLE II
SWITCH BLOCK PARAMETERS

S.NO	Switch Parameters	Value Used
1	Resistance	1mΩ
2	C_{in}	1fF
3	C_{out}	0

It was observed that on an average routing energy was reduced by 86%, total energy by 75% and more predominantly leakage power by 99.9%. Significant reduction in energy can be attributed to the fact that MEM has zero leakage in the OFF state. Output Capacitance (Cout) of MEMS is zero as there exists no parasitic capacitance. With the nature of results obtained when compared with CMOS, it can be affirmed that hybrid MEM/CMOS has a tremendous impact in designing energy efficient FPGA. With the nature of results obtained because of superior characteristics of MEM, we can affirm that usage of MEM in FPGAs possess strong potential to lead innovation and technology breakthroughs in the design of reconfigurable platforms in future Nano technology regime.

V. CHIP SECURITY

Integrated Circuits (IC) manufacturers are outsourcing the fabrication of their (ICs) across the globe. However, there are some disadvantages in this new supply chain mechanism. As the third party manufacturing units are usually located overseas [32], it is not possible to monitor the fabrication processes and practices. This results in potential violation of intellectual Property (IP) rights [33], and possible security and trust risks. Manufacturers require complete design layout details for IC fabrication. With access to the design layout details, it is possible that a design can be modified that may cause damages [34] [36] [35] [37] if not detected before releasing the manufactured devices. The MEM switch with its very low insertion resistance (1 mΩ) offers a way to have design interconnect to be programmable offering secure design environment.

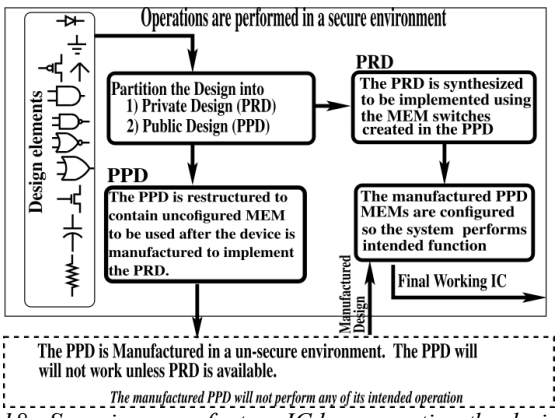

Fig. 18: Securing manufacture IC by encrypting the design using MEMS.

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The process which secure an IC is shown in Fig. 18. The targeted design uses the basic design elements shown inside the box labeled 'Design elements'. The design can be a mixture of low-level transistors, gates and high-level Register Transfer Level (RTL). We assume that the detailed design is performed in a secured and controlled design environment. In this environment, the design is partitioned into two parts, the private design (PRD) and the public design (PPD). The PRD is secured by not disclosing MEM switch location and details to the manufacturer. In other word, keep the PRD inside the secure environment and never let the PRD implementation details leaves the solid box labeled 'Operation is performed in a secure environment'. The PPD is the design that will be revealed to the offshore manufacturing plant. The PPD consists of all design components. The interconnect MEM that correspond to the PRD are left unconnected. The correct MEM switch is in the PRD implementation. They correspond to a sequence of logic low '0' and logic high '1' which stores the correct MEM's PRD function. This sequence is used to configure the PPD MEM of the manufactured device. The correct sequence and how it should be loaded into the storage place holder can only be performed in a secure environment. In this approach, the disclosed PPD does not performs any of its intended functions while outside the secured environment. The only time the PPD can perform its intended function outside the secured environment is when the manufacturer can find the correct sequence that implements the PRD. The PRD consists of a set of n inputs controlling design interconnect. In this way, for each input combination the output of the function must be specified, resulting in 2^n combinations. For large n, it is impossible to find in a finite amount of time the correct interconnect configuration. The MEM switch with its low resistance and capacitance provides superior protection with very low overhead in terms of delays and power consumption.

VI. Power Management

FPGAs used in low power application such as mobile and handheld devices face the challenge of dissipated leakage energy during idle periods [38]. Moreover, there are various embedded system used for event driven applications where lowering the power consumption is critical. This challenge has been addressed by proposing dynamically controlled power gating to controllable logic blocks, power gating in switch blocks [38] and power gating in supply voltage. Power gating with transistors faces challenges like leakage of the power gates and delay due to the voltage drop for the ON resistance of the gates [39][19]. Moreover, in [40] it has been presented that MEMS relay provides energy reduction benefits over MOSFET power gates with even large size and high actuation voltage The ideal power gating technology exhibits infinite OFF resistance and zero ON resistance such as in MEMS switches. Fig. 19 shows a modified MEMS switch based on the cross-bar geometry for power gating. Power gated sub-circuit block and the toggle switch connection with transistors for assisting the toggling action to control power to sub-circuit is presented in Figure 20.

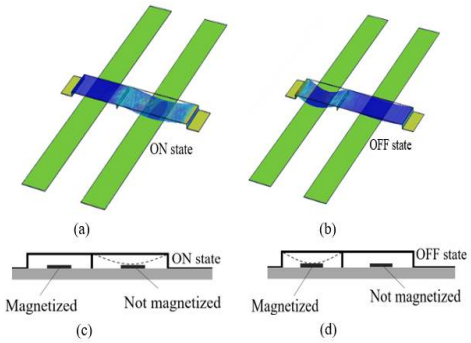

Fig. 19: a) 3D rendering of the ON state of the power gate MEMS switch, b) its OFF state; c) and d) their corresponding 2D renderings.

The area of the top bridge is divided into two section by a support beam in the middle, but it will act as one single bridge. The bridge can be "toggled" between the right and the left side and as the bottom electrodes are magnetized, it will stick when electrostatic actuation will be applied on any one of the sides. When left side will stay on by latching the top electrode to bottom left electrode, right side will stay off. To turn on the right side, electrostatic actuation will force the left side to turn off by pushing the top electrode to the right side. COMSOL simulation showed that the 50 μm long bridge with 100 nm gap with magnetostatic forces, had an actuation voltage of 1.3 V and the electrostatic force is 21.9 μN with turn-on resistance ∼ 1 mΩ which is much lower compared to the CMOS transistors. The turn-off voltage was 1.4V and the electrostatic and magnetostatic forces have behavior, similar to the 200 nm gap magnetic switch characteristics shown in Fig. 8.

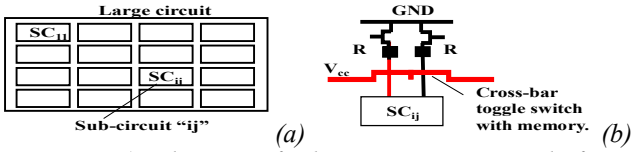

Figure 20: a) Schematic of a large circuit composed of many smaller sub-circuits. b) Schematic of toggle switch connection to control power to sub-circuit "ij."

VII. Conclusion

Design, fabrication and analysis of the cross-bar MEMS switch with ferromagnetic and other electrodes were discussed. A fabrication technique involving very low processing temperatures below 100 °C and using wet and XeF_2 etching was described that is suitable for back-end of the line processing. We showed that both turn-on voltages of these switches can be varied over a large range from 1 V up to 10s of volts. Its speed, however, was somewhat slow in the μs-ns range. We discussed application of these devices in ESD, memory and other IC-related areas including power management, chip security and FPGAs.

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