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Article

Partial Isolation Type Saddle-Finfet(Pi-Finfet) for Sub-30 Nm DRAM Cell Transistors

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Abstract: In this paper, we proposed a novel saddle type FinFET (S-FinFET) to effectively solve problems occurring under the capacitor node of dynamic random-access memory (DRAM) cell and showed how its structure was superior to conventional S-FinFETs in terms of short channel effect (SCE), subthreshold slope (SS), and gate-induced drain leakage (GIDL). The proposed FinFET exhibited 4 times lower Ioff than modified S-FinFET called RFinFET with more improved DIBL characteristics while minimizing Ion reduction compared to RFinFET. Our results also confirmed that the proposed device showed improved DIBL and Ioff characteristics as gate channel length decreased.

Keywords: gate-induced drain leakage (GIDL), drain-induced barrier lowering (DIBL), recessed channel array transistor (RCAT), on-current (I_{on}), off-current (I_{off}), subthreshold slope (SS), threshold voltage (V_{TH}), saddle FinFET (S-FinFET), Potential Drop Width (PDW), Shallow Trench Isolation (STI).

1. Introduction

With decreasing dynamic random-access memory (DRAM) cell size, recessed channel array transistor (RCAT) has been proposed to overcome short channel effect (SCE) of conventional MOSFETs with planar channel. Although recessed channel of RCAT has improved SCE, RCAT suffers from low driving current and V_{TH} sensitivity due to the shape of the bottom corner of the recessed channel [1]. To solve these problems, saddle FinFET (S-FinFET) has been proposed with a tri-gate that wraps both the recessed channel surface and the side surface [2]. S-FinFET not only exhibits excellent short channel effect characteristics, but also maintains excellent subthreshold swing (SS), high I_{on}, and nearly constant V_{TH}. However, S-FinFET has higher gate-induced drain leakage (GIDL) than RCAT because the overlap region between the gate and the drain region is wider in S-FinFET. Although modified S-FinFET called RFinFET has emerged to reduce leakage by GIDL, RFinFET still needs to operate in sub-30nm cell size [3, 4]. Minimizing I_{off} in DRAM applications is a critical issue to achieve long refresh time. If this problem is not addressed, conventional S-FinFETs including S-FinFET and RFinFET will experience significant drawbacks in the application of DRAM technology. In this paper, we proposed a new device with a partial isolation region under the storage node of conventional S-FinFET. This device structure can be fabricated by using an isotropic dry etching technique for the buried insulator under the cell transistor [5, 6]. We analyzed characteristics of this proposed device and compared them with those of conventional S-FinFETs of the same size. We also showed optimized parameters of the buried insulator using a three-dimensional (3D) device

simulator [7]. The device described in this paper has reliable S/D doping concentration with a Gaussian profile. The simulator is well tuned to predict DRAM cell transistor leakage distribution [8, 9].

2. Device Structure

The partial isolation type S-FinFET (Pi-FinFET) is a structure with a buried insulator at a certain depth from the storage node of a conventional S-FinFET. Figure 1a shows a 3-D schematic of a Pi-FinFET. Silicon film thickness, buried insulator thickness, and L_{in} shown in Figure 1a are defined as the distance from the contact surface of the storage node to the buried insulator, the thickness of the buried insulator in the direction perpendicular to the channel, and the distance from the side gate oxide to the buried insulator, respectively. L_g, L_{side}, L_{ov_xj}, and L_{ov_side} represent gate channel length, the length of the side-gate in the direction parallel to the channel, the overlapped length of the side-gate and S/D doping region shown in Figure 1a, and the side-channel width shown in Figure 1c, respectively. When L_{side} and L_{ov_xj} are increased, the width of the overlap region of the gate and the S/D region will also increase. The n^+ poly gate with a gate work function of 4.2eV was applied. L_g, L_{side}, L_{ov_side} and the recessed depth are 30 nm, 42 nm, 10nm and 100nm respectively. RFinFET is the modified S-FinFET with a structure in which the overlap region between the side-gate and the S/D region is removed [3]. Therefore, Pi- FinFETs proposed in this paper can be divided into Pi-SFinFET and Pi-RFinFET depending on the presence or absence of the overlap region between the side-gate and the S/D region. Namely, in this paper, the L_{ov_xj} of Pi-RFinFET is 0nm and that of Pi-SFinFET is 70nm.

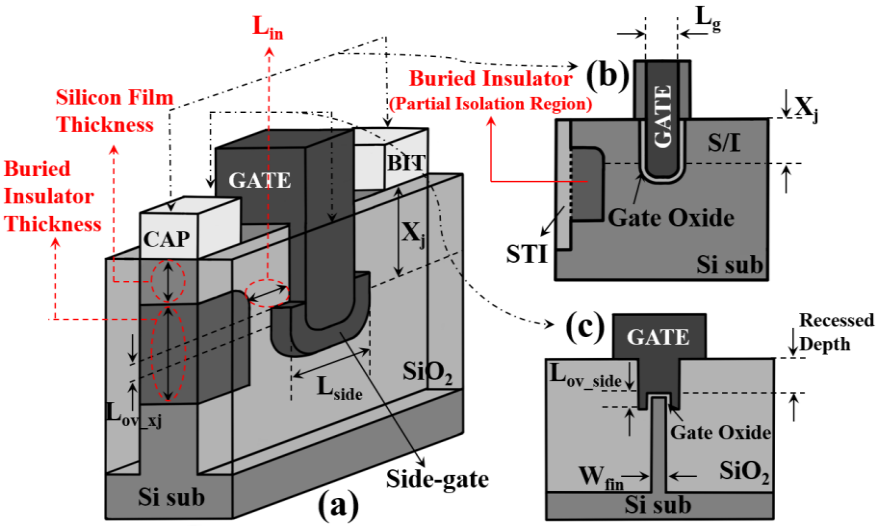

Figure 1. (a) 3-D schematic view of Pi-FinFET. (b) Cross-sectional view across the gate. (c) Cross-sectional view of the thin body. The gate wraps three surfaces of the recessed channel, similar to a FinFET. The buried insulator material is used with SiO_2 below the storage node. The buried insulator is penetrated from the STI region. The X_j of the source/drain (S/D) is located 112nm from the top surface of the S/D region with a Gaussian profile. The peak concentration of the S/D Gaussian doping profile is $1.5 \cdot 10^{20} cm^{-3}$ and the uniform body doping concentration is $5 \cdot 10^{17} cm^{-3}$.

3. Results And Discussion

Log and linear I_D -V_{GS} curves shown in Figure 2 are result of comparing conventional S-FinFETs and RCAT with the Pi-FinFETs proposed in this paper. Silicon film thickness, buried insulator thickness, and L_{in} of Pi-FinFET was set to be 20 nm, 100 nm, and 20 nm, respectively. As shown in Figure 2, the four saddle type FinFETs have significantly lower SS and higher I_{on} than RCAT. Pi-SFinFET has about 3 times smaller I_{off} than S-FinFET while Pi-RFinFET has about 4 times smaller I_{off}

than RFinFET at V_{GS} of -0.5V. To understand physical characteristics of I_{off} reduction for Pi-FinFET, device simulations have been performed using TCAD tool [7, 8].

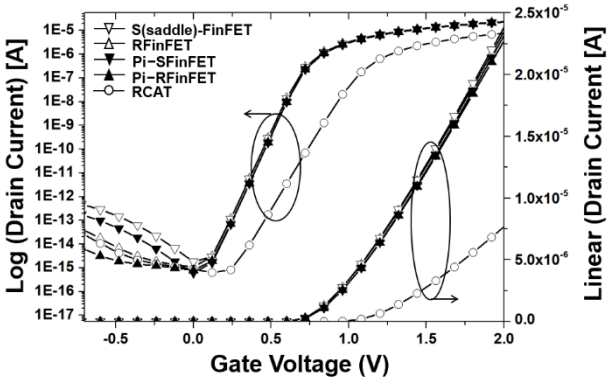

Figure 2. I_{DS}-V_{GS} characteristic for S-FinFET, RFinFET, Pi-FinFETs and RCAT at V_{DS}=1.5V.

Figure 3 shows simulated potential contour near the drain region of conventional S-FinFET and Pi-FinFET at V_{DS} of 1.5V and V_{GS} of -0.5V. We defined the gap of equi-potential lines as the potential drop width (PDW). In particular, dotted arrows in Figures 3a and 3b indicate PDW from 1.8V to -0.4V. As shown in Figure 3(a), the conventional S-FinFET has intensive and narrow PDW from 1.8V to -0.4V near the drain/body (D/B) junction. On the other hand, PDW is mostly limited by the buried insulator of Pi-FinFET as shown in Figure 3b. Namely, the rather constant electric field in the buried insulator of Pi-FinFET induces a wider PDW near the drain region [10]. The dotted red ellipse in Figure 3b shows that the PDW is wider in the silicon layer compared to the conventional S-FinFET. In other words, Pi-FinFET can reduce the electric field affecting GIDL in the silicon layer between the gate and the drain region. Also, the penetration of the electric field from the drain to the source affecting DIBL is minimized in Pi-FinFET.

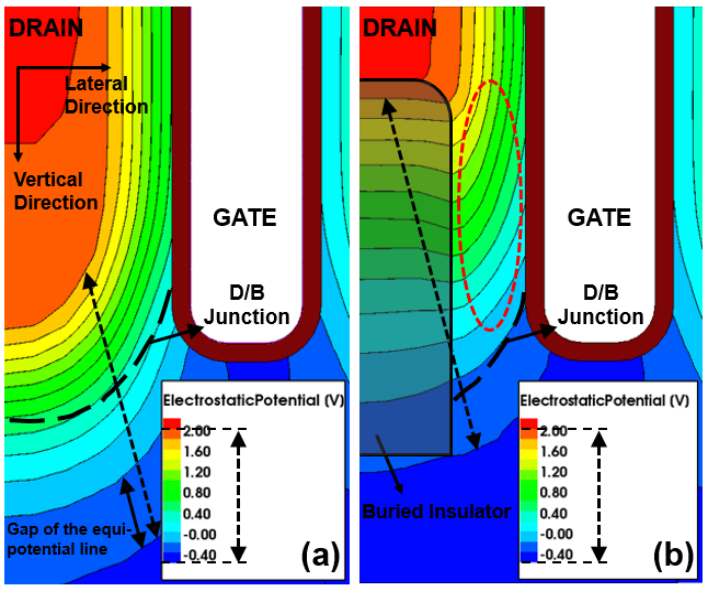

Figure 3. Potential contour indicating equi-potential line distribution near the drain region at V_{DS} = 1.5V, V_{GS} = -0.5V. (a) Conventional S-FinFET, (b) Pi-FinFET. Dotted arrows indicate potential drop width (PDW) from 1.8V to -0.4V while dotted red ellipse shows wider PDW compared to conventional S-FinFET.

Figure 4a shows that I_{off} and I_{on} are decreased when L_{in} is decreased. If L_{in} is very close to 15 nm or less, lateral direction PDW of the silicon layer induced by the buried insulator will become narrow because deep penetration of the buried insulator limits the lateral direction PDW in a narrow silicon

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layer between gate and drain region. As a result, it induces abnormal I_{off} increase and I_{on} decrease as shown in Figure 4a Therefore, in order to maintain a relatively high I_{on} while maintaining a low I_{off}, it is desirable to define L_{in} in the range from 15 to 25 nm in which L_{in} corresponds to the range from 50% to 83.3% of L_g, respectively. As shown in Figure 4a, when L_{in} is 20 nm, I_{off} is minimized. As shown in Figure 4b, SS characteristics are maintained at constant level according to silicon film thickness change. They tend to improve slightly when L_{in} is decreased while DIBL characteristics are consistently improved.

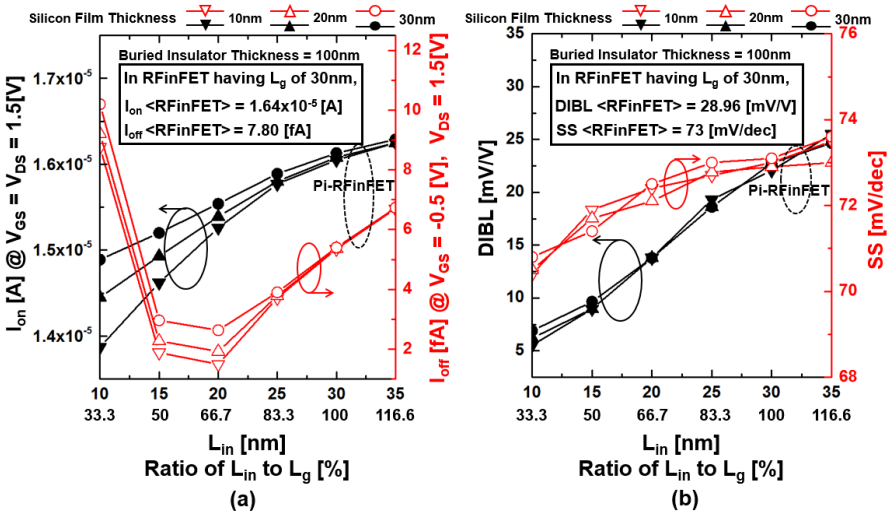

Figure 4. (a). I_{on}, I_{off} and (b) DIBL, SS characteristics of Pi-RFinFET according to L_{in} when L_g is 30nm. And electrical characteristics of RFinFET are displayed in the square box for comparison with Pi-RFinFET when L_g is 30nm.

Figure 5 shows I_{off} and DIBL characteristics according to L_g. L_{in} values in Figure 5 were set to maintain 60% of L_g. Pi-FinFETs consistently exhibited improved I_{off} and DIBL characteristics compared to conventional S-FinFETs regardless of L_g. Especially, Pi-FinFETs exhibited improved DIBL characteristics with opposite tendency compared to conventional S-FinFETs as L_g decreases as shown in Figure 5b. Figure 6 also show DIBL and $g_{m.max}$ characteristics of Pi-FinFETs and S-FinFETs according to the recessed depth. As shown in Figure 6, as the recessed depth decreases, DIBL characteristics of S-FinFETs increases sharply, whereas DIBL of Pi-FinFETs is relatively constant because the PDW of Pi-FinFETs is wider. As the recessed depth decreases, the $g_{m.max}$, which represents the on-current characteristic, is improved. In other words, Pi-FinFETs have found that the recessed depth can be set more flexibly than conventional S-FinFETs.

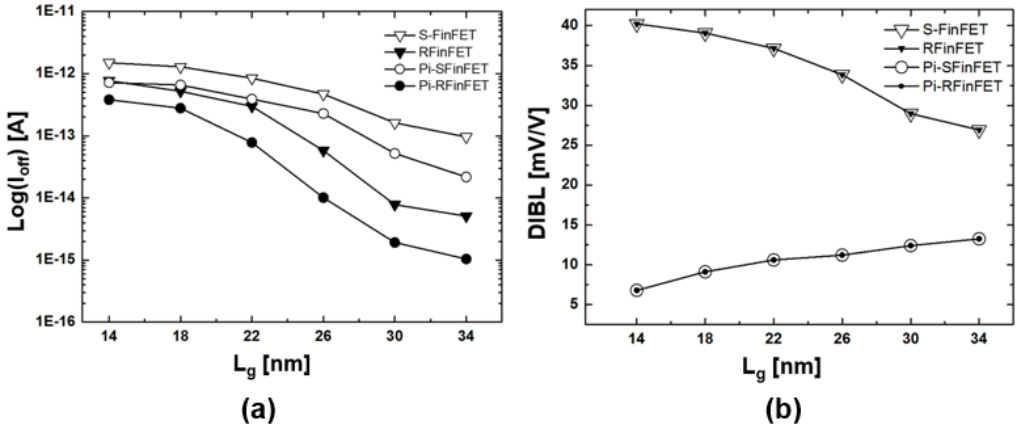

Figure 5. (a) I_{off} (V_{GS} = -0.5V, V_{DS}=1.5V) and (b) DIBL ($V_{DS.low}$=0.05V, $V_{DS.high}$ = 1.5V) dependence on L_g of conventional S-FinFETs and Pi-FinFETs.

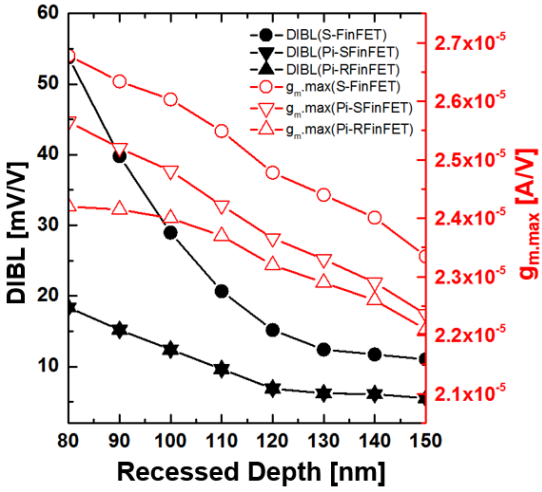

Figure 6. DIBL ($V_{DS.low}$=0.05V, $V_{DS.high}$ = 1.5V) and $g_{m.max}$ characteristics of Pi-FinFETs and S-FinFET according to the recessed depth when L_g is 30nm.

4. Conclusion

We proposed a new device with a partial isolation region under the storage node of the conventional saddle-FinFETs. This device can be classified as either Pi-SFinFET or Pi-RFinFET depending on the overlap area of the side gate and the S/D region. The proposed device not only maintains high DIBL characteristics regardless of the gate channel length, but also reduces the I_{off} by up to four times compared to the conventional saddle-FinFETs. It also minimizes I_{on} reductions. From the study, we concluded that Pi-FinFET is a promising candidate for sub 30nm DRAM technology.

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Conflicts of Interest: The authors declare no conflict of interest.

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