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Article

Multi-port Current Source Inverter for Smart Microgrid Applications: A Cyber Physical Paradigm

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Abstract: This paper presents a configuration of dual output single phase current source inverter with 6 switches for microgrid applications. The inverter is capable of delivering power to two independent set of loads of equal voltages or different voltages at the load end. The control strategy is based on Integral Sliding Mode Control (ISMC). The remote monitoring of the inverter is performed with cyber infrastructure. The cyber physical test bench is developed based on Reconfigurable I/O processor (NI MyRIO-1900) for control and monitoring of the inverter. The inverter prototype is tested in cyber physical test bench in laboratory conditions. The performance of the inverter is analyzed and monitored through the remote system. Also, the inverter is analyzed with different voltage conditions.

Keywords: Cyber physical systems; Dual output inverter ; Rapid control prototype.

1. Introduction

The distributed generation (DG) with photo voltaic, wind energy, fuel cell, and battery termed as microgrid which is able to supply for low and medium voltage applications. The DC microgrid is capable of supplying both DC loads and AC loads with inverter. The inverters for microgrid discussed in [1], [2] are capable of supplying single output. The inverters with reduced semiconductor switches and dual output is capable of feeding dual loads and less complexity in implementation. This enables the feeding of different types of loads using an inverter. The development of inverter with reduced power semiconductor devices make the system economical and compact. The dual output inverters reduces the number of switches in a system and supplies energy to two AC autonomous loads. Four switch inverter [3] is initially proposed with reduced number of switches by replacing split capacitors for sharing between power converters. The dual output voltage source inverters discussed by Yu, Strake et.al [4] are dual phase single DC bus inverter with four switches, three wire single phase inverter with six switches, dual phase dual DC bus inverter with four switch, dual phase with four switch and transformer. The inverter models discussed in [4] has the capability of operating only in half bridge configuration. The dual output single phase inverter based on voltage source inverters (VSI) is proposed by Fatemi, e.al. [5] explains about the half bridge dual output inverter with split capacitor as a sharing leg for both outputs and for the full bridge dual output with six switches, the switch leg is common of for both outputs by sharing a row of switches for upper and lower outputs. The six switch voltage source inverter delivers equal voltage at output with open loop operation. The six switch dual output with buck structure delivers dual output with equal voltage at both output and operated in open loop is presented by Nguyen, et.al. [6]. The dual output inverter with sharing of switch legs will results in reduction of semiconductor switches by 25%.

From literature, most of the researchers concentrate on dual output voltage source inverter rather than dual output current source inverter. The current source inverters (CSI) have inherent short circuit protection owing to the presence of dc link reactor which results in the low harmonic distortion

and better load voltage regulations [7], [8]. The control of CSI is difficult compared to VSI due to the simultaneous regulation of DC link current and output voltage. The dynamic response of CSI is studied using current controller [9] and continuous time based control strategy is employed [10]. The sliding mode control (SMC) [8], [11], [12] provides a dynamic response to the nonlinear systems with the property of hysteresis. It offers stability to variations in system parameters and easy implementations. The sliding surface is created with reference to error variable of inductor current and capacitor voltage for single phase single output CSI is proposed by Komurcugil, et.al. [13]. The sliding mode control for voltage source inverter based shunt active filter is presented in [14] for power quality improvements in power system. The control of y source boost DC-DC converter controlled by cascaded sliding mode control is proposed by Ahmadzadeh et.al. [15]. The control of power electronics equipments using sliding mode control is presented in various literatures for multi-terminal HVDC [16], induction motor control [17], h6 inverter [18], and modular multilevel converter [19]. The SMC [20] based control strategies are applied widely to single output inverters [1], [2] rather than dual output inverters from the literatures. To implement continuous time based control strategies processors with high speed data processing is required. Reconfigurable Input/Output (RIO) based processors are utilised effectively for these types of controllers [21] .

The interfacing of the power electronics circuits to the smart environment [22], [23] makes the system more efficient and controllable. This provides two-way communication between the target and the users (man to machine and vice versa) and results in cyber physical systems (CPS) [24]. The CPS implementation will result in smart grids [25] and remote laboratories for educational purposes. The definition of CPS given by E.A. Lee [26] is that the integration of physical process with embedded computation, controlling and network monitoring along with the feedback loops for computations. In another way CPS is defined as a controllable, credible and scalable network with the physical system. The CPS is stated as $3C's$ (Computations, Communications, and Control). The basic concepts, method, and implementation of CPS is explained briefly by Liu, et.al [27]. CPS implementation for conveyor belt block pickup with application and platform level reconfiguration is in case of faults is presented by Andalam, et.al. [28]. The CPS based optimal power flow management in electric grid with energy demand management is proposed by Nguyen, et.al.[29]. The remote monitoring of microgrid using LabVIEW and PLC is proposed in [30]The researchers developed various CPS models for the physical systems with the utilization of wireless sensor network (WSN), radio frequency identification (RFID), Zigbee, CAN protocols [31–35]. The WSN can only sense signal but not capable of identifying the specific one from more sensors. Similarly, RFID also senses the data based on the perception of data. RFID is widely used in Internet of Things (IoT). While IoT only has the perception of sensing alone, but CPS has the ability of the robust control to the target.

In this paper, the modeling of dual output current source inverter with the capability of operating in equal voltage and different voltage modes at the output end for microgrid applications. The sliding mode control (SMC) strategies are introduced to control the dual output inverter and performance analysis of sliding mode and integral sliding mode control (ISMC) is performed. The comparative analysis of SMC and ISMC reveal the performance and better controller for a dual output current source inverter. The main advantages of ISMC are robustness of large variations, stability, and fast dynamic response. The integration of power electronics devices and cyber physical systems (CPS) is introduced. The Reconfigurable Input/Output (RIO) based embedded control is employed to control and monitor the physical device. The experimental test bench is developed to test the proposed inverter model with ISMC and CPS. The cyber physical system consists of physical device, cyber physical integration layer, and cyber layer. The integration of this heterogeneous frame is needed to deploy on the single platform to reduce the data exchange error occurs while using a different platform for each section. The cyber physical test bench is developed based on LabVIEW, MyRIO, C-DAQ and NI-Web services.

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2. Reconfigurable I/O Test Bench - A Cyber Perspective Model

The Reconfigurable Input/Output (RIO) based design of Cyber-Physical System RCP evaluation test bench is created for the evaluation of two switch dual output inverter with ISMC control. The experimental setup consists of three sections Physical layer, cyber-physical integration layer, and cyber layer. Fig. 6a. shows the configuration of the proposed RCP evaluation of the inverter. The CPS architecture consists of three layers: Physical layer, Cyber Physical integration layer, and Cyber layer. Physical layer comprises of the physical device (target) which needs to be controlled and monitored by CPS. The cyber physical integration layer has the sensors, controllers and software technologies with a host computer to collect the data from the physical device and to control the device based on the responses. The data observed from this layer is monitored and the physical device is controlled by the control center through the internet. The data transfer between the physical device and control center is executed by cyber layer.

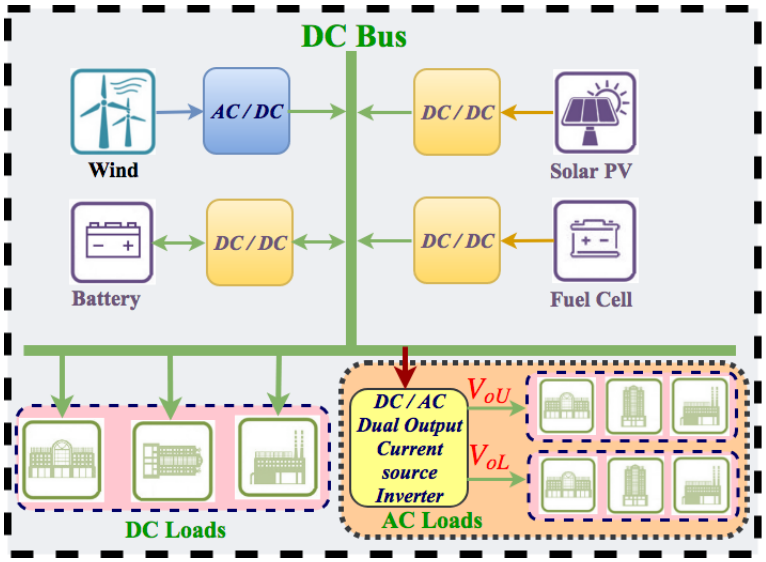

Figure 1. Schematic of Mircogrid

2.1. Physical Layer: Dual Output Current Source Inverter

The microgrid schematic with proposed dual output inverter is shown in Fig.1. The proposed inverter is compared with the family of dual output inverters and given in Table.1. The configuration of proposed dual output current source inverter is shown in Fig.6a.

It consists of a DC link reactor with six semiconductor switches. The inverter has two legs with three semiconductor switches and a sharing row of switches for upper and lower output. The inverter is capable of operating at equal voltages (EV) and different voltages (DV).

Table 1. Comparison of Inverters

Inverter Type	Switches	Source Type	EV	DV
Dual phase with single DC bus with split Capacitor	4	Voltage	Yes	No
Dual phase with three wire	6	Voltage	Yes	No
Dual phase dual DC bus	4	Voltage	Yes	No
Dual phase with transformer	4	Voltage	Yes	No
Dual output VSI	6	Voltage	Yes	No
Proposed	6	Current	Yes	Yes

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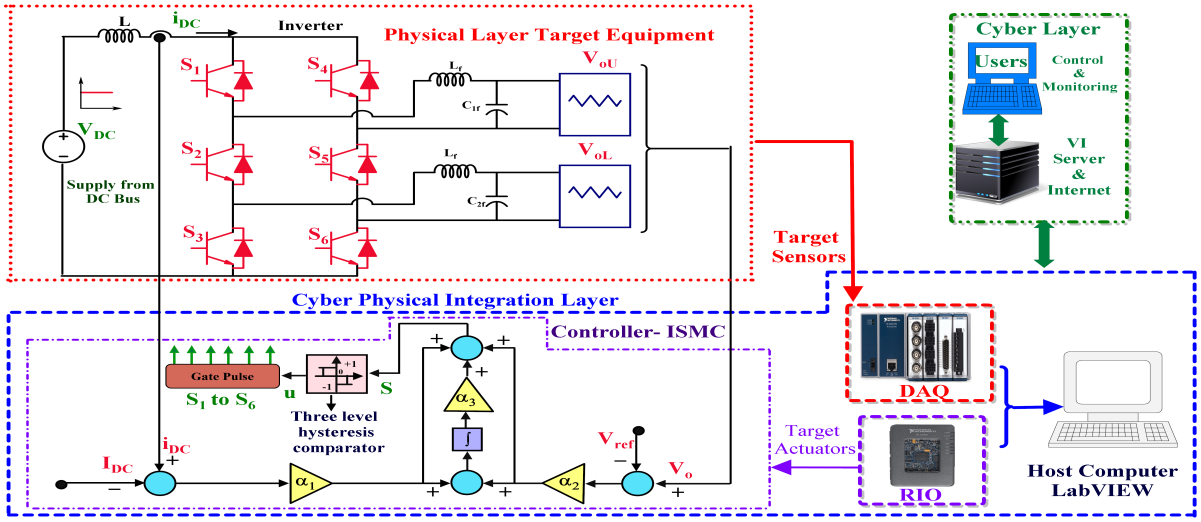

Figure 2. System Configuration

2.1.1. Equal voltage (EV) mode of operation

In this mode, the two ac outputs voltages are independent and equal. The inverter works similar to a full bridge with two parallel loads. The gate signals for upper (S_1, S_4) and lower (S_3, S_6) switches are generated by the control strategy. The control signals for sharing switches (S_2, S_5) is generated by the logical XOR of the upper and lower signals of the same itself. The instantaneous output voltage (v_{on}) of the dual output inverter are same when it operates at EV mode is expressed in (1).

$$v_{on} = v_{oU} = v_{oL} = \sum_{n=1,3,5..}^{\infty} \frac{4V_{DC}}{n\pi} Sinn\omega t \tag{1}$$

2.1.2. Different voltage (DV) mode of operation

In this operating condition, the inverter is capable of delivering different voltage magnitude. The upper side will act as a full bridge and lower will act as a half bridge. The DV mode is in existence due to the presence of DC link reactor. It will protect the inverter from short circuit and floating modes. If the inverter is operated at different voltage mode, the upper side voltage (v_{oU}) will be in full bridge mode as expressed in equation (2) and the lower side (v_{oL}) will be in half bridge mode. The output equations for the half bridge are given by (2).

$$v_{oU} = \sum_{n=1,3,5..}^{\infty} \frac{4V_{DC}}{n\pi} Sinn\omega t, \quad v_{oL} = \sum_{n=1,3,5..}^{\infty} \frac{2V_{DC}}{n\pi} Sinn\omega t \tag{2}$$

2.1.3. System modelling

The dual output inverter is modeled based on CSI topology. It comprises the source voltage (V_S), a DC link reactor (L), IGBT switches, output capacitive filter (C) and a resistive load (R). The equation of the CSI is written as,

$$L\frac{di_{DC}}{dt} + ri_{DC} = V_S - V_{DC} \tag{3}$$

$$C\frac{dv_o}{dt} = i_o - \frac{v_o}{R} \tag{4}$$

where, u is the switching function, $V_{DC} = uv_o$ is the input DC voltage, $i_o = ui_{DC}$ is the output AC current, and r_{idc} the internal resistance of DC link reactor. In order to reduce the computational

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parameters of dual output inverter, it is assumed that $C = C_{1f} = C_{2f}$ as dual output capacitive filter and $v_o = v_{oU} = v_{oL}$ as dual output voltage. The state space for the system operation is described in matrix form is given by (5),

$$\begin{bmatrix} \dot{v_o} \\ \dot{i_o} \end{bmatrix} = \begin{bmatrix} -r/L & -1/L \\ -1/C & -1/RC \end{bmatrix} \begin{bmatrix} v_o \\ i_o \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} u + \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} v_o \\ i_o \end{bmatrix} \tag{5}$$

The transfer function for the system operation is represented in (6),

$$G(s) = \frac{\frac{1}{LC}}{S^2 - S\left(\frac{-L + RC(-r_{idc})}{RCL}\right) + \left(\frac{(-r_{idc}RC - L)LC + RCL}{RC^2L^2}\right)} \tag{6}$$

2.2. Cyber-Physical Integration Layer: C-DAQ, RIO with sliding mode controllers

Cyber-Physical Integration Layer in a CPS incorporates the algorithm to gather sensor information and issue control signals through actuators to the physical device. This layer has software and hardware coordination in-order to control and monitor the physical device. The CPS should behave as, (A) Intelligent: To predict and understand the behaviour of the system using LabVIEW environment, (B) Real-Time : To gather the real-time data from physical device C-DAQ-9174 is utilised, (C) Adaptive & Predictive control: To respond and anticipate the changes in the physical systems the ISMC based control strategy is implemented in MyRIO-1900 .

2.2.1. Sliding Mode Control (SMC)

The Sliding Mode Control (SMC) is an effective controller with switching nature of inverter derived from the system model. The advantages of SMC are, it has a better dynamic response, stability against the variations of the load and easy implementation. It consists of inner and outer control loops. The input inductor current and output capacitor voltage is considered as the state variables for controlling. The error variables are given by,

$$\text{Error Variables} = \begin{cases} x_1 = i_{DC} - I_{DC} \\ x_2 = V_o - V_{ref} \end{cases} \tag{7}$$

The sliding surface (S) of SMC is expressed by (8),

$$S = \alpha_1 x_1 + \alpha_2 x_2 \tag{8}$$

Where, α_1 and α_2 are the sliding coefficients. The additional variable x_3 accumulates directly to the steady state errors of x_1 and x_2. The time derivative of (8) is,

$$\dot{S} = \alpha_1 \dot{x_1} + \alpha_2 \dot{x_2} \tag{9}$$

The derivatives of x_1 and x_2 is given by (10) and (11) ,

$$\dot{x_1} = \frac{1}{L}\left(V_s - r i_{DC} - u v_o\right) - \frac{dI_{DC}}{dt} \tag{10}$$

$$\dot{x_2} = \frac{1}{C}\left(u i_{DC} - \frac{v_o}{R}\right) - \frac{dV_{ref}}{dt} \tag{11}$$

By substituting (10) and (11) in time derivative equation (9) gives (12),

$$\dot{S} = \left(-\frac{u\alpha_1}{L} - \frac{\alpha_2}{RC}\right) v_o + \left(-\frac{\alpha_1 r}{L} + \frac{\alpha_2 u}{C}\right) i_{DC} + A \tag{12}$$

Where A is given by (13),

$$A = \left(\alpha_1 \frac{V_s}{L} - \frac{dI_{DC}\alpha_1}{dt} - \alpha_2 \frac{dV_{ref}}{dt}\right) \tag{13}$$

The condition for stability $S\dot{S} < 0$ should be satisfied and the control variable is given by,

$$u = -signum(S) \tag{14}$$

To satisfy the stability condition,$u = 1$ and $u = -1$ is incorporated to the equation (12).

$$if,\ S < 0 = \dot{S} > 0 \Rightarrow u = 1,$$
$$\dot{S} = \left[\left(-\frac{\alpha_1}{L} - \frac{\alpha_2}{RC}\right) v_o + \left(-\frac{\alpha_1 r}{L} + \frac{\alpha_2}{C}\right) i_{DC} + A\right] > 0 \tag{15}$$

$$if,\ S > 0 = \dot{S} < 0 \Rightarrow u = -1,$$
$$\dot{S} = \left[\left(\frac{\alpha_1}{L} - \frac{\alpha_2}{RC}\right) v_o + \left(-\frac{\alpha_1 r}{L} - \frac{\alpha_2}{C}\right) i_{DC} + A\right] < 0 \tag{16}$$

From equation (15) and (16) the simplified condition for stability is given by (17),

$$0 \quad < \quad \left(-\alpha_1 C + \alpha_2 \frac{L}{R}\right) v_o \ + \ (\alpha_2 L + \alpha_1 r C)\, i_{DC} \ - \ LCA \quad < \quad 2\,(\alpha_2 L i_{DC} - \alpha_1 C v_o) \tag{17}$$

The equivalent continuous control variable u_{eq} is given by (18),

$$u_{eq} = \frac{LC}{v_o C\alpha_1 - \alpha_2 L}\left(-\frac{\alpha_2 v_o}{RC} - \frac{i_{DC}\alpha_1 r}{L} + A\right) \tag{18}$$

The u_{eq} maintains the error variables of the systems. The problem with u_{eq} is complicated while implementing in analog controllers. For the easy implementation of sliding mode control instead of direct implementation of u_{eq}, the switching relay function is used. The switch relay function is given by (19),

$$u_{eq} = \text{-sign(S)} = \begin{cases} +1 & if \ \ S < 0 \\ -1 & if \ \ S > 0 \end{cases} \tag{19}$$

The switching function is realized by *signum* function and direct implementation of this function results in uncontrolled switching frequency and no steady-state errors. Operating of CSI in this condition leads to system failure in practical conditions. To operate CSI with limited frequency and controllable, hysteresis band with boundary layer is utilized. The hysteresis band is implemented instead of *signum* function and the function is given by (20),

$$u = \begin{cases} +1 & if \ \ S < -h \\ -1 & if \ \ S > h \end{cases} \tag{20}$$

The hysteresis bandwidth in S is used to control the dual output CSI with switching frequency, inductor current, and capacitor voltage. If S=0, CSI cannot be controlled. To control dual output CSI, the switching should lie in $S = \pm h$. The performance plot for both inductor current and capacitor output voltage is given in Fig.3a and 3b. The parameters considered are $L = 10mH$, $C = 20\mu F$, $R = 50\Omega$, $\alpha_1 = 0.0002$, $\alpha_2 = 0.2$ and $\alpha_3 = 50$ and are simulated with Matlab.

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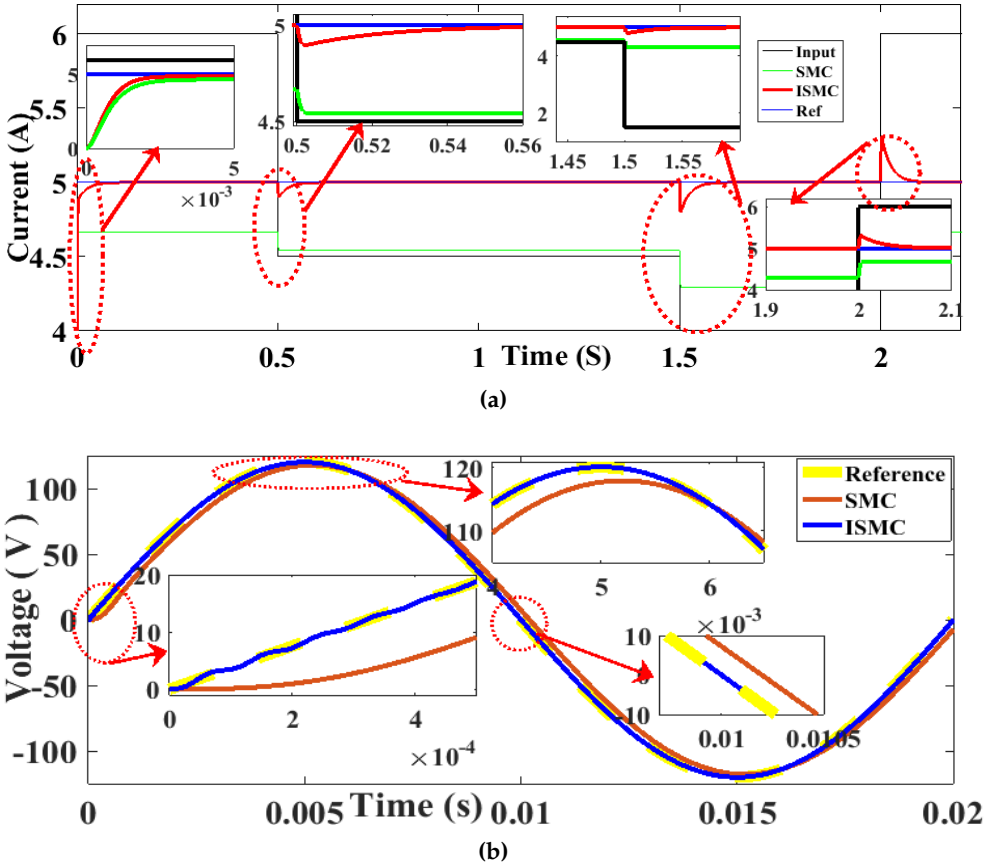

Figure 3. Performance comparision of SMC and ISMC: (a) Input current, (b) Output Voltage

2.2.2. Integral sliding mode control (ISMC)

The SMC based control has steady-state errors in both capacitor output voltage and inductor current. It is observed from Fig.3b, the capacitor output voltage is not tracked with the reference voltage and has a steady-state error of 10%. The steady state error of the inductor current is about 5% as observed from Fig.3a. As a method to suppress the steady state error of the inductor current and output voltage, an additional integral term of the state variables x_1 and x_2 are introduced to the sliding surface. The additional integral term of error variable is introduced into SMC as an additional control variable and stated as integral sliding mode controller (ISMC). The additional variable x_3 is considered and it is obtained by integrating the state variables x_1 and x_2 is given by (21),

$$\text{Error Variable} = x_3 = \int (x_1 + x_2) dt \tag{21}$$

The sliding surface (S) of ISMC is expressed by (22),

$$S = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 \tag{22}$$

Where, α_1, α_2 and α_3 are the sliding coefficients. The additional variable x_3 accumulates directly to the steady state errors of x_1 and x_2. The time derivative of (22) is,

$$\dot{S} = \alpha_1 \dot{x_1} + \alpha_2 \dot{x_2} + \alpha_3 \dot{x_3} \tag{23}$$

$$\dot{x_3} = x_1 + x_2 \tag{24}$$

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The derivatives of x_1, x_2 and x_3 is given by (25), (26) and (27) ,

$$\dot{x_1} = \frac{1}{L}\left(V_s - ri_{DC} - uv_o\right) - \frac{dI_{DC}}{dt} \tag{25}$$

$$\dot{x_2} = \frac{1}{C}\left(ui_{DC} - \frac{v_o}{R}\right) - \frac{dV_{ref}}{dt} \tag{26}$$

$$\dot{x_3} = \left(i_{DC} - I_{DC}\right) + \left(v_o - V_{ref}\right) \tag{27}$$

By substituting (25), (26) and (27) in time derivative equation (23) gives (28),

$$\dot{S} = \left(-\frac{u\alpha_1}{L} - \frac{\alpha_2}{RC} + \alpha_3\right)v_o + \left(-\frac{\alpha_1 r}{L} + \frac{\alpha_2 u}{C} + \alpha_3\right)i_{DC} + B \tag{28}$$

Where B is given by (29),

$$B = \left(\alpha_1\frac{V_s}{L} - \frac{dI_{DC}\alpha_1}{dt} - \alpha_2\frac{dV_{ref}}{dt} - \alpha_3 I_{DC} - \alpha_3 V_{ref}\right) \tag{29}$$

The condition for stability $S\dot{S} < 0$ should be satisfied and the control variable is given by,

$$u = -signum(S) \tag{30}$$

To satisfy the stability condition,$u = 1$ and $u = -1$ is incorporated to the equation (29).

$if,\ S < 0 = \dot{S} > 0 \Rightarrow u = 1,$

$$\dot{S} = \left[\left(-\frac{\alpha_1}{L} - \frac{\alpha_2}{RC} + \alpha_3\right)v_o + \left(-\frac{\alpha_1 r}{L} + \frac{\alpha_2}{C} + \alpha_3\right)i_{DC} + B\right] > 0 \tag{31}$$

$if,\ S > 0 = \dot{S} < 0 \Rightarrow u = -1,$

$$\dot{S} = \left[\left(\frac{\alpha_1}{L} - \frac{\alpha_2}{RC} + \alpha_3\right)v_o + \left(-\frac{\alpha_1 r}{L} - \frac{\alpha_2}{C} + \alpha_3\right)i_{DC} + B\right] < 0 \tag{32}$$

From equation (31) and (32) the simplified condition for stability is given by (33),

$$0 < \left(-\alpha_1 C + \alpha_2\frac{L}{R} - \alpha_3 LC\right)v_o + \left(-\alpha_3 LC + \alpha_2 L + \alpha_1 rC\right)i_{DC} - LCB < 2\left(\alpha_2 L i_{DC} - \alpha_1 C v_o\right) \tag{33}$$

The equivalent continuous control variable u_{eq} is given by (34),

$$u_{eq} = \frac{LC}{v_o C\alpha_1 - \alpha_2 L}\left(-\frac{\alpha_2 v_o}{RC} + v_o\alpha_3 - \frac{i_{DC}\alpha_1 r}{L} + i_{DC}\alpha_3 + B\right) \tag{34}$$

The information about the sliding mode is given by (33). In the proposed ISMC, the condition for stability in (33) is tested by the numerical computations of the sliding coefficients (α_1, α_2 and α_3). The stability is tested along with i_{DC} and v_o minimum and maximum values. And from (33) the equation (35) can be obtained based on the numerical computations.

$$2\left(\alpha_2 L i_{DC} - \alpha_1 C v_o\right) > 0 \tag{35}$$

Due to the stability requirement the sliding coefficients (α_1, α_2 and α_3) will be in positive. In steady state condition $i_{DC} = I_{DC}$. The condition for v_o is given by,

$$\frac{\alpha_2}{\alpha_1} > \frac{Cv_o}{Li_{DC}} \tag{36}$$

The sliding coefficient (α_3) will be determined regardless of (α_1 and α_2) by fine-tuning to obtain the desired response. The block diagram for ISMC is shown in Fig.6a. The switching function is defined by the hysteresis (h) block in the controller design. The hysteresis switching function has three levels $(-1, 0, +1)$. Hysteresis band is fixed based on the reference output voltage (v_o). In general, the hysteresis band (h) will be fixed between 5-10%. The instantaneous hysteresis band is calculated based on the frequency (f) and expressed as (37),

$$\text{Hysteresis band } = \frac{1}{8fL}\left(V_{DC} - \frac{4v_o^2}{V_{DC}}\right) \tag{37}$$

In three-level hysteresis , for $+_{ve}$ operation voltage is $+V_{DC}$ when error reaches the lower hysteresis band ($h_{lower}, -h$) and $'0'$ when reaches lower then '-h'. For $-_{ve}$ operation voltage is $-V_{DC}$ when error reaches the upper hysteresis band ($h_{upper}, +h$) and $'0'$ when reaches higher than '+h'. In two-level hysteresis, the no existence of dead band (t_d) due to the direct transition of $+_{ve}$ to $-_{ve}$ The excursion of sliding surface (S) beyond the hysteresis band (h) results in a dead band (t_d) for semiconductor switches. In three-level hysteresis, the $'0'$ level existence will result in the dead time for semiconductor switches and has less distortion in output voltage. The switching frequency (f_{sw}) for three-level hysteresis function[11] is calculated based on (38),

$$f_{sw} = \frac{\omega_o^2 V_{DC}}{h + t_d \omega_o^2 V_{DC}}\left(\frac{2}{\pi}m - \frac{1}{2}m^2\right) \tag{38}$$

Where, $\omega_o = 2\pi f$, f is the line frequency, m is the amplitude of disturbance. The instantaneous switching frequency (f_{in}) is based on the transition between h_{upper} to h_{lower}. The average switching frequency is calculated with the dead-band of $3\mu s$ and hysteresis width of $0.05V\mu s$ resulted in the average switching frequency of 2.9kHz and the line frequency is 50Hz. The switching function for the inverter model shown in Fig.6a is given by (39),

$$\begin{aligned} u_{1,2} &= \begin{cases} +1 \;\; if \;\; S < -h \\ 0 \;\; if \;\; S > 0 \end{cases} \qquad u_{4,5} = \begin{cases} -1 \;\; if \;\; S > +h \\ 0 \;\; if \;\; S < 0 \end{cases} \\ u_{2,3} &= \begin{cases} +1 \;\; if \;\; S < -h \\ 0 \;\; if \;\; S > 0 \end{cases} \qquad u_{5,6} = \begin{cases} -1 \;\; if \;\; S > +h \\ 0 \;\; if \;\; S < 0 \end{cases} \end{aligned} \tag{39}$$

The sliding surface (S) is the input to the schmitt trigger (hysteresis switching). The schmitt trigger is designed to operate as per the switching conditions (39) for generating control signals. The ISMC respond better than SMC and minimized the steady state errors. The ISMC based control strategy is implemented for the dual output single phase inverter. The controller is designed in reconfigurable input/output (RIO) processor. The experimental test bench is created and the performance of the inverter with the ISMC is analyzed. The performance of the SMC and ISMC is analyzed and shown in Fig.3a and 3b. The inner current control is analyzed by fixing the reference of 5A and changing the input signal of 6A, 4.5A, 1.5A, and 6A. It is inferred from Fig.3a, the settling time for SMC is 0.01s with steady state error of 10% and ISMC has 0.05s with tracking to reference and alleviates the steady state error in the inductor current. From Fig.3a it is observed that the SMC has the high steady state error compared to ISMC. For the outer voltage control loop analysis, the reference voltage is 120V. It is inferred from Fig.3b, the the steady-state error of SMC is 10% and not tracking the reference voltage and ISMC alleviates the steady state error in the voltage and settles at 0.005s with oscillations. The control based on SMC has higher steady state error compared to ISMC. The host computer with LabVIEW, C-DAQ, and MyRIO comprises a cyber-physical integration layer as shown in Fig.1. The LabVIEW is a graphical programming tool with seamless integration of hardware for both data acquisition and controlling the physical devices. The source voltage (V_{ABC}), source current (i_{DC}), output voltage (V_o), output current (i_o) is sensed from the physical device using the NI C-DAQ 9174 with voltage (NI-9225)

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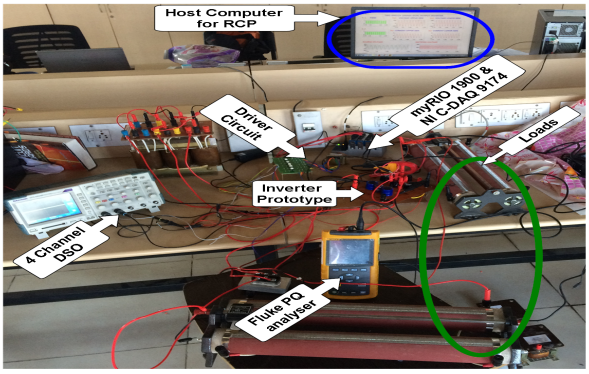

Figure 4. Experimental Setup

and current (NI-9227) sensor. The voltage and current data collected from physical layer are processed in LabVIEW. The acquired signals are monitored in the front panel. the control algorithm for inverter based on ISMC is modeled and block diagram is shown in Fig.1. The controller (actuator) is based on NI-1900 MyRIO (Reconfigurable Input/Output) which has Xilinx Zynq-7010 with a combination of Artix-7 FPGA processor, dual-core ARM Cortex-A9 real-time processor and, onboard WIFI. As an advantage of RIO architecture and WIFI, the physical equipment at a remote location is easily controlled. The terminals are reconfigurable as per the requirements. This leads this test bench to utilize for all power electronics prototype testing. The control algorithm is programmed in NI-My RIO 1900 and connected to the physical device gate driver TI SM72295. The experimental setup is shown in Fig.4.

2.3. Cyber Layer - LabVIEW based CPS

The combination of physical layer and the cyber-physical layer is integrated into the cyber layer. The cyber layer has host computer with server and monitoring station (control center). The data transmission and security is the major concern in the cyber layer. The traditional data transmission is not sufficient to transfer large data in CPS. In order to satisfy the needs, the CPS must have the inbuilt transmission systems. The MyRIO has inbuilt Wi-Fi for data exchange between the host and target. While considering the security of the connection, It utilizes the TCP protocol with SSL.x.509 secured layer to enhance the security. The host computer with LabVIEW has the web service management tool for creating the secured URL. The URL mapping is given by **https://localhost:port address/web service.html**. The LabVIEW has the in-built server for the data exchange with secured network. The collected data from the target is monitored and controlled through the web browser. This method has good live data support, good interaction between the client and user.

Table 2. System Parameters

Parameters	Values (Units)
Maximum Rated Power	1kW
DC Voltage (V_{DC})	120V
Inductor	10mH
IGBT	IRG4BC30S
Diodes	MUR860
Controller	NI myRIO 1900
Data Acquisition Systems	NI C-DAQ 9174
Driver Circuit	Texas Instruments SM72295
Server	NI web server
Network Monitoring	Total Network Manager (TNM)
Oscilloscope	Textronix TPS 2024B four channel

3. Results and Discussions

The performance of the proposed dual output inverter with ISMC control strategy is tested and monitored through the CPS system. The analysis performed under various test conditions like equal output voltage at both upper and lower side, the different output voltage in upper and lower side and inverter analyzed with and without load variations. The control strategy is implemented using reconfigurable input/output (RIO) processor. The hardware prototype is fabricated to demonstrate the proposed inverter. The prototype specifications are given in the Table.2.

3.1. Steady state performance

The steady state performance of the dual output current source inverter is analyzed with ISMC based control strategy. The tracking performance of ISMC is discussed in Section 2.2.2 and performance the comparison of SMC with ISMC is plotted in Fig.3b and 3a. The IMSC alleviates the steady state error and settles at 0.05s. Fig.5 shows the performance of dual output inverter with ISMC. The DC voltage (V_{dc}) and current (I_{dc}) shown in Fig.5a. Due to the current source inverter configuration, the DC link inductor limits the sudden changes in the current and the distortion will get reduced. Fig.5b depicts the dual output voltage and current for 50Hz operation at EV mode. The dual output current source inverter delivers 83V at both load ends (V_{oU}, V_{oL}) due to the DC link of 120V. The upper load current (I_{oU}) 3.60A is observed and lower output current (I_{oL}) is 2.65A. The dual output CSI is, capable of delivering different voltages (DV mode). In this mode, the upper output voltage is similar to full bridge inverter and lower output voltage similar to as half bridge inverter.

Fig.5c shows the upper output voltage (V_{oU}) as 83V and lower voltage (V_{oL}) as 38.4V. The upper load current (I_{oU}) observed is 3.80A and lower load current (I_{oL}) observed is 1.68A. The inverter is operated at both EV and DV mode with ISMC.

3.2. Response to load variations

Fig.5d depicts the step change in both upper and lower load of the dual output current source inverter when operates at EV mode. The inverter operates at 50Hz, the output voltage of upper (V_{oU}) and lower voltage (V_{oL}) is 83V. The IMSC has a robust response to the load variation and maintains the voltage at the desired level. Fig.5e and 5f represents the dual output current source inverter waveforms when a sudden step change in upper or lower load. Fig.5e shows the upper (V_{oU}) and lower voltage (V_{oL}) respectively. The change in upper load (I_{oU}) and current observed is 1.24A and lower load current (I_{oL}) results in 597mA and waveforms shows the change in load. From Fig.5f the EV mode operation with step change in upper load is observed with 83V in upper and lower. The load current in 1.24A and 2.51A respectively. In Fig.5g, the performance of the inverter with ISMC. Resultant waveform evidences the operation of the inverter at a different voltage (DV mode) with variations in load current. Fig.5gshows the upper voltage (V_{oU}) 83V and lower voltage (V_{oL}) 38V with variations in upper load current (I_{oU}) and lower load current (I_{oL}).

In Fig.5h, the performance of inverter in DV mode with a step change in upper load is analyzed and corresponding upper load current (I_{oU}) is 269mA. The lower load current (I_{oL}) inferred is 1.22A. The overall observations from Fig.5 shows that dual output current source inverter has the capability of supplying two independent loads of same (EV mode) and different voltage (DV mode). The dual output current source inverter has the capability of supplying two independent loads of equal (EV mode) and different voltage (DV mode). The dual output inverter can be used in renewable applications to feed simultaneously power to grid and to the stand-alone load. In electric drives applications to operate two different machines of same or different voltage level. The selection of DC link inductor should be concentrated more to obtain the maximum performance of the inverter. Gate pulse generation of the middle switches is critical, due to dual operation.

The performance of the inverter is analysed with single phase power quality analyser (Fluke analyser). Fig.6 depicts the output voltage and current of the Inverter in DV mode. From Fig.6a the

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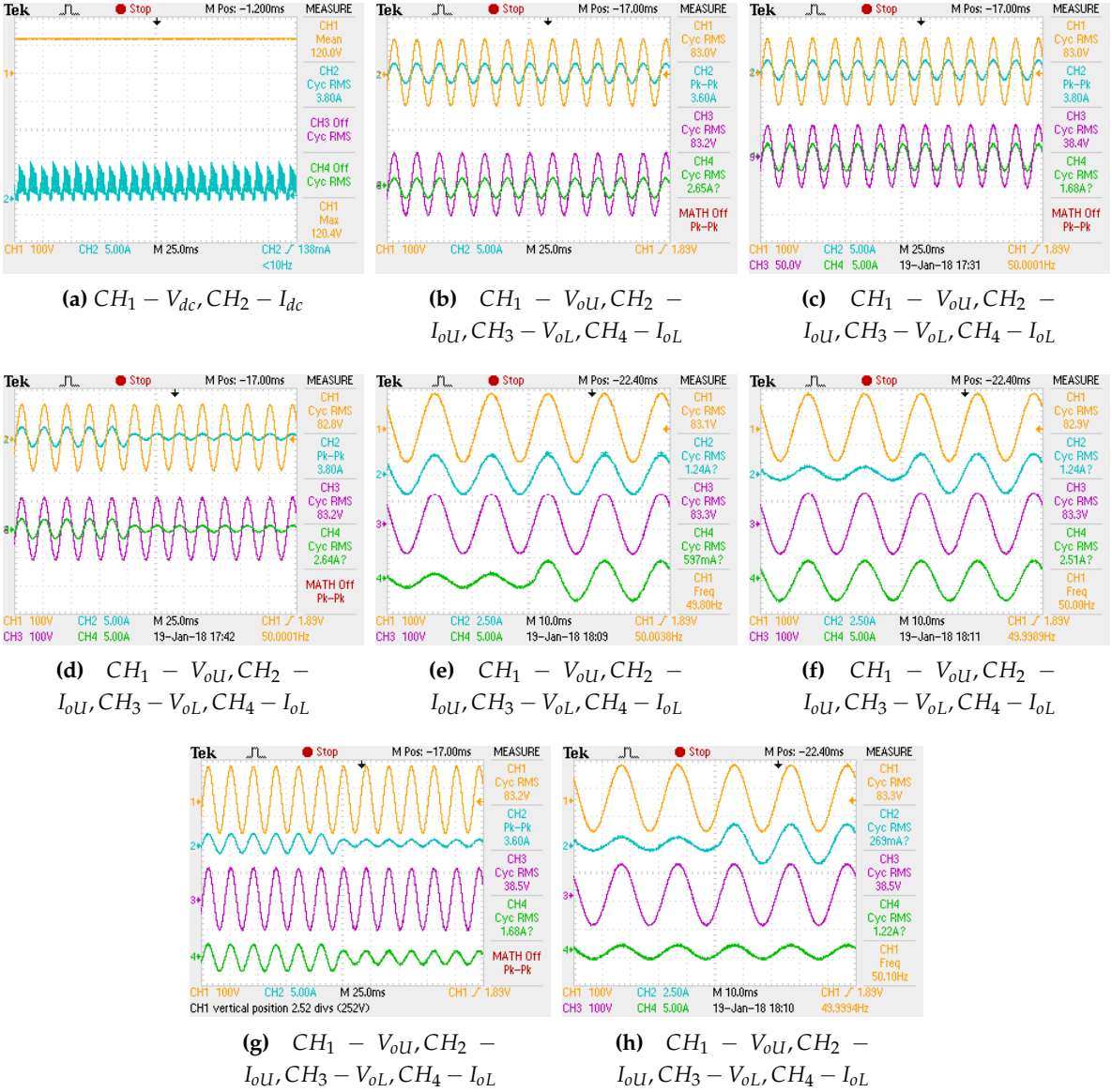

(a) $CH_1 - V_{dc}, CH_2 - I_{dc}$

(b) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$

(c) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$

(d) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$

(e) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$

(f) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$

(g) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$

(h) $CH_1 - V_{oU}, CH_2 - I_{oU}, CH_3 - V_{oL}, CH_4 - I_{oL}$

Figure 5. Prototype Results: (a) DC voltage and current, (b) EV mode output voltage and load current, (c) DV mode output voltage and load current, (d) EV mode output voltage and load current with step change, (e) EV mode output voltage and load current with step change in lower load, (f) EV mode output voltage and load current with step changes in upper load, (g) DV mode output voltage and load current with step changes in load, (h) DV mode output voltage and load current with step change in upper load

upper voltage (V_{oU}) and upper current (I_{oU}) is observed. Fig.6b shows the lower voltage (V_{oL}) and lower current (I_{oL}). The total harmonic distortion (THD) of upper load voltage and current is observed from Fig.6. Fig.6c depicts the THD of upper voltage (V_{oU}) is 4.7% and from Fig.6d it is observed that THD of upper current (I_{oU}) is 5.4%. The total harmonic distortion (THD) of lower load voltage and current is observed from Fig.6. From Fig.6e the THD of lower voltage (V_{oL}) observed is 4.3%. Fig.6f depicts the THD of lower current (I_{oL}) is 4.8%. The THD observed from the results depicts that the THD is under the acceptable limit as per standards IEEE519-2014.

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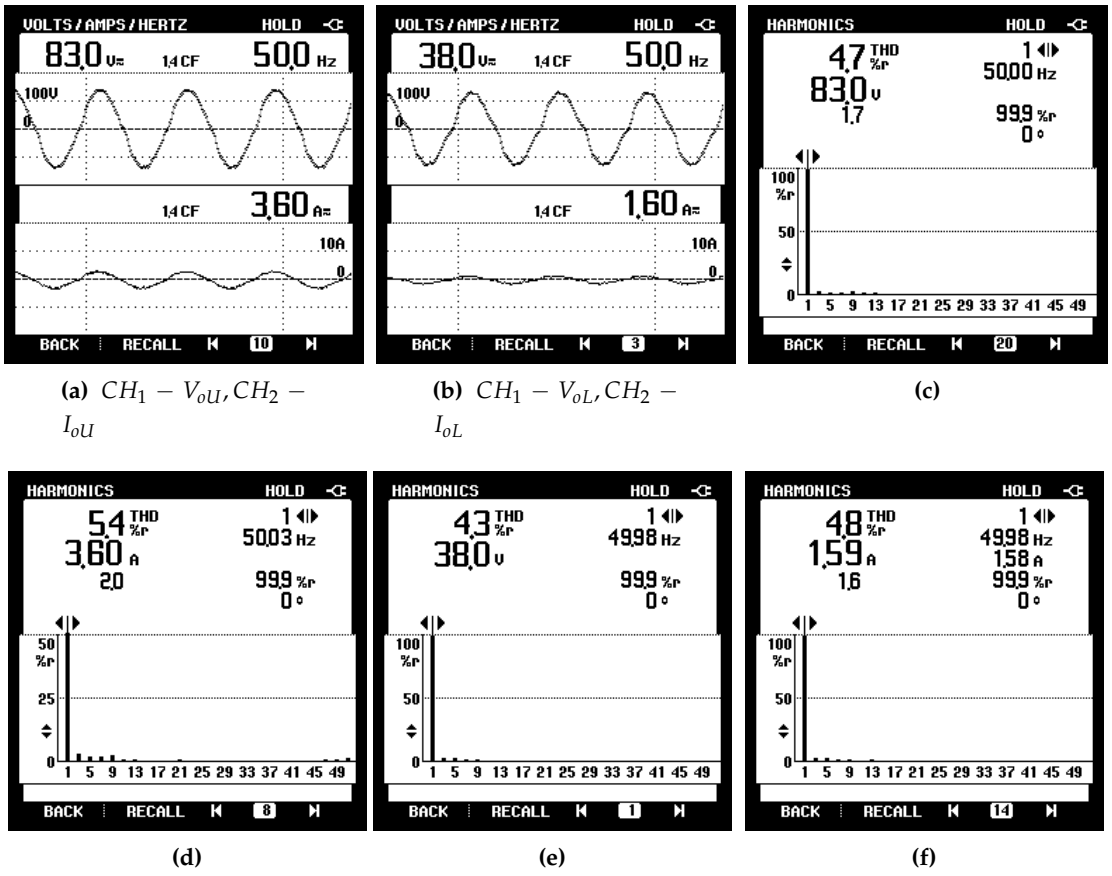

(a) $CH_1 - V_{oU}, CH_2 - I_{oU}$ **(b)** $CH_1 - V_{oL}, CH_2 - I_{oL}$ **(c)**

(d) **(e)** **(f)**

Figure 6. Prototype Results: (a) Upper output voltage and load current, (b) Lower output voltage and load current, (c) Upper output voltage THD, (d) Lower output voltage THD, (e) Upper Current THD, (f) Lower Current THD

3.3. Online monitoring

The CPS design is implemented to evaluate the performance of CSI dual output inverter. The control and monitoring of the target device are done through the internet browser. The connection is based on TCP protocol and SSL.x.509 secured layer is used to ensure the webpage security. From Fig.7 the online monitoring of dual output CSC inverter performance is displayed. The resilient cyber infrastructure designed using single domain has the advantage of lower transport delay and easy implementation compared to other methods. The incorporation of CPS in the inverter model leads to the development of smart grids, smart manufacturing in industries for controlling inverters in drives and smart learning with decentralized control of multiple systems.

4. Conclusion

The dual output current source inverter topology operating in two different voltage mode is presented. A significant advantage of this topology is that it can supply power simultaneously to two different loads of equal (EV mode) and/or different (DV mode) voltages for microgrid applications. The control strategy based on sliding mode controllers is analyzed. The conventional sliding function has the steady state error of 10% for voltage control and 5% for current control. To alleviate the steady state error an additional integral term is introduced and integral sliding mode control is derived for the dual output current source inverter. Reconfigurable Input/ Output processors (MyRIO-1900) with cyber physical test bench is developed to implement continuous time based control strategies,

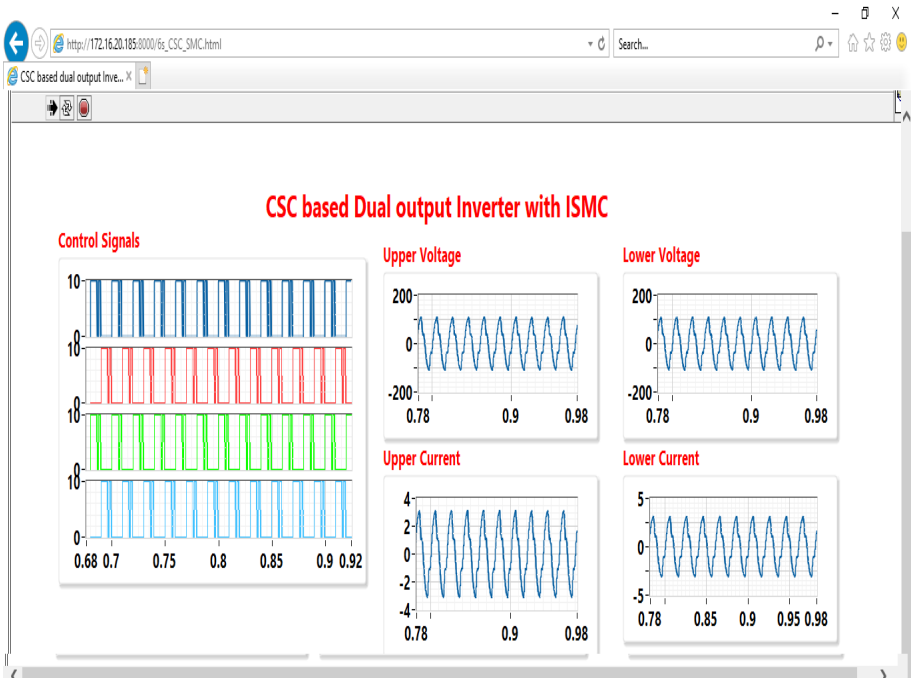

Figure 7. Monitoring Screen

processors with high speed data processing is required. The development the cyber physical system for inverter leads to the development of virtual laboratories and smart grids.

Conflicts of interest

The authors declare that they have no conflicts of interest.

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References

1. Pichan, M.; Karimi, M.; Simorgh, H. Improved low-cost sliding mode control of 4-leg inverter for isolated microgrid applications. *International Transactions on Electrical Energy Systems* **2018**, p. e2642. doi:10.1002/etep.2642.
2. Li, T.; Cheng, Q. Structure analysis and sliding mode control of new dual quasi-Z-source inverter in microgrid. *International Transactions on Electrical Energy Systems* **2018**, p. e2662. doi:10.1002/etep.2662.
3. Jacobina, C.; de Freitas, I.; Lima, A. DC-Link Three-Phase-to-Three-Phase Four-Leg Converters. *IEEE Transactions on Industrial Electronics* **2007**, *54*, 1953–1961. doi:10.1109/tie.2007.895141.
4. Yu, X.; Starke, M.; Tolbert, L.; Ozpineci, B. Fuel cell power conditioning for electric power applications: a summary. *IET Electric Power Applications* **2007**, *1*, 643. doi:10.1049/iet-epa:20060386.
5. Fatemi, A.; Azizi, M.; Mohamadian, M.; Varjani, A.Y.; Shahparasti, M. Single-Phase Dual-Output Inverters With Three-Switch Legs. *IEEE Transactions on Industrial Electronics* **2013**, *60*, 1769–1779. doi:10.1109/tie.2012.2190952.
6. Nguyen, B.L.H.; Cha, H.; Kim, H.G. Single-Phase Six-Switch Dual-Output Inverter Using Dual-Buck Structure. *IEEE Transactions on Power Electronics* **2017**, pp. 1–1. doi:10.1109/tpel.2017.2774363.
7. Senthilnathan, K.; Annapoorani, I. Implementation of unified power quality conditioner (UPQC) based on current source converters for distribution grid and performance monitoring through LabVIEW Simulation

Interface Toolkit server: a cyber physical model. *IET Generation, Transmission & Distribution* **2016**, *10*, 2622–2630. doi:10.1049/iet-gtd.2015.1040.

8. Komurcugil, H. Integral sliding-mode-based current-control strategy for single-phase current-source inverters. *Electrical Engineering* **2011**, *93*, 127–136. doi:10.1007/s00202-011-0197-3.
9. Li, R.T.H.; hung Chung, H.S.; Chan, T.K.M. An Active Modulation Technique for Single-Phase Grid-Connected CSI. *IEEE Transactions on Power Electronics* **2007**, *22*, 1373–1382. doi:10.1109/tpel.2007.900488.
10. Komurcugil, H. Steady-State Analysis and Passivity-Based Control of Single-Phase PWM Current-Source Inverters. *IEEE Transactions on Industrial Electronics* **2010**, *57*, 1026–1030. doi:10.1109/tie.2009.2025297.
11. Kukrer, O.; Komurcugil, H.; Doganalp, A. A Three-Level Hysteresis Function Approach to the Sliding-Mode Control of Single-Phase UPS Inverters. *IEEE Transactions on Industrial Electronics* **2009**, *56*, 3477–3486. doi:10.1109/tie.2009.2016512.
12. Afghoul, H.; Krim, F.; Babes, B.; Beddar, A.; Kihel, A. Design and real time implementation of sliding mode supervised fractional controller for wind energy conversion system under sever working conditions. *Energy Conversion and Management* **2018**, *167*, 91–101. doi:10.1016/j.enconman.2018.04.097.
13. Komurcugil, H.; Biricik, S. Time-Varying and Constant Switching Frequency-Based Sliding-Mode Control Methods for Transformerless DVR Employing Half-Bridge VSI. *IEEE Transactions on Industrial Electronics* **2017**, *64*, 2570–2579. doi:10.1109/tie.2016.2636806.
14. Morales, J.; de Vicuna, L.G.; Guzman, R.; Castilla, M.; Miret, J. Modeling and Sliding Mode Control for Three-Phase Active Power Filters Using the Vector Operation Technique. *IEEE Transactions on Industrial Electronics* **2018**, *65*, 6828–6838. doi:10.1109/tie.2018.2795528.
15. Ahmadzadeh, S.; Markadeh, G.A.; Blaabjerg, F. Voltage regulation of the Y-source boost DC–DC converter considering effects of leakage inductances based on cascaded sliding-mode control. *IET Power Electronics* **2017**, *10*, 1333–1343. doi:10.1049/iet-pel.2016.0767.
16. Musa, A.; Sabug, L.R.; Monti, A. Robust Predictive Sliding Mode Control for Multiterminal HVDC Grids. *IEEE Transactions on Power Delivery* **2018**, *33*, 1545–1555. doi:10.1109/tpwrd.2018.2811560.
17. Wang, H.; Ge, X.; Liu, Y.C. Second-Order Sliding-Mode MRAS Observer Based Sensorless Vector Control of Linear Induction Motor Drives for Medium-Low Speed Maglev Applications. *IEEE Transactions on Industrial Electronics* **2018**, pp. 1–1. doi:10.1109/tie.2018.2818664.
18. Dai, Y.; Zhuang, S.; Ren, H.; Chen, Y.; He, K. Discrete modelling and state-mutation analysis for sliding mode controlled non-isolated grid-connected inverter with H6-type. *IET Power Electronics* **2017**, *10*, 1307–1314. doi:10.1049/iet-pel.2016.0941.
19. Yang, Q.; Saeedifard, M.; Perez, M.A. Sliding Mode Control of the Modular Multilevel Converter. *IEEE Transactions on Industrial Electronics* **2018**, pp. 1–1. doi:10.1109/tie.2018.2818657.
20. Sankar, K.; Jana, A.K. Nonlinear multivariable sliding mode control of a reversible PEM fuel cell integrated system. *Energy Conversion and Management* **2018**, *171*, 541–565. doi:10.1016/j.enconman.2018.05.079.
21. Instruments, N. NI Single-Board RIO General-Purpose Inverter Controller Features. Technical report, National Instruments, 2012.
22. Balda, J.C.; Mantooth, A.; Blum, R.; Tenti, P. Cybersecurity and Power Electronics: Addressing the Security Vulnerabilities of the Internet of Things. *IEEE Power Electronics Magazine* **2017**, *4*, 37–43. doi:10.1109/mpel.2017.2761422.
23. van der Meer, A.A.; et.al, P.P. Cyber-physical energy systems modeling, test specification, and co-simulation based testing. 2017 Workshop on Modeling and Simulation of Cyber-Physical Energy Systems (MSCPES). IEEE, 2017. doi:10.1109/mscpes.2017.8064528.
24. Yoo, H.; Shon, T. Challenges and research directions for heterogeneous cyber–physical system based on IEC 61850: Vulnerabilities, security requirements, and security architecture. *Future Generation Computer Systems* **2016**, *61*, 128–136. doi:10.1016/j.future.2015.09.026.
25. Maffei, A.; et al, S.S. A Cyber-Physical Systems Approach for Implementing the Receding Horizon Optimal Power Flow in Smart Grids. *IEEE Transactions on Sustainable Computing* **2017**, pp. 1–1. doi:10.1109/tsusc.2017.2737144.
26. A, L.E. Computing foundations and practice for CPS: A preliminary report. Technical report, University of California, 2007.

27. Liu, Y.; Peng, Y.; Wang, B.; Yao, S.; Liu, Z. Review on cyber-physical systems. *IEEE/CAA Journal of Automatica Sinica* **2017**, *4*, 27–40. doi:10.1109/jas.2017.7510349.
28. Andalam, S.; Ng, D.J.X.; Easwaran, A.; Thangamariappan, K. Contract-based Methodology for Developing Resilient Cyber-Infrastructure in the Industry 4.0 Era. *IEEE Embedded Systems Letters* **2018**, pp. 1–1. doi:10.1109/les.2018.2801360.
29. Nguyen, V.; Besanger, Y.; Tran, Q.; Nguyen, T. On Conceptual Structuration and Coupling Methods of Co-Simulation Frameworks in Cyber-Physical Energy System Validation. *Energies* **2017**, *10*, 1977. doi:10.3390/en10121977.
30. Gonzalez, I.; Calderon, A.; Andujar, J. Novel remote monitoring platform for RES-hydrogen based smart microgrid. *Energy Conversion and Management* **2017**, *148*, 489–505. doi:10.1016/j.enconman.2017.06.031.
31. Zhang, F.; Liu, M.; Zhou, Z.; Shen, W. An IoT-Based Online Monitoring System for Continuous Steel Casting. *IEEE Internet of Things Journal* **2016**, *3*, 1355–1363. doi:10.1109/jiot.2016.2600630.
32. Moness, M.; Moustafa, A.M. A Survey of Cyber-Physical Advances and Challenges of Wind Energy Conversion Systems: Prospects for Internet of Energy. *IEEE Internet of Things Journal* **2016**, *3*, 134–145. doi:10.1109/jiot.2015.2478381.
33. Gonizzi, P.; Ferrari, G.; Gay, V.; Leguay, J. Data dissemination scheme for distributed storage for IoT observation systems at large scale. *Information Fusion* **2015**, *22*, 16–25. doi:10.1016/j.inffus.2013.04.003.
34. Zhou, P.; Huang, G.; Zhang, L.; Tsang, K.F. Wireless sensor network based monitoring system for a large-scale indoor space: data process and supply air allocation optimization. *Energy and Buildings* **2015**, *103*, 365–374. doi:10.1016/j.enbuild.2015.06.042.
35. Aslan, Y.E.; Korpeoglu, I.; Ulusoy, O. A framework for use of wireless sensor networks in forest fire detection and monitoring. *Computers, Environment and Urban Systems* **2012**, *36*, 614–625. doi:10.1016/j.compenvurbsys.2012.03.002.